74AHC138-Q100; 74AHCT138-Q100

3-to-8 line decoder/demultiplexer; inverting

Rev. 5 — 29 February 2024 Product data sheet

1. General description

The 74AHC138-Q100; 74AHCT138-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74AHC138-Q100; 74AHCT138-Q100 is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address inputs (A0, A1 and A2) and, when enabled, provides eight mutually exclusive outputs ($\overline{Y}0$ to $\overline{Y}7$) that are LOW when selected.

There are three enable inputs: two active LOW ($\overline{E}1$ and $\overline{E}2$) and one active HIGH (E3). Every output will be HIGH unless $\overline{E}1$ and $\overline{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74AHC138-Q100; 74AHCT138-Q100 devices and one inverter. The 74AHC138-Q100; 74AHCT138-Q100 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Inputs accepts voltages higher than V_{CC}
- For 74AHC138-Q100 only: operates with CMOS input levels
- For 74AHCT138-Q100 only: operates with TTL input levels
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC138D-Q100 74AHCT138D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC138PW-Q100 74AHCT138PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC138BQ-Q100 74AHCT138BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram

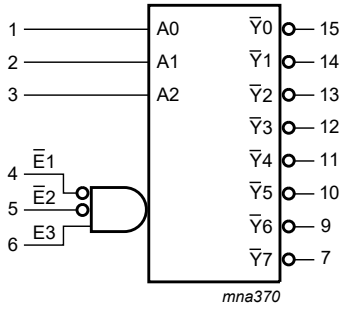


Fig. 1. Logic symbol

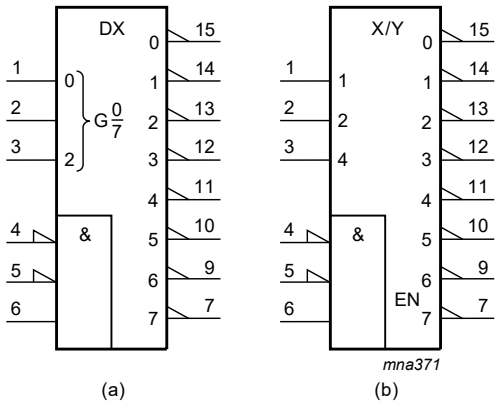


Fig. 2. IEC logic symbol

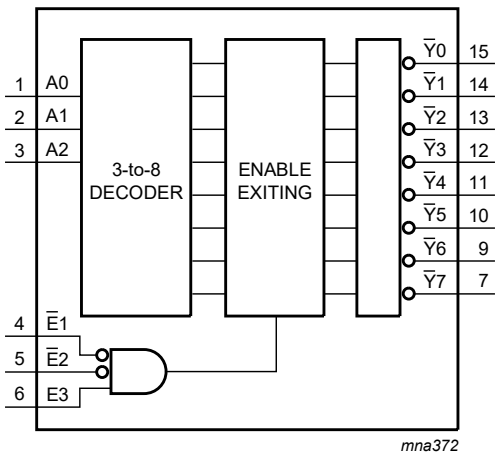
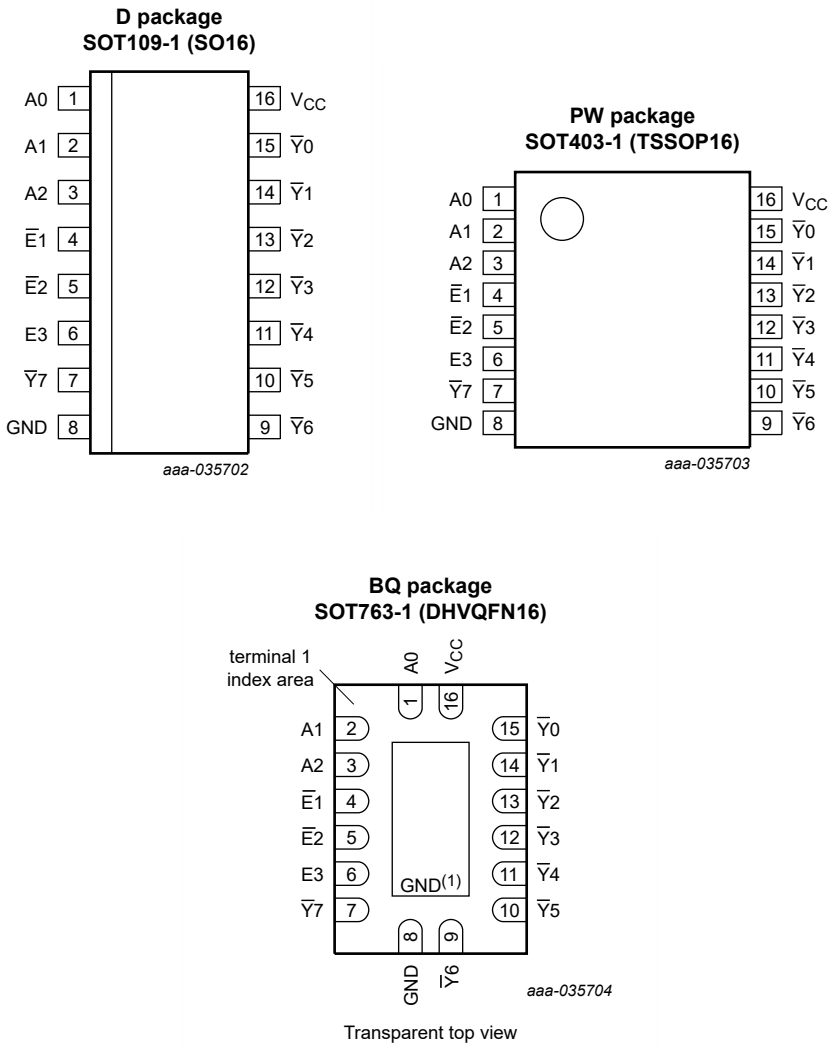


Fig. 3. Functional diagram

5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0	1	address input
A1	2	address input
A2	3	address input
$\overline{E}1$	4	enable input (active LOW)
$\overline{E}2$	5	enable input (active LOW)
E3	6	enable input (active HIGH)
GND	8	ground (0 V)
$\overline{Y}0$, $\overline{Y}1$, $\overline{Y}2$, $\overline{Y}3$, $\overline{Y}4$, $\overline{Y}5$, $\overline{Y}6$, $\overline{Y}7$	15, 14, 13, 12, 11, 10, 9, 7	output
V_{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input						Output							
$\overline{E}1$	$\overline{E}2$	E3	A0	A1	A2	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage			-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V	[1]	-20	-	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	[1]	-	±20	mA
I_O	output current	V_O = -0.5 V to (V_{CC} + 0.5 V)		-	±25	mA
I_{CC}	supply current			-	75	mA
I_{GND}	ground current			-75	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC138-Q100			74AHCT138-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 3.3 V ± 0.3 V	-	-	100	-	-	-	ns/V
		V_{CC} = 5.0 V ± 0.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC138-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = -50 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -50 µA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = -50 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.4	-	V
		I_O = -8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.8	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 50 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V or 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
C_I	input capacitance		-	3.0	10	-	10	-	10	pF
74AHCT138-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -8.0 mA	3.94	-	-	3.8	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V or 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3.0	10	-	10	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

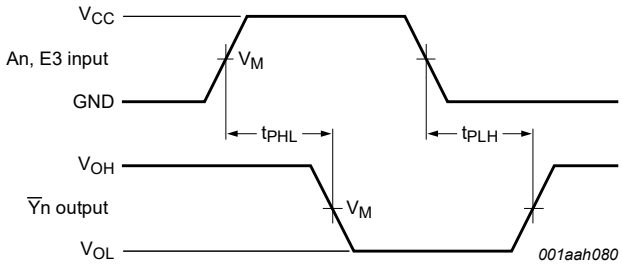
GND = 0 V; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC138-Q100										
t_{pd}	propagation delay	An to $\overline{Y}n$; see Fig. 4 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	6.0	11.4	1.0	13.0	1.0	14.5	ns
		C_L = 50 pF	-	8.6	15.8	1.0	18.0	1.0	20.0	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.4	8.1	1.0	9.5	1.0	10.5	ns
		C_L = 50 pF	-	6.3	10.1	1.0	11.5	1.0	13.0	ns
		E3 to $\overline{Y}n$; see Fig. 4 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.8	12.8	1.0	15.0	1.0	16.0	ns
		C_L = 50 pF	-	8.2	16.3	1.0	18.5	1.0	20.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.2	8.1	1.0	9.5	1.0	10.5	ns
		C_L = 50 pF	-	6.0	10.1	1.0	11.5	1.0	13.0	ns
		$\overline{E}1$, $\overline{E}2$ to $\overline{Y}n$; see Fig. 5 [2]								
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	5.7	11.4	1.0	13.5	1.0	14.5	ns
		C_L = 50 pF	-	8.2	14.9	1.0	17.0	1.0	19.0	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.2	8.1	1.0	9.5	1.0	10.5	ns
		C_L = 50 pF	-	6.0	10.1	1.0	11.5	1.0	13.0	ns
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	18.0	-	-	-	-	-	pF
74AHCT138-Q100										
t_{pd}	propagation delay	An to $\overline{Y}n$; see Fig. 4 [2]								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.4	10.4	1.0	12.0	1.0	13.0	ns
		C_L = 50 pF	-	6.2	11.4	1.0	13.0	1.0	14.5	ns
		E3 to $\overline{Y}n$; see Fig. 4 [2]								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.3	9.1	1.0	10.5	1.0	11.5	ns
		C_L = 50 pF	-	6.2	10.1	1.0	11.5	1.0	13.0	ns
		$\overline{E}1$, $\overline{E}2$ to $\overline{Y}n$; see Fig. 5 [2]								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	4.3	9.6	1.0	11.0	1.0	12.0	ns
		C_L = 50 pF	-	6.2	10.6	1.0	12.0	1.0	13.5	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	23.0	-	-	-	-	-	pF

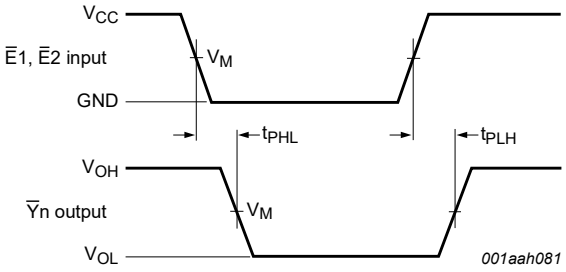
[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz, f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. The inputs An, E3 to outputs $\overline{Y}$n propagation delays

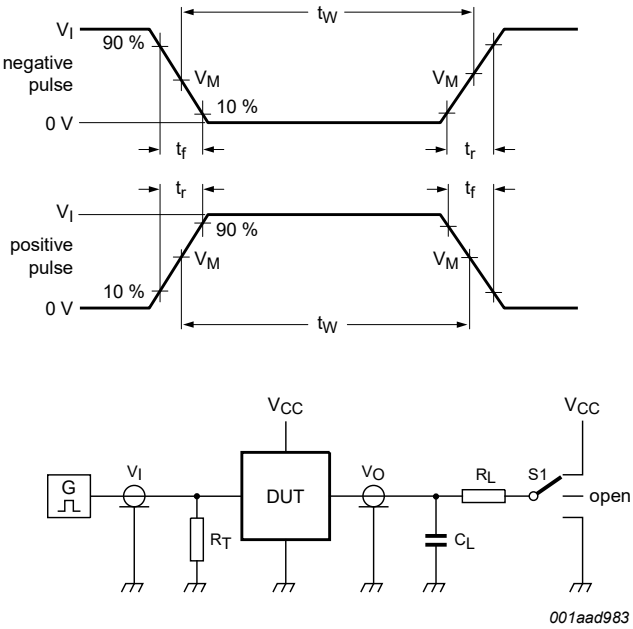


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. The inputs $\overline{E}$n to outputs $\overline{Y}$n propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC138-Q100	0.5 × V_{CC}	0.5 × V_{CC}
74AHCT138-Q100	1.5 V	0.5 × V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

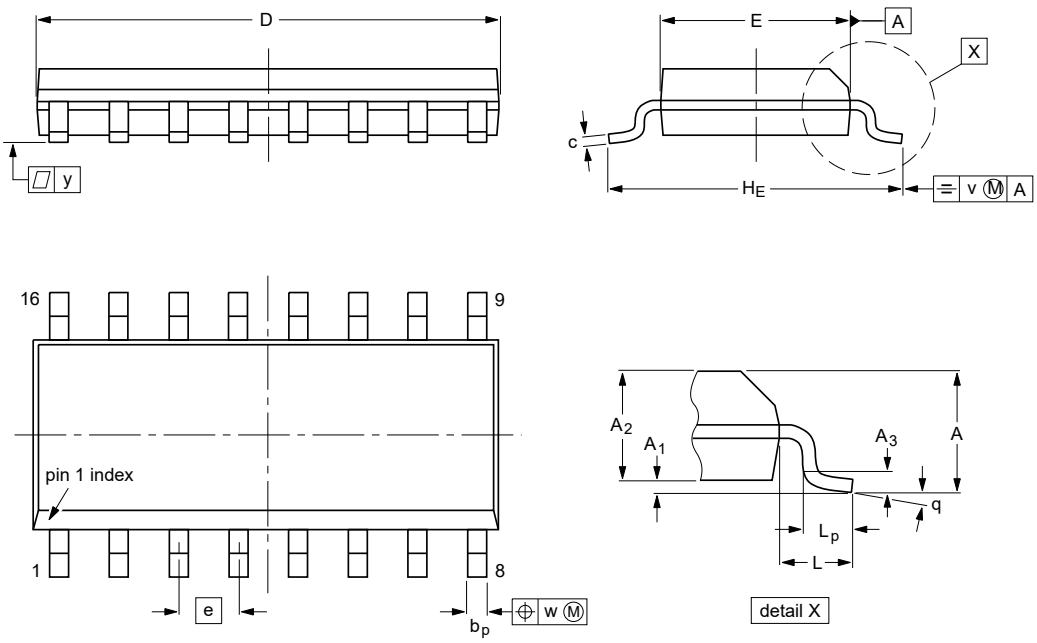
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74AHC138-Q100	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74AHCT138-Q100	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

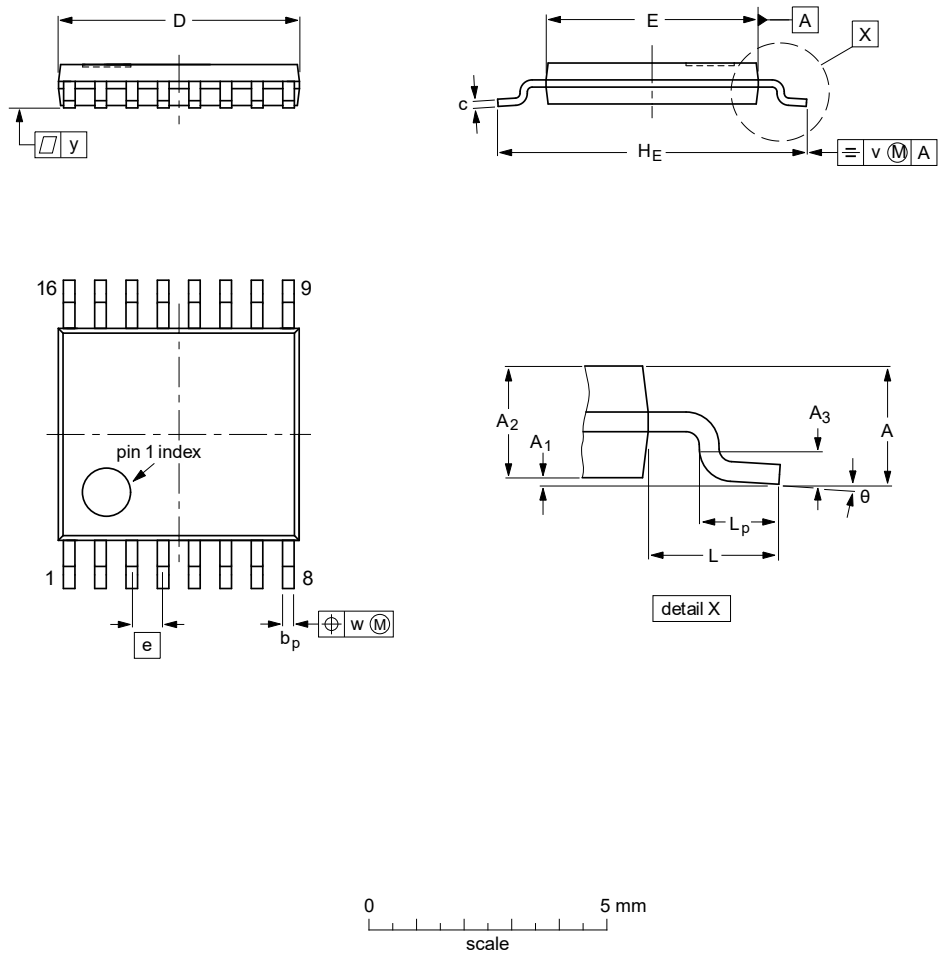
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

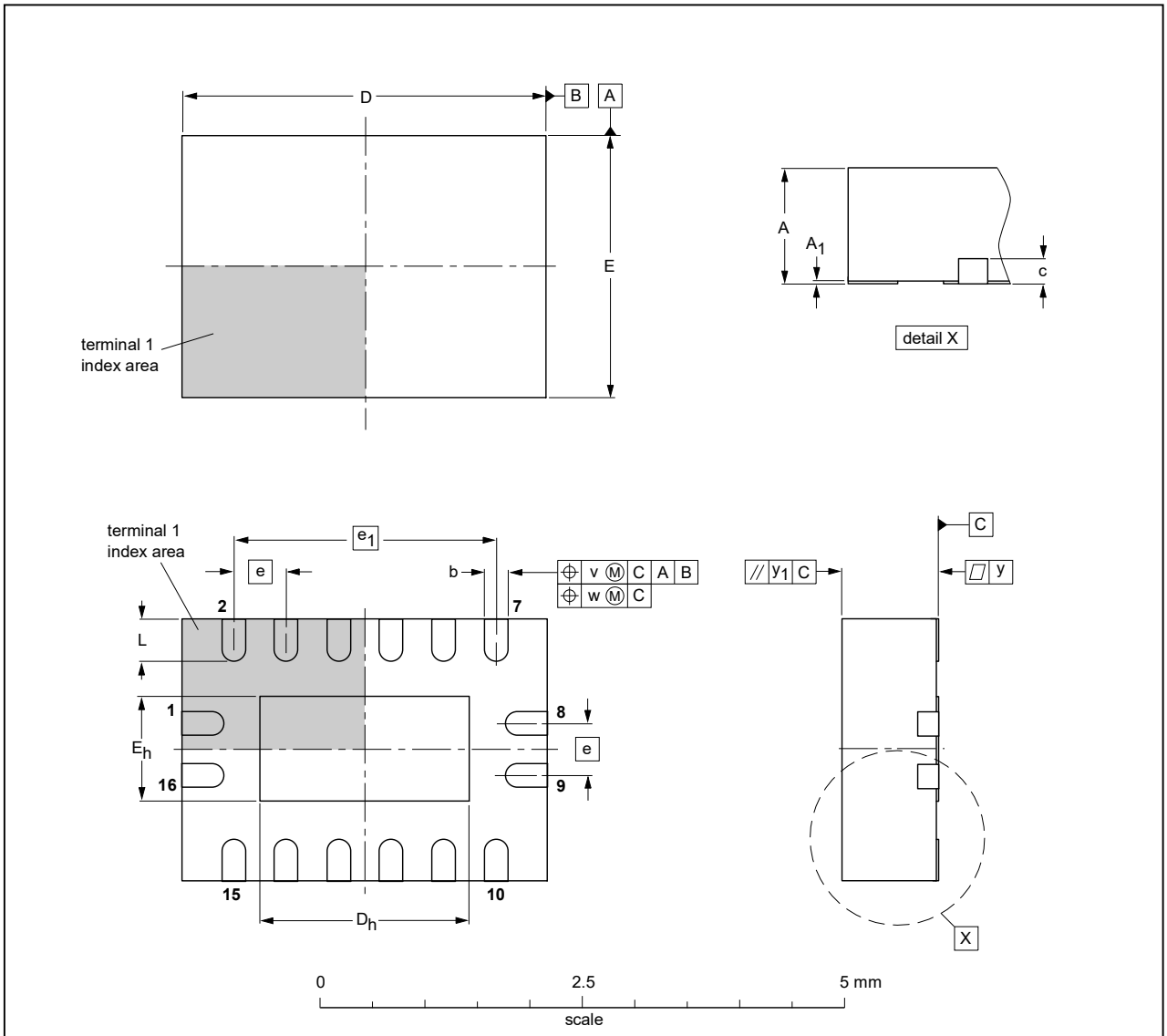
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig. 9. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT138_Q100 v.5	20240229	Product data sheet	-	74AHC_AHCT138_Q100 v.4
Modifications:	• Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74AHC_AHCT138_Q100 v.4	20230904	Product data sheet	-	74AHC_AHCT138_Q100 v.3
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AHC_AHCT138_Q100 v.3	20200910	Product data sheet	-	74AHC_AHCT138_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74AHC_AHCT138_Q100 v.2	20140402	Product data sheet	-	74AHC_AHCT138_Q100 v.1
Modifications:	• Description for t_{pd} for the 74AHCT138-Q100 corrected (errata) in Table 7.			
74AHC_AHCT138_Q100 v.1	20130326	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 29 February 2024