74ALVC74-Q100

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 2 — 5 February 2024 Product data sheet

1. General description

The 74ALVC74-Q100 is a dual positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 3.6 V
- CMOS low power dissipation
- Overvoltage tolerant inputs to 3.6 V
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD78 Class II.A
- Complies with JEDEC standard:
  - JESD8-7 (1.65 to 1.95 V)
  - JESD8-5 (2.3 to 2.7 V)
  - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC74PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

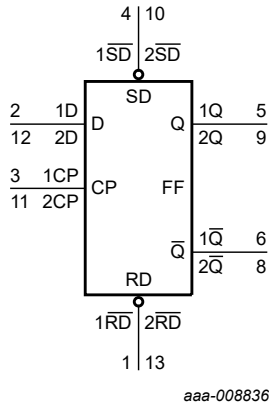

Fig. 1. Logic symbol

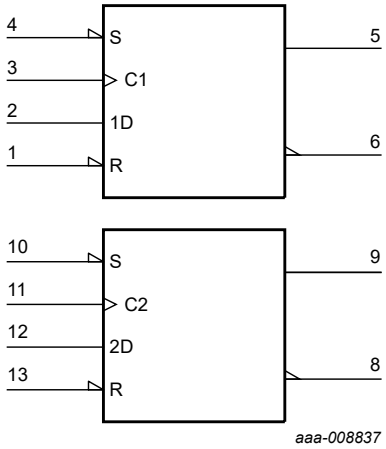

Fig. 2. IEC logic symbol

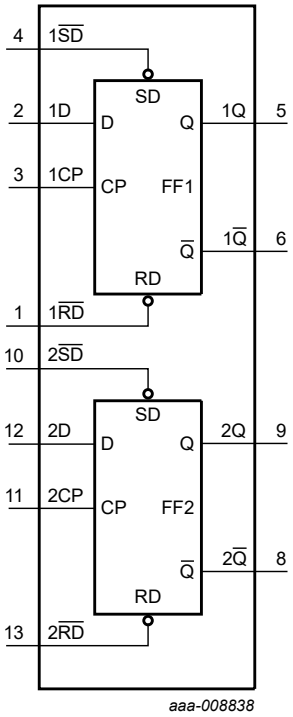

Fig. 3. Functional diagram

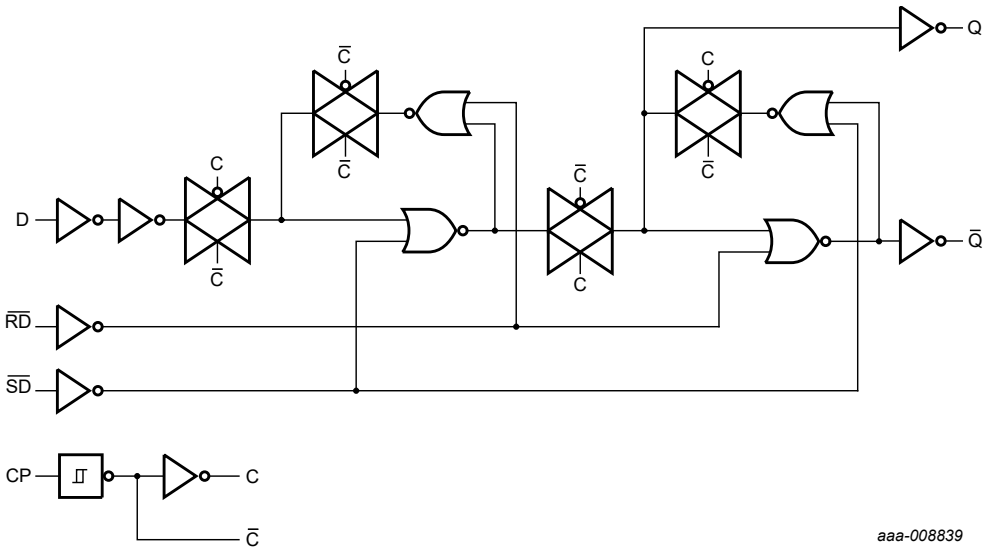

Fig. 4. Logic diagram (one flip-flop)

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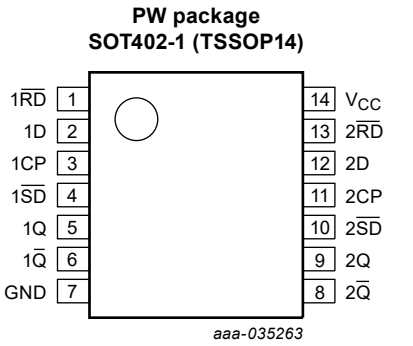
5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{RD}$	1	asynchronous reset-direct input (active-LOW)
1D	2	data input
1CP	3	clock input (LOW-to-HIGH), edge-triggered
1$\overline{SD}$	4	asynchronous set-direct input (active-LOW)
1Q	5	true flip-flop output
1$\overline{Q}$	6	complement flip-flop output
GND	7	ground (0 V)
2$\overline{Q}$	8	complement flip-flop output
2Q	9	true flip-flop output
2$\overline{SD}$	10	asynchronous set-direct input (active-LOW)
2CP	11	clock input (LOW-to-HIGH), edge-triggered
2D	12	data input
2$\overline{RD}$	13	asynchronous reset-direct input (active-LOW)
V_{CC}	14	supply voltage

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6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition; nQ_{n+1} = state after the next LOW-to-HIGH CP transition.

Input				Output			
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$	nQ_{n+1}	$n\overline{Q}_{n+1}$
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage		[1]	-0.5	+4.6	V
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+4.6	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	V_{CC} = 1.65 to 3.6 V	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature	in free air	-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	-	-	0.65 × V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35 × V_{CC}	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		V_{CC} = 1.65 V to 3.6 V; I_O = -100 µA	V_{CC} - 0.2	-	-	V_{CC} - 0.2	-	V
		V_{CC} = 1.65 V; I_O = -6 mA	1.25	1.51	-	1.25	-	V
		V_{CC} = 2.3 V; I_O = -12 mA	1.8	2.10	-	1.8	-	V
		V_{CC} = 2.3 V; I_O = -18 mA	1.7	2.01	-	1.7	-	V
		V_{CC} = 2.7 V; I_O = -12 mA	2.2	2.53	-	2.2	-	V
		V_{CC} = 3.0 V; I_O = -18 mA	2.4	2.76	-	2.4	-	V
		V_{CC} = 3.0 V; I_O = -24 mA	2.2	2.68	-	2.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		V_{CC} = 1.65 V to 3.6 V; I_O = 100 µA	-	-	0.2	-	0.2	V
		V_{CC} = 1.65 V; I_O = 6 mA	-	0.11	0.3	-	0.3	V
		V_{CC} = 2.3 V; I_O = 12 mA	-	0.17	0.4	-	0.4	V
		V_{CC} = 2.3 V; I_O = 18 mA	-	0.25	0.6	-	0.6	V
		V_{CC} = 2.7 V; I_O = 12 mA	-	0.16	0.4	-	0.4	V
		V_{CC} = 3.0 V; I_O = 18 mA	-	0.23	0.4	-	0.45	V
		V_{CC} = 3.0 V; I_O = 24 mA	-	0.30	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	±0.1	±5	-	±20	µA
I_{OFF}	power-off leakage current	V_{CC} = GND; V_I or V_O = 3.6 V	-	±0.1	±10	-	±80	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.2	10	-	80	µA
ΔI_{CC}	additional supply current	V_{CC} = 3.0 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	750	-	750	µA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V): for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, n$\overline{Q}$; see Fig. 5 [2]						
		V_{CC} = 1.65 to 1.95 V	1.0	3.7	6.2	1.0	7.1	ns
		V_{CC} = 2.3 to 2.7 V	1.0	2.6	4.2	1.0	4.8	ns
		V_{CC} = 2.7 V	1.0	2.8	4.2	1.0	4.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.7	3.8	1.0	4.4	ns
		n$\overline{SD}$ to nQ, n$\overline{Q}$; see Fig. 6						
		V_{CC} = 1.65 to 1.95 V	1.0	3.4	5.4	1.0	6.2	ns
		V_{CC} = 2.3 to 2.7 V	1.0	2.4	3.8	1.0	4.4	ns
		V_{CC} = 2.7 V	1.0	3.2	4.2	1.0	4.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	3.5	1.0	4.0	ns
		n$\overline{RD}$ to nQ, n$\overline{Q}$; see Fig. 6						
		V_{CC} = 1.65 to 1.95 V	1.0	3.5	5.4	1.0	6.2	ns
		V_{CC} = 2.3 to 2.7 V	1.0	2.5	3.8	1.0	4.4	ns
		V_{CC} = 2.7 V	1.0	3.1	4.2	1.0	4.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	3.5	1.0	4.0	ns
t_W	pulse width	nCP; HIGH or LOW; see Fig. 5						
		V_{CC} = 1.65 to 1.95 V	2.5	0.9	-	2.5	-	ns
		V_{CC} = 2.3 to 2.7 V	2.5	0.6	-	2.5	-	ns
		V_{CC} = 2.7 V	2.5	1.3	-	2.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	1.3	-	2.5	-	ns
		n$\overline{SD}$ or n$\overline{RD}$; LOW; see Fig. 6						
		V_{CC} = 1.65 to 1.95 V	2.5	0.9	-	2.5	-	ns
		V_{CC} = 2.3 to 2.7 V	2.5	0.6	-	2.5	-	ns
		V_{CC} = 2.7 V	2.5	1.0	-	2.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	0.7	-	2.5	-	ns
t_{rec}	recovery time	n$\overline{RD}$ to nCP; see Fig. 6						
		V_{CC} = 1.65 to 1.95 V	0.7	−0.1	-	0.7	-	ns
		V_{CC} = 2.3 to 2.7 V	0.7	−0.1	-	0.7	-	ns
		V_{CC} = 2.7 V	0.7	−0.1	-	0.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.7	−0.1	-	0.7	-	ns
t_{su}	set-up time	nD to nCP; see Fig. 5						
		V_{CC} = 1.65 to 1.95 V	1.2	0.6	-	1.2	-	ns
		V_{CC} = 2.3 to 2.7 V	1.2	0.8	-	1.2	-	ns
		V_{CC} = 2.7 V	0.9	0.5	-	0.9	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.8	0.4	-	0.8	-	ns

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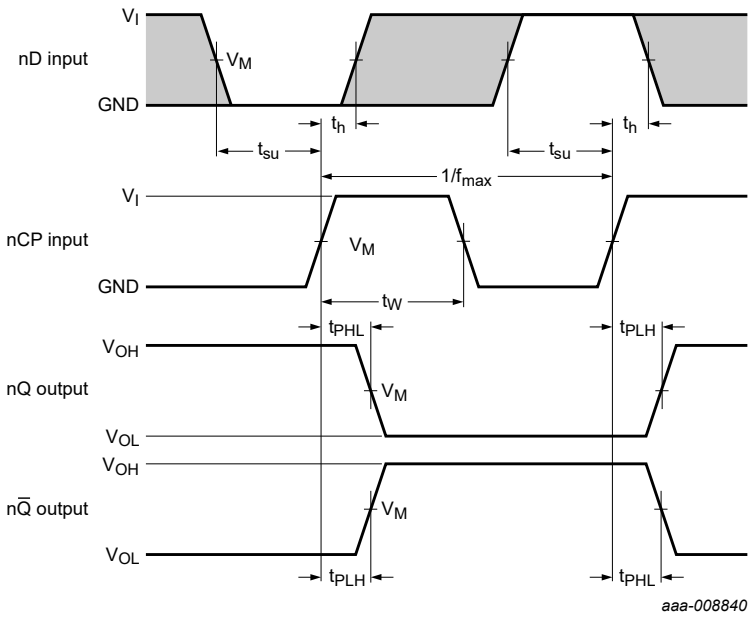
Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_h	hold time	nD to nCP; see Fig. 5						
		V_{CC} = 1.65 to 1.95 V	0.6	−0.4	-	0.6	-	ns
		V_{CC} = 2.3 to 2.7 V	0.6	−0.3	-	0.6	-	ns
		V_{CC} = 2.7 V	0.7	−0.4	-	0.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.8	−0.1	-	0.8	-	ns
f_{max}	maximum frequency	nCP; see Fig. 5						
		V_{CC} = 1.65 to 1.95 V	150	275	-	150	-	MHz
		V_{CC} = 2.3 to 2.7 V	200	325	-	200	-	MHz
		V_{CC} = 2.7 V	250	375	-	250	-	MHz
		V_{CC} = 3.0 V to 3.6 V	300	425	-	300	-	MHz
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]	-	35	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
Typical values are measured at V_{CC} = 1.8 V for V_{CC} = 1.65 V to 1.95 V.
Typical values are measured at V_{CC} = 2.5 V for V_{CC} = 2.3 V to 2.7 V.
Typical values are measured at V_{CC} = 3.3 V for V_{CC} = 3.0 V to 3.6 V

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$, where:
f_i = input frequency in MHz; f_o = output frequency in MHz;
N = total load switching outputs; C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5. Clock pulse (nCP) to output (nQ, nQ̄) propagation delays, nCP pulse width, the nD to nCP set-up times, the nCP to nD hold times and maximum frequency

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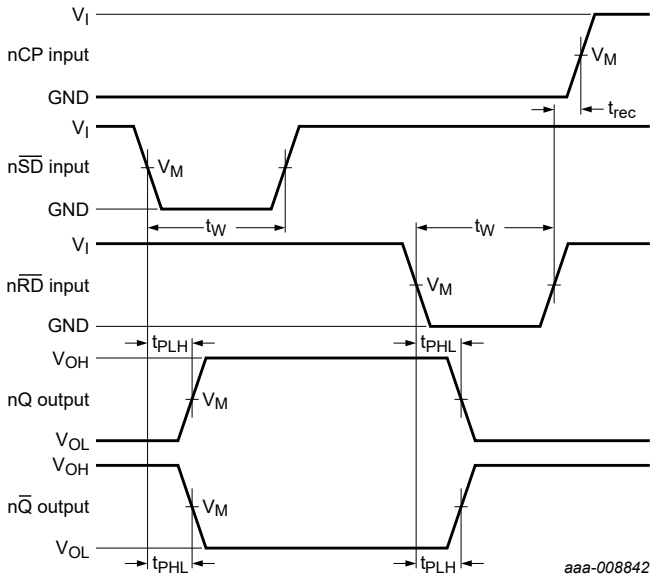

Measurement points are given in Table 8.

Fig. 6. Set ($\overline{nSD}$) and reset ($\overline{nRD}$) input to output (nQ, $\overline{nQ}$) propagation delays, set ($\overline{nSD}$) and reset ($\overline{nRD}$) pulse widths and $\overline{nRD}$ to nCP recovery time

Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.65 V to 1.95 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.3 V to 2.7 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V

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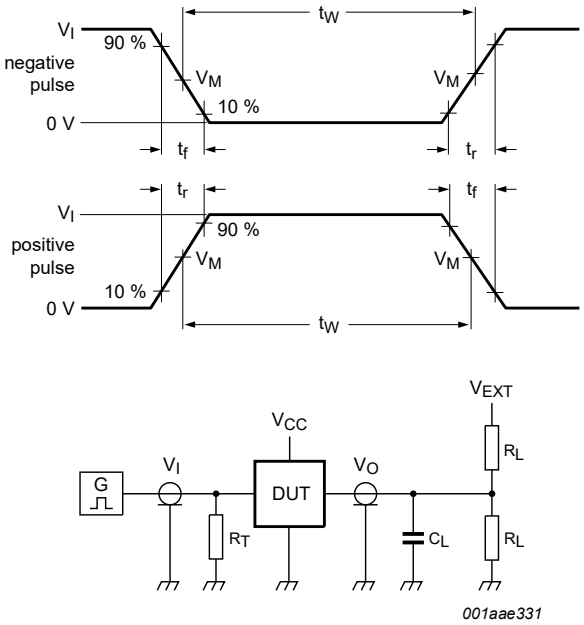

Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open

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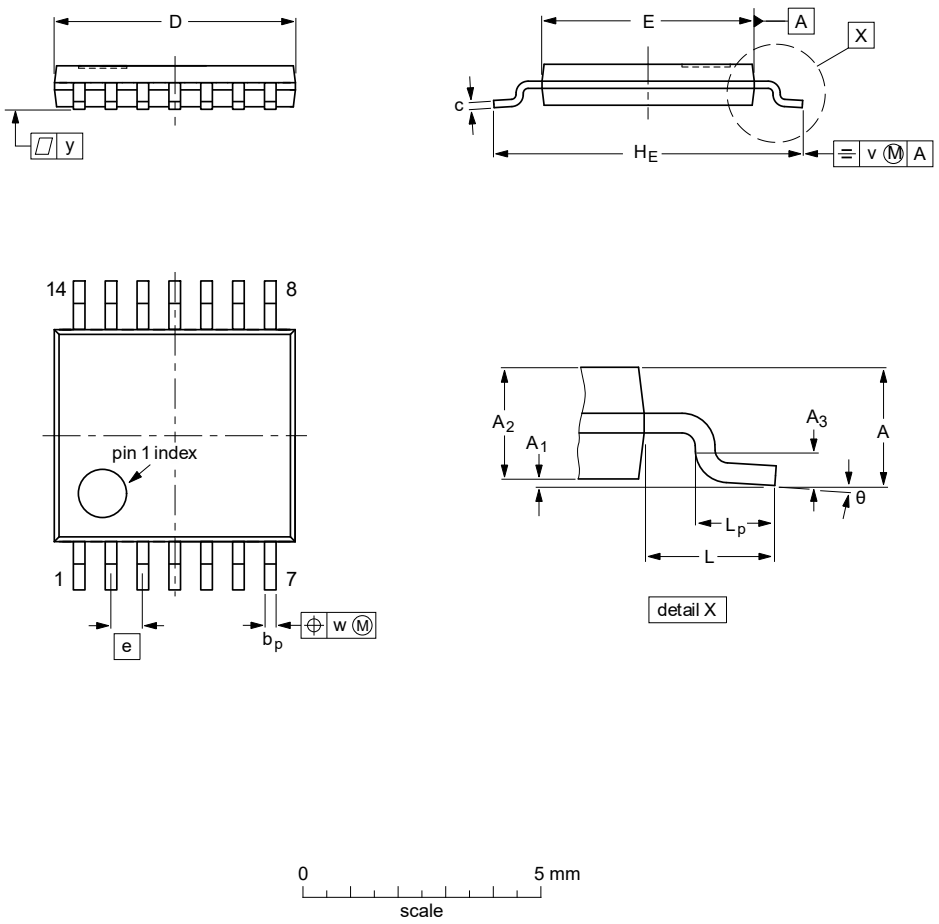
11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT402-1 (TSSOP14)

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12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC74_Q100 v.2	20240205	Product data sheet	-	74ALVC74_Q100 v.1
Modifications:	• Fig. 8: Aligned TSSOP package outline drawings to JEDEC MO-153.			
74ALVC74_Q100 v.1	20231018	Product data sheet	-	-

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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For more information, please visit: http://www.nexperia.com
For sales office addresses, please send an email to: salesaddresses@nexperia.com
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