



74ALVCH16501

18-bit universal bus transceiver; 3-state

Rev. 8 — 1 July 2024

Product data sheet

1. General description

The 74ALVCH16501 is an 18-bit universal transceiver with bus hold inputs and 3-state outputs. Data flow in each direction is controlled by output enable (OEAB and OEBA), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CPAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CPAB. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state. Data flow for B-to-A is similar to that of A-to-B but uses OEBA, LEBA and CPBA. The output enables are complimentary (OEAB is active HIGH and OEBA is active LOW). This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power dissipation
- Direct interface with TTL levels
- Current drive ± 24 mA at $V_{CC} = 3.0$ V
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched or clocked mode
- Bus hold on all data inputs
- Output drive capability 50 Ω transmission lines at 85 °C
- 3-state non-inverting outputs for bus-oriented applications
- Latch-up performance exceeds 100 mA per JESD78 Class II.A
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16501DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4. Functional diagram

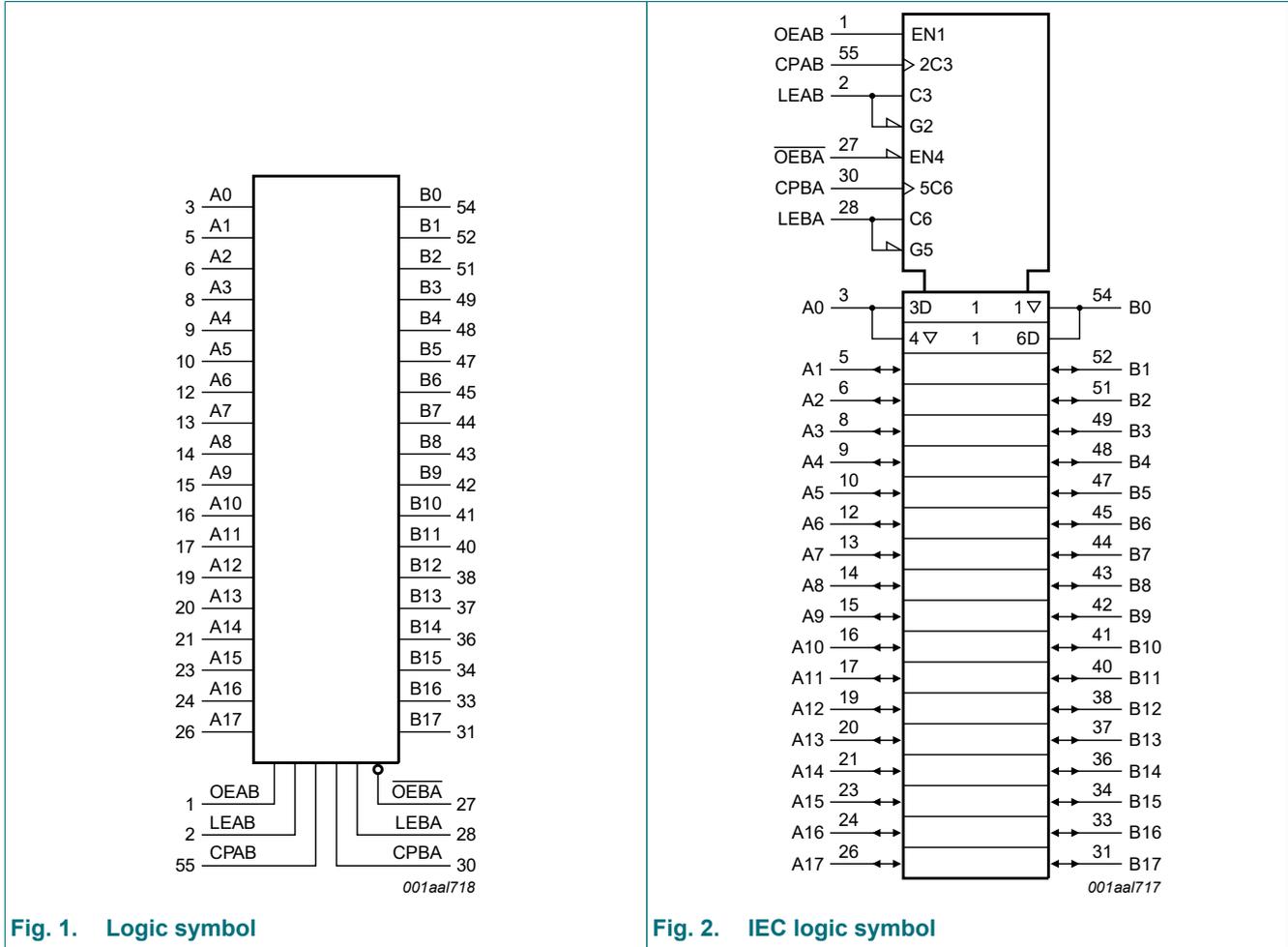


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

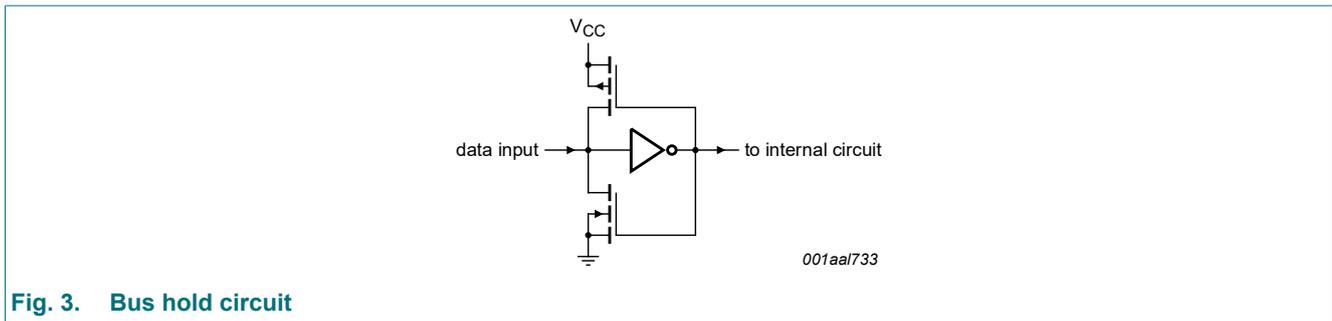


Fig. 3. Bus hold circuit

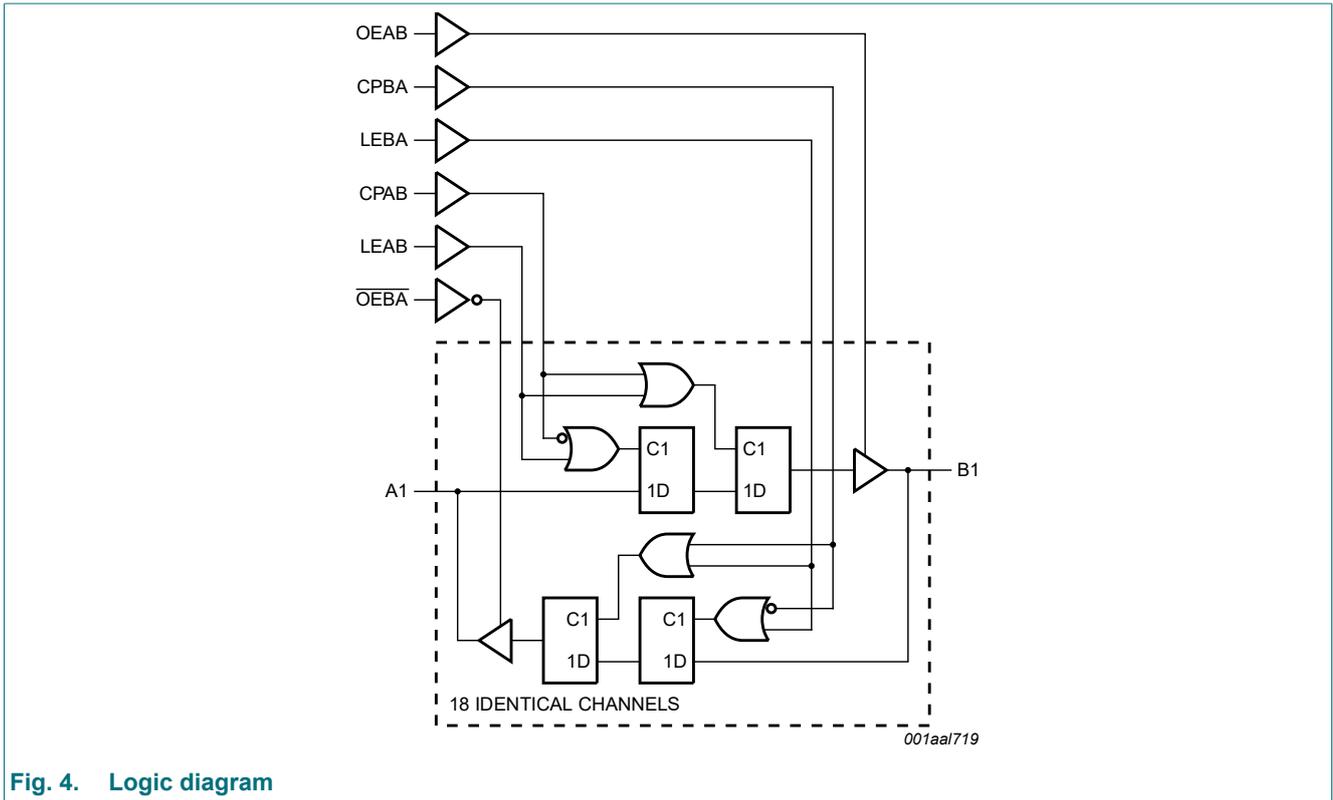
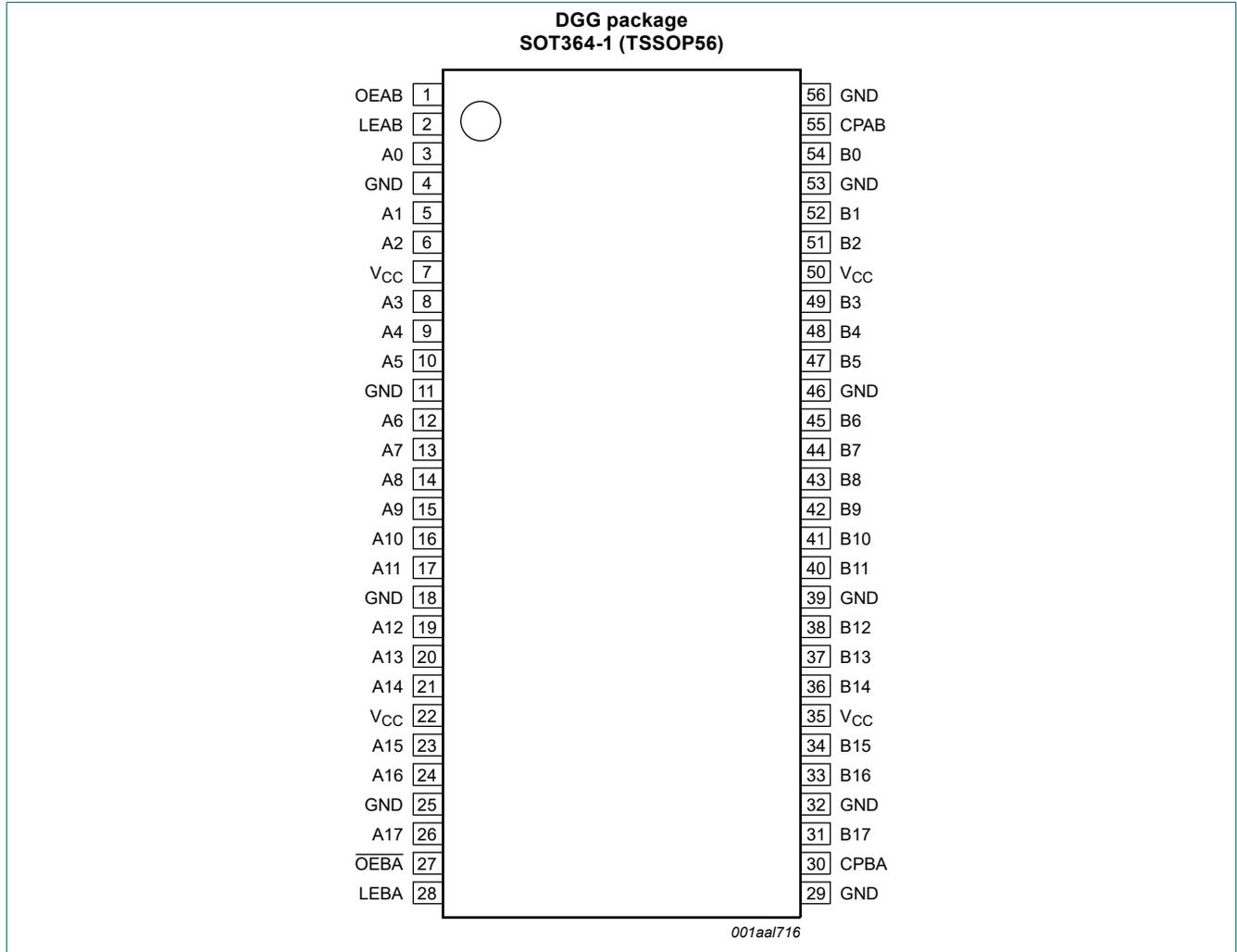


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
OEAB	1	output enable A-to-B input (active HIGH)
LEAB	2	latch enable A-to-B input
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17	3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	data inputs or outputs
GND	4, 11, 18, 25, 29, 32, 39, 46, 53, 56	ground (0 V)
V _{CC}	7, 22, 35, 50	positive supply voltage
\overline{OEBA}	27	output enable B-to-A (active LOW)
LEBA	28	latch enable B-to-A
CPBA	30	clock input B-to-A
B0, B1, B2, B3, B4, B5, B6, B7, B8 B9, B10, B11, B12, B13, B14, B15, B16, B17	54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs or outputs
CPAB	55	clock input A-to-B

6. Functional description

Table 3. Function table

A-to-B data flow is shown; B-to-A flow is similar but uses \overline{OEBA} , LEBA and CPBA.

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the enable or clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the enable or clock transition;

X = don't care; Z = high-impedance OFF-state;

↓ = HIGH-to-LOW clock transition; ↑ = LOW-to-HIGH clock transition.

Inputs				Output	Operating mode
OEAB	LEAB	CPAB	An	Bn	
L	X	X	X	Z	disabled
H	H	X	H	H	transparent
H	H	X	L	L	
H	↓	X	h	H	latch data and display
H	↓	X	l	L	
H	L	↑	h	H	clock data and display
H	L	↑	l	L	
H	L	H or L	X	H	hold data and display
H	L	H or L	X	L	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	control inputs [1]	-0.5	+4.6	V
		data inputs [1]	-0.5	$V_{CC} + 0.5$	V
V_O	output voltage	[1]	-0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance				
		$C_L = 30$ pF	2.3	-	2.7	V
		$C_L = 50$ pF	3.0	-	3.6	V
		low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	0	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7	1.2	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	-	1.2	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	1.5	0.8	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.3	V _{CC} - 0.08	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.26	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.14	-	V
		I _O = -12 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	V _{CC} - 0.09	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.28	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.07	0.40	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.15	0.70	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.14	0.40	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.27	0.55	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 2.3 V to 3.6 V	-	0.1	5	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 2.7 V to 3.6 V	-	0.1	10	µA
I _{CC}	supply current	V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.2	40	µA
ΔI _{CC}	additional supply current	per data I/O pin; V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	150	750	µA
I _{BHL}	bus hold LOW current	V _{CC} = 2.3 V; V _I = 0.7 V [2]	45	-	-	µA
		V _{CC} = 3.0 V; V _I = 0.8 V [2]	75	150	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 2.3 V; V _I = 1.7 V [2]	-45	-	-	µA
		V _{CC} = 3.0 V; V _I = 2.0 V [2]	-75	-175	-	µA
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 3.6 V [2]	500	-	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 3.6 V [2]	-500	-	-	µA
C _I	input capacitance		-	4.0	-	pF
C _{I/O}	input/output capacitance		-	8.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Valid for data inputs of bus hold parts only.

10. Dynamic characteristics

Table 7. Dynamic characteristics

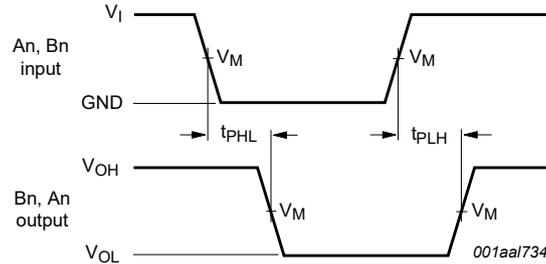
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
f _{max}	maximum frequency	see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V [2]	150	333	-	MHz
		V _{CC} = 3.0 V to 3.6 V [3]	150	340	-	MHz
		V _{CC} = 2.7 V	150	333	-	MHz
t _{pd}	propagation delay	An to Bn; Bn to An; see Fig. 5 [4]				
		V _{CC} = 2.3 V to 2.7 V [2]	1.0	2.8	5.1	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.0	3.0	4.2	ns
		V _{CC} = 2.7 V	-	3.0	4.6	ns
		LEAB, LEBA to Bn, An; see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V [2]	1.1	3.5	6.1	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.3	3.4	4.8	ns
		V _{CC} = 2.7 V	-	3.6	5.3	ns
		CPAB, CPBA to Bn, An; see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V [2]	1.0	3.3	6.1	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.4	3.3	4.9	ns
		V _{CC} = 2.7 V	-	3.4	5.6	ns
		t _{en}	enable time	OEBA to An; see Fig. 6 [4]		
V _{CC} = 2.3 V to 2.7 V [2]	1.3			2.8	6.3	ns
V _{CC} = 3.0 V to 3.6 V [3]	1.1			2.5	5.0	ns
V _{CC} = 2.7 V	-			3.3	6.0	ns
OEAB to Bn; see Fig. 6						
V _{CC} = 2.3 V to 2.7 V [2]	1.0			2.5	5.8	ns
V _{CC} = 3.0 V to 3.6 V [3]	1.0			2.4	4.6	ns
V _{CC} = 2.7 V	-			2.7	5.3	ns
t _{dis}	disable time	OEBA to An; see Fig. 6 [4]				
		V _{CC} = 2.3 V to 2.7 V [2]	1.3	2.5	5.3	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.3	3.1	4.2	ns
		V _{CC} = 2.7 V	-	3.3	4.6	ns
		OEAB to Bn; see Fig. 6				
		V _{CC} = 2.3 V to 2.7 V [2]	1.5	2.5	6.2	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.4	2.9	5.0	ns
		V _{CC} = 2.7 V	-	3.6	5.7	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t _w	pulse width	LEAB, LEBA HIGH; see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V [2]	3.3	0.8	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	3.3	0.9	-	ns
		V _{CC} = 2.7 V	3.3	0.7	-	ns
		CPAB, CPBA HIGH or LOW; see Fig. 7				
		V _{CC} = 2.3 V to 2.7 V [2]	3.3	2.0	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	3.3	1.1	-	ns
		V _{CC} = 2.7 V	3.3	1.4	-	ns
t _{su}	set-up time	An, Bn to CPAB, CPBA; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V [2]	1.7	0.1	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.3	-0.3	-	ns
		V _{CC} = 2.7 V	1.4	-0.1	-	ns
		An, Bn to LEAB, LEBA; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V [2]	1.1	0.1	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.0	0.3	-	ns
		V _{CC} = 2.7 V	1.0	-0.2	-	ns
t _h	hold time	An, Bn to CPAB, CPBA; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V [2]	1.7	0.3	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.3	0.4	-	ns
		V _{CC} = 2.7 V	1.6	0.3	-	ns
		An, Bn to LEAB, LEBA; see Fig. 8				
		V _{CC} = 2.3 V to 2.7 V [2]	1.6	0.3	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	1.2	0.1	-	ns
		V _{CC} = 2.7 V	1.5	0.1	-	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} [5]				
		outputs enabled	-	21	-	pF
		outputs disabled	-	3	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] Typical values are measured at V_{CC} = 2.5 V.
- [3] Typical values are measured at V_{CC} = 3.3 V.
- [4] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = total load switching outputs;
Σ(C_L × V_{CC}² × f_o) = sum of outputs.

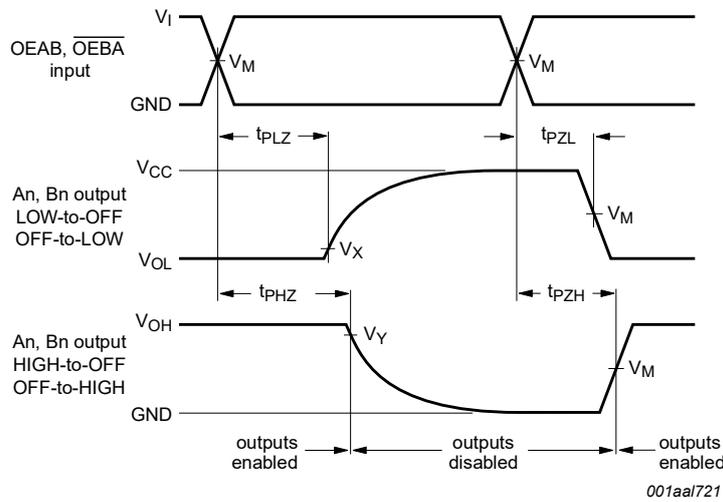
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output levels that occur with the output load.

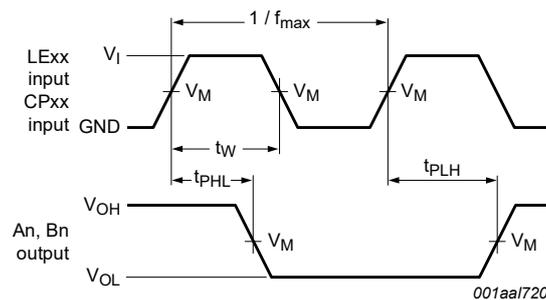
Fig. 5. Propagation delay, data input (An, Bn) to data output (Bn, An)



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output levels that occur with the output load.

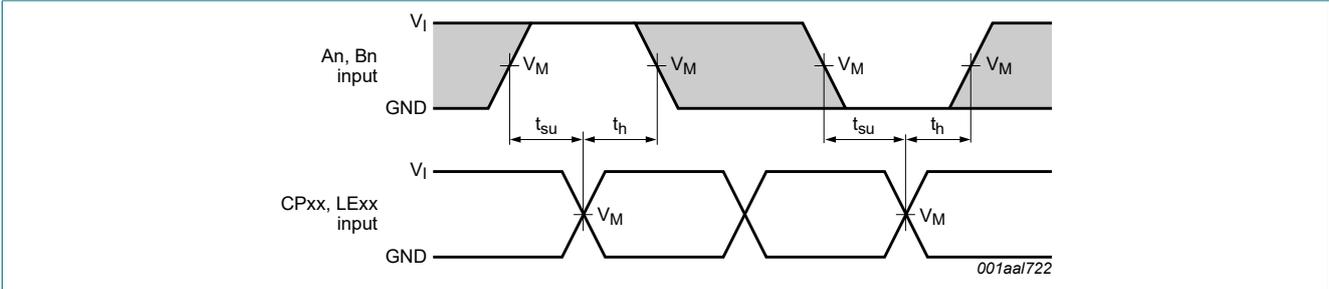
Fig. 6. 3-state output enable and disable times



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 7. Propagation delay, latch enable input (LEAB, LEBA) and clock pulse input (CPAB, CPBA) to data output, and pulse width

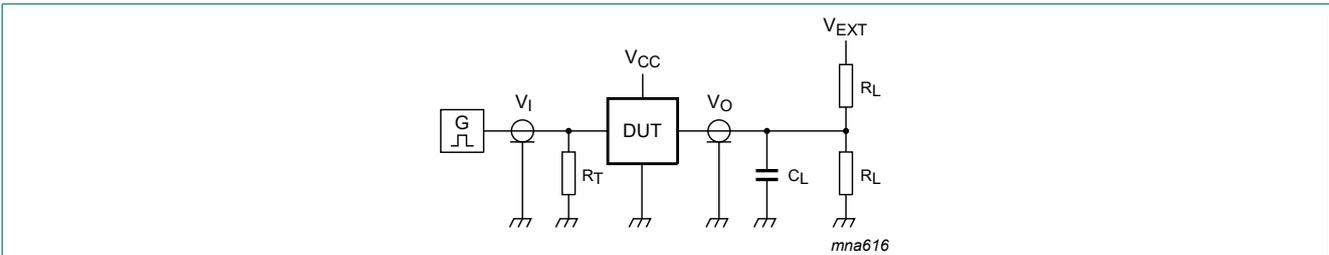


Measurement points are given in [Table 8](#).

Fig. 8. Data set-up and hold times (An, Bn inputs to LEAB, LEBA, CPAB and CPBA inputs)

Table 8. Measurement points

Supply voltage	Input		Output		
V _{CC}	V _I	V _M	V _M	V _X	V _Y
1.2 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
1.8 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.3 V to 2.7 V	V _{CC}	0.5 × V _{CC}	0.5 × V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V _{OL} + 0.3 V	V _{OH} - 0.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance includes jig and probe capacitance;

R_T = Termination resistance should be equal to Z_o of pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
V _{CC}	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
1.8 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

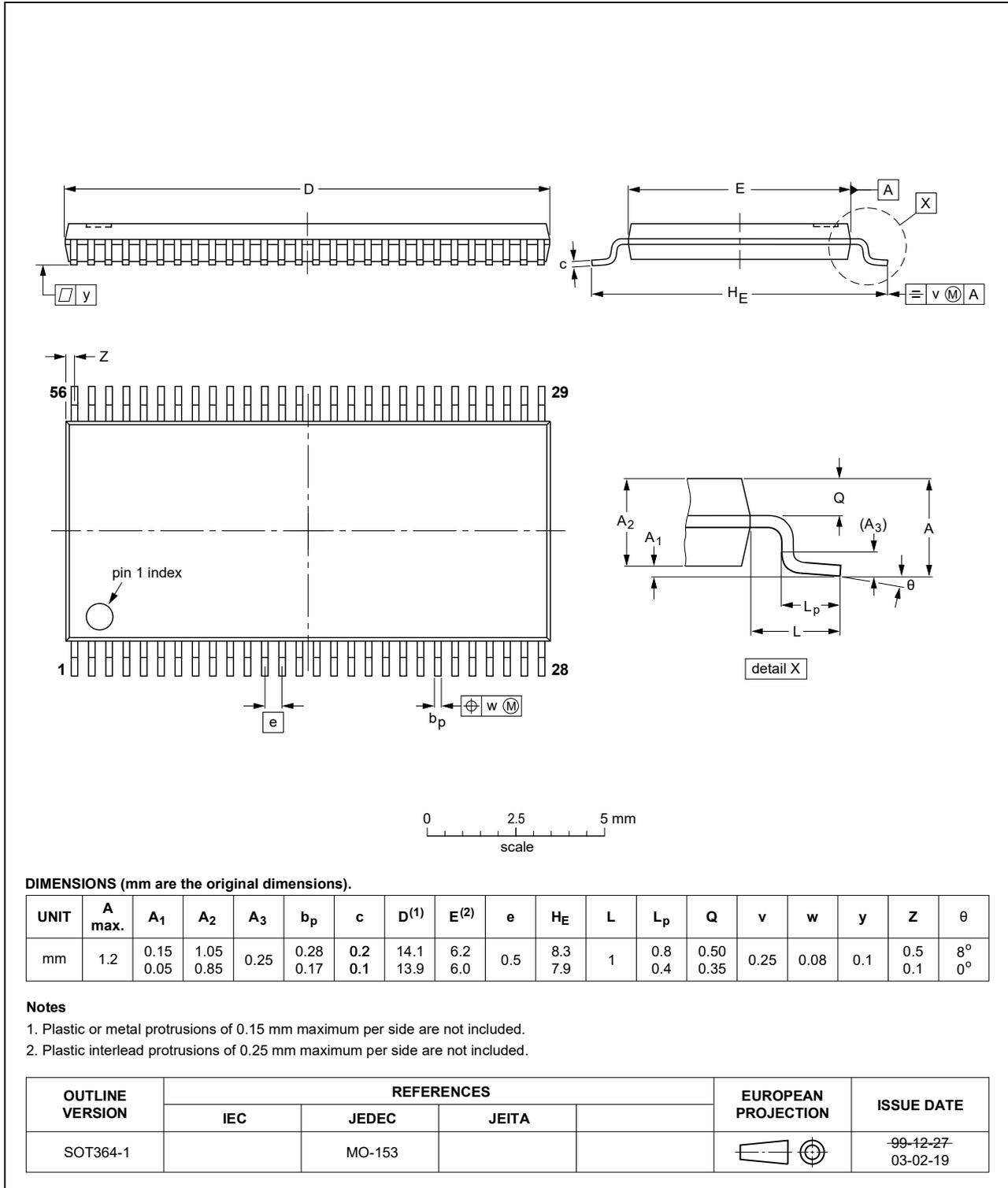


Fig. 10. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16501 v.8	20240701	Product data sheet	-	74ALVCH16501 v.7
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74ALVCH16501 v.7	20211124	Product data sheet	-	74ALVCH16501 v.6
Modifications:	<ul style="list-style-type: none"> Section 1 and Section 2 updated. Errata corrected in Table 4. 			
74ALVCH16501 v.6	20190313	Product data sheet	-	74ALVCH16501 v.5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type numbers 74ALVCH16501DL (SOT371-1) removed. 			
74ALVCH16501 v.5	20120710	Product data sheet	-	74ALVCH16501 v.4
Modifications:	<ul style="list-style-type: none"> Table 8 corrected (errata). 			
74ALVCH16501 v.4	20111117	Product data sheet	-	74ALVCH16501 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74ALVCH16501 v.3	20100402	Product data sheet	-	74ALVCH16501 v.2
74ALVCH16501 v.2	19980929	Product specification	-	74ALVCH16501 v.1
74ALVCH16501 v.1	19980929	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 1 July 2024
