

16-bit registered transceiver; 3-state

Rev. 4 — 10 July 2024

1. General description

The 74ALVCH16952 consists of two sections, each containing a dual octal non-inverting registered transceiver. Two 8-bit back to back registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the clock (nCPAB and nCPBA) provided that the clock enable (nCEAB and nCEBA) is LOW. The data is then present at the output buffers, but is only accessible when the output enable input (nOEAB and nOEBA) is LOW. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

2. Features and benefits

- CMOS low-power consumption
- MULTIBYTE[™] flow-through pinout architecture
- Low inductance, multiple center power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 85 °C
- Complies with JEDEC standard JESD8-B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

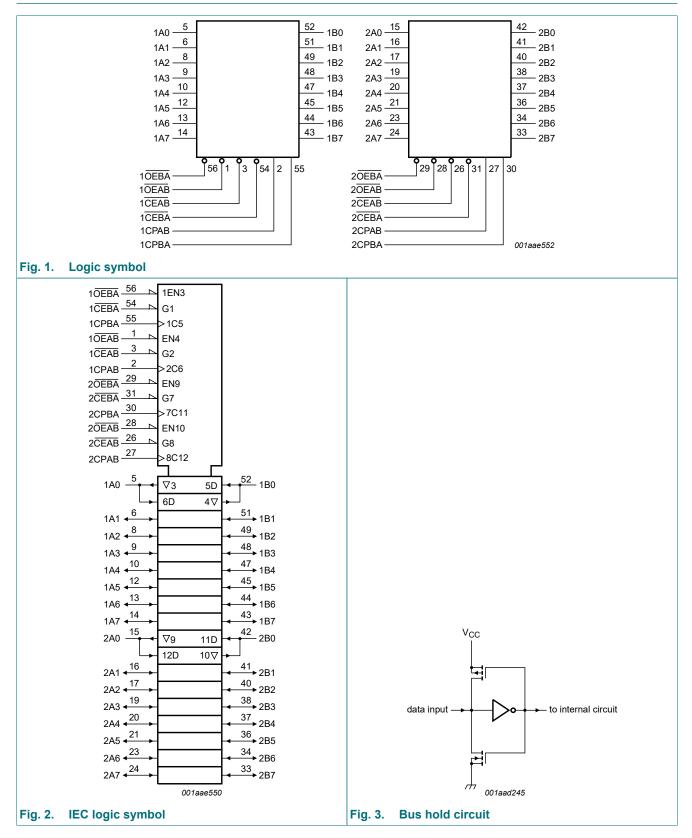
3. Ordering information

Table 1. Ordering information

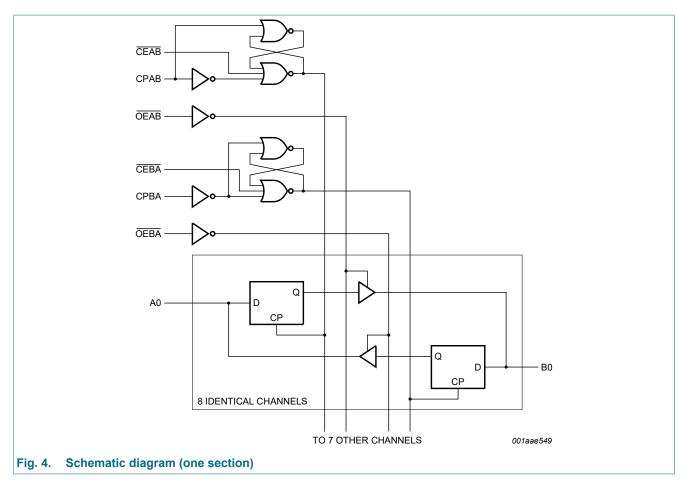
| Type number | Package | ackage | | | | | | | |
|-----------------|-------------------|---------|---|-----------------|--|--|--|--|--|
| | Temperature range | Name | Description | Version | | | | | |
| 74ALVCH16952DGG | -40 °C to +85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | <u>SOT364-1</u> | | | | | |



4. Functional diagram

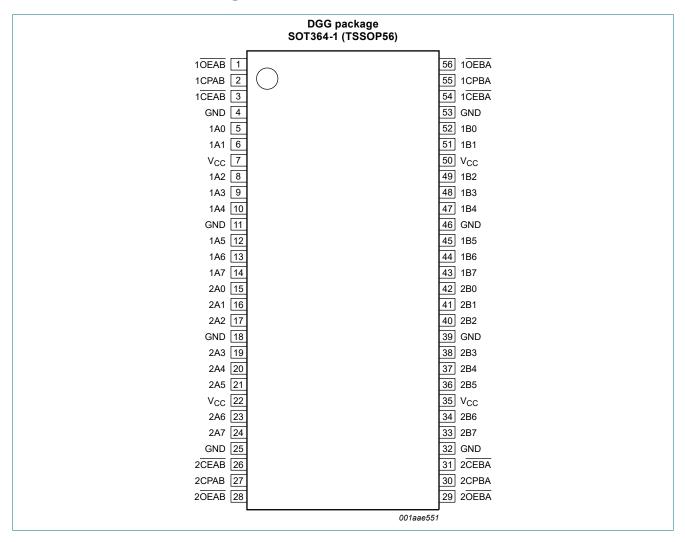


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5. Pinning information





Product data sheet

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5.2. Pin description

| Symbol | Pin | Description |
|--|--------------------------------|--|
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 5, 6, 8, 9, 10, 12, 13, 14 | data inputs or outputs |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 52, 51, 49, 48, 47, 45, 44, 43 | data inputs or outputs |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 15, 16, 17, 19, 20, 21, 23, 24 | data inputs or outputs |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 42, 41, 40, 38, 37, 36, 34, 33 | data inputs or outputs |
| 10EAB, 10EBA, 20EAB, 20EBA | 1, 56, 28, 29 | output enable input (active LOW) |
| 1CEAB, 1CEBA, 2CEAB, 2CEBA | 3, 54, 26, 31 | clock enable input (active LOW) |
| 1CPAB, 1CPBA, 2CPAB, 2CPBA | 2, 55, 27, 30 | clock pulse input (LOW-to-HIGH, edge-triggered) |
| GND | 4, 11, 18, 25, 32, 39, 46, 53 | ground (0 V) |
| V _{CC} | 7, 22, 35, 50 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; $\uparrow = LOW$ -to-HIGH clock transition;

X = don't care; *Z* = high impedance OFF-state; NC = no change.

| Operating mode | Control | Control | | | | Output |
|------------------------|---------------------------|--------------|--------------|----------|-----|----------|
| A to B, B to A | nOEAB, nOEBA | nCEAB, nCEBA | nCPAB, nCPBA | nAn, nBn | nQn | nBn, nAn |
| Hold | L | Н | Х | Х | NC | NC |
| Load and output enable | d and output enable L L ↑ | | L | L | L | |
| | | | | Н | Н | Н |
| Load and output H L ↑ | 1 | L | L | Z | | |
| disable | | | | Н | Н | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | | Min | Мах | Unit |
|------------------|-------------------------|---|-----|------|-----------------------|------|
| V _{CC} | supply voltage | | | -0.5 | +4.6 | V |
| VI | input voltage | control pins | [1] | -0.5 | +4.6 | V |
| | | data inputs | [1] | -0.5 | V _{CC} + 0.5 | V |
| Vo | output voltage | | [1] | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | input clamping current | V ₁ < 0 V | | - | -50 | mA |
| I _{OK} | output clamping current | $V_{\rm O}$ > $V_{\rm CC}$ or $V_{\rm O}$ < 0 V | | - | ±50 | mA |
| lo | output current | $V_{O} = 0 V$ to V_{CC} | | - | ±50 | mA |
| I _{CC} | supply current | | | - | 100 | mA |
| I _{GND} | ground current | | | -100 | - | mA |
| T _{stg} | storage temperature | | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +85 °C | | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Тур | Мах | Unit |
|------------------|-------------------------------------|----------------------------------|-----|-----|-----------------|------|
| V _{CC} | supply voltage | maximum speed performance | | | | |
| | | C _L = 30 pF | 2.3 | - | 2.7 | V |
| | | C _L = 50 pF | 3.0 | - | 3.6 | V |
| VI | input voltage | | 0 | - | V _{CC} | V |
| Vo | output voltage | | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | operating in free-air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.3 V to 3.0 V | 0 | - | 20 | ns/V |
| | | V _{CC} = 3.0 V to 3.6 V | 0 | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | |
|------------------|-----------------------------|---|-----------------------|------------------------|------|----|
| | | | Min | Тур [1] | Мах | |
| V _{IH} | HIGH-level input | V _{CC} = 2.3 V to 2.7 V | 1.7 | 1.2 | - | V |
| | voltage | V _{CC} = 2.7 V to 3.6 V | 2.0 | 1.5 | - | V |
| V _{IL} | LOW-level input | V _{CC} = 2.3 V to 2.7 V | - | 1.2 | 0.7 | V |
| | voltage | V _{CC} = 2.7 V to 3.6 V | - | 1.5 | 0.8 | V |
| V _{OH} | HIGH-level output | $V_{I} = V_{IH} \text{ or } V_{IL}$ | | | | |
| | voltage | V_{CC} = 2.3 V to 3.6 V; I _O = -100 µA | V _{CC} - 0.2 | V _{CC} | - | V |
| | | V _{CC} = 2.3 V; I _O = -6 mA | V _{CC} - 0.3 | V _{CC} - 0.08 | - | V |
| | | V _{CC} = 2.3 V; I _O = -12 mA | V _{CC} - 0.6 | V _{CC} - 0.26 | - | V |
| | | V _{CC} = 2.7 V; I _O = -12 mA | V _{CC} - 0.5 | V _{CC} - 0.14 | - | V |
| | | V _{CC} = 3.0 V; I _O = -12 mA | V _{CC} - 0.6 | V _{CC} - 0.09 | - | V |
| | | V _{CC} = 3.0 V; I _O = -24 mA | V _{CC} - 1.0 | V _{CC} - 0.28 | - | V |
| V _{OL} | LOW-level output voltage | $V_{I} = V_{IH} \text{ or } V_{IL}$ | | | | |
| | | V_{CC} = 2.3 V to 3.6 V; I _O = 100 µA | - | GND | 0.20 | V |
| | | V _{CC} = 2.3 V; I _O = 6 mA | - | 0.07 | 0.40 | V |
| | | V _{CC} = 2.3 V; I _O = 12 mA | - | 0.15 | 0.70 | V |
| | | V _{CC} = 2.7 V; I _O = 12 mA | - | 0.14 | 0.40 | V |
| | | V _{CC} = 3.0 V; I _O = 24 mA | - | 0.27 | 0.55 | V |
| lı | input leakage current | V _{CC} = 2.3 V to 3.6 V; V _I = V _{CC} or GND | - | 0.1 | 5 | μA |
| I _{OZ} | OFF-state output current | V_{CC} = 2.7 V to 3.6 V; V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND | - | 0.1 | 10 | μA |
| I _{CC} | supply current | $V_{CC} = 2.3 V \text{ to } 3.6 V;$ $V_I = V_{CC} \text{ or GND; } I_O = 0 \text{ A}$ | - | 0.2 | 40 | μA |
| ΔI _{CC} | additional supply current | V_{CC} = 2.3 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A | - | 150 | 750 | μA |
| I _{BHL} | bus hold LOW | V _{CC} = 2.3 V; V _I = 0.7 V | 45 | - | - | μA |
| | sustaining current | V _{CC} = 3.0 V; V _I = 0.8 V | 75 | 150 | - | μA |

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| Symbol | Parameter | r Conditions | | -40 °C to +85 °C | | | |
|-------------------|------------------------------------|---|------|------------------|-----|----|--|
| | | | Min | Тур [1] | Max | | |
| I _{BHH} | bus hold HIGH | V _{CC} = 2.3 V; V _I = 1.7 V | -45 | - | - | μA | |
| | sustaining current | V _{CC} = 3.0 V; V _I = 2.0 V | -75 | -175 | - | μA | |
| I _{BHLO} | bus hold LOW overdrive current | V _{CC} = 3.6 V | 500 | - | - | μA | |
| I _{BHHO} | bus hold HIGH overdrive current | V _{CC} = 3.6 V | -500 | - | - | μA | |
| Ci | input capacitance | | - | 3.0 | - | pF | |

[1] Typical values are measured at T_{amb} = 25 °C.

Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V. Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 8.

| Symbol | Parameter | Conditions | -4 | 0 °C to +85 | °C | Unit |
|------------------|-------------|--|-----|-------------|-----|------|
| | | | Min | Typ [1] | Мах | |
| t _{pd} | | nCPBA to nAn; nCPAB to nBn; see Fig. 5 [2 |] | | | |
| | delay | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.2 | 4.1 | ns |
| | | V _{CC} = 2.7 V | 1.0 | - | 4.6 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 3.2 | 3.9 | ns |
| t _{en} | enable time | nOEBA to nAn; nOEAB to nBn; see Fig. 7 [2 |] | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | - | 5.4 | ns |
| | | V _{CC} = 2.7 V | 1.0 | - | 5.3 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | - | 4.4 | ns |
| t _{dis} | disable | nOEBA to nAn; nOEAB to nBn; see Fig. 7 [2 |] | | | |
| | time | V _{CC} = 2.3 V to 2.7 V | 1.0 | - | 5.3 | ns |
| | | V _{CC} = 2.7 V | 1.4 | - | 4.4 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.1 | - | 4.0 | ns |
| t _w | pulse width | nCPAB; nCPBA; HIGH or LOW; see Fig. 5 | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 3.3 | - | - | ns |
| | | V _{CC} = 2.7 V | 3.3 | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 3.3 | - | - | ns |
| t _{su} | set-up time | nAn to nCPAB or nBn to nCPBA; see Fig. 6 | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | ns |
| | | V _{CC} = 2.7 V | 1.9 | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.5 | - | - | ns |
| | | nCEAB to nCPAB; nCEBA to nCPBA; see Fig. 6 | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.2 | - | - | ns |
| | | V _{CC} = 2.7 V | 1.0 | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | - | - | ns |

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| Symbol | Parameter | Conditions | -40 | °C to +85 | 5 °C | Unit |
|------------------|-------------------------------------|--|-----|-----------|------|------|
| | | | Min | Typ [1] | Max | |
| t _h | hold time | nAn to nCPAB or nBn to nCPBA; see Fig. 6 | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.6 | - | - | ns |
| | | V _{CC} = 2.7 V | 0.6 | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.8 | - | - | ns |
| | | nCEAB to nCPAB; nCEBA to nCPBA; see Fig. 6 | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.1 | - | - | ns |
| | | V _{CC} = 2.7 V | 0.9 | - | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.1 | - | - | ns |
| f _{max} | maximum | CP; see Fig. 5 | | | | |
| | frequency | V _{CC} = 2.3 V to 2.7 V | 150 | 350 | - | MHz |
| | | V _{CC} = 2.7 V | 150 | 350 | - | MHz |
| | | V _{CC} = 3.0 V to 3.6 V | 150 | 350 | - | MHz |
| C _{PD} | power dissipation capacitance | per driver; $V_I = GND$ to V_{CC} [3] | - | 30 | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C.

Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.

Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

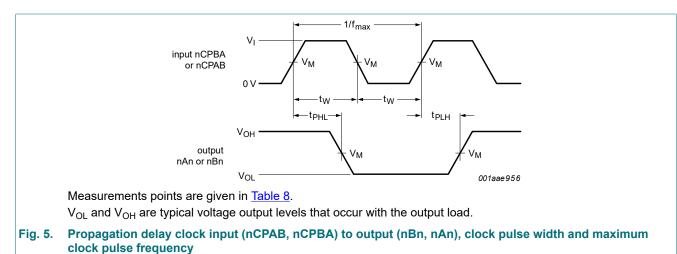
[2] t_{pd} is the same as t_{PHL} and t_{PLH} ; t_{en} is the same as t_{PZH} and t_{PZL} ; t_{dis} is the same as t_{PHZ} and t_{PLZ} . [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

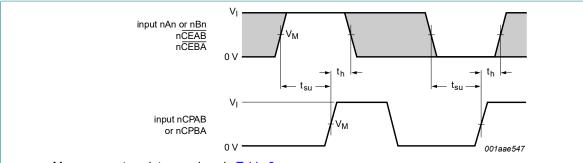
 f_i = input frequency in MHz; f_o = output frequency in MHz;

 C_L = output load capacitance in pF; V_{CC} = supply voltage in V; N = number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit



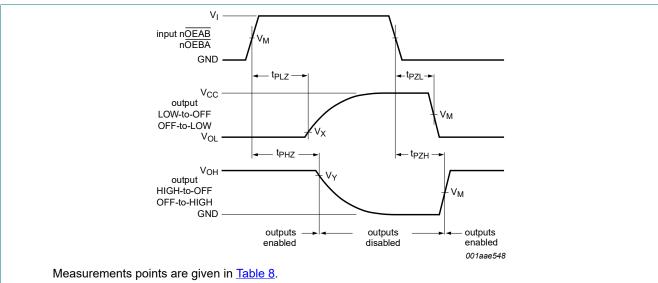
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Measurements points are given in <u>Table 8</u>.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6. Setup and hold times



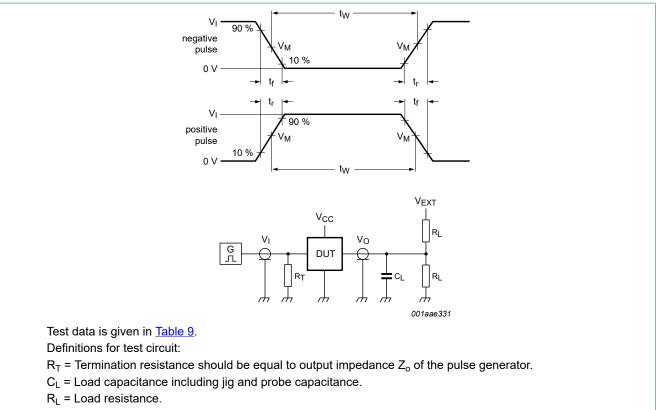
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. 3-state enable and disable time

Table 8. Measurement points

| Supply voltage | Input | nput l | | Output | | | |
|-----------------|-----------------|----------------|----------------|--------------------------|--------------------------|--|--|
| V _{cc} | VI | V _M | V _M | Vx | V _Y | | |
| 2.3 V to 2.7 V | V _{CC} | 0.5 V | 0.5 V | V _{OL} + 0.15 V | V _{OH} - 0.15 V | | |
| 2.7 V | 2.7 V | 1.5 V | 1.5 V | V _{OL} + 0.3 V | V _{OH} - 0.3 V | | |
| 3.0 V to 3.6 V | 2.7 V | 1.5 V | 1.5 V | V _{OL} + 0.3 V | V _{OH} - 0.3 V | | |

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V_{EXT} = External voltage for measuring switching times.

Fig. 8. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | Input | | Load | | V _{EXT} | | |
|-----------------|-----------------|---------------------------------|-------|-------|-------------------------------------|-------------------------------------|-------------------------------------|--|
| V _{cc} | VI | t _r , t _f | CL | RL | t _{PLH} , t _{PHL} | t _{PLZ} , t _{PZL} | t _{PHZ} , t _{PZH} | |
| 2.3 V to 2.7 V | V _{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND | |
| 2.7 V | 2.7 V | 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND | |
| 3.0 V to 3.6 V | 2.7 V | 2.5 ns | 50 pF | 500 Ω | open | $2 \times V_{CC}$ | GND | |

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11. Package outline

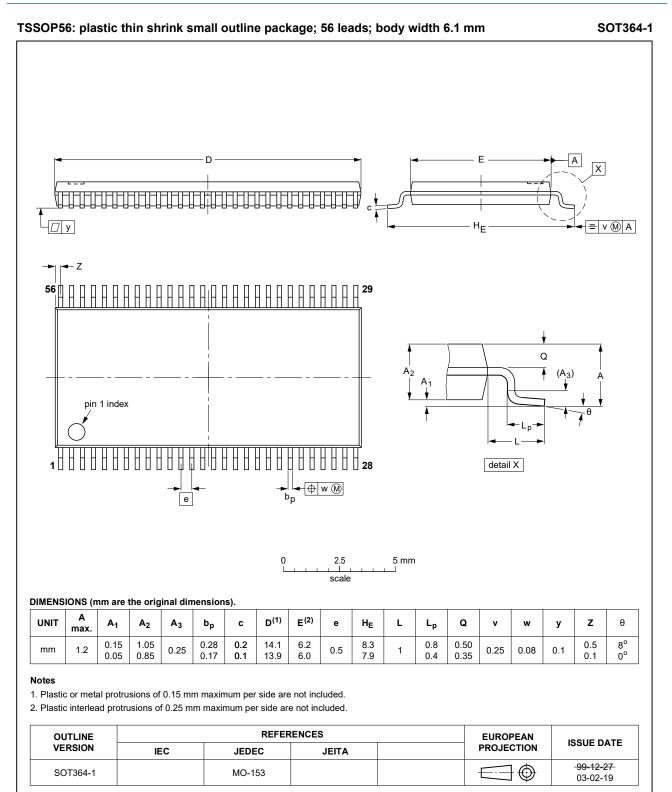


Fig. 9. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

| Table 10. Abbrev | Table 10. Abbreviations | | | | | |
|------------------|---|--|--|--|--|--|
| Acronym | Description | | | | | |
| ANSI | American National Standards Institute | | | | | |
| CDM | Charged Device Model | | | | | |
| CMOS | Complementary Metal-Oxide Semiconductor | | | | | |
| DUT | Device Under Test | | | | | |
| ESD | ElectroStatic Discharge | | | | | |
| ESDA | ElectroStatic Discharge Association | | | | | |
| НВМ | Human Body Model | | | | | |
| JEDEC | Joint Electron Device Engineering Council | | | | | |
| TTL | Transistor-Transistor Logic | | | | | |

13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes | |
|------------------|--|---------------------------|---------------|------------------|--|
| 74ALVCH16952 v.4 | 20240710 | Product data sheet | - | 74ALVCH16952 v.3 | |
| Modifications: | <u>Section 2</u>: ESD specification updated according to the latest JEDEC standard. <u>Fig. 1</u>: corrected pinnumber for 2A5. <u>Table 4</u>: P_{tot} total power dissipation updated. | | | | |
| 74ALVCH16952 v.3 | 20180109 | Product data sheet | - | 74ALVCH16952 v.2 | |
| Modifications: | The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. | | | | |
| 74ALVCH16952 v.2 | 20060427 | Product data sheet | - | 74ALVCH16952 v.1 | |
| Modifications: | The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors The symbol of pin numbers 15, 16, 17, 19, 20, 21, 23 and 24 is rectified | | | | |
| 74ALVCH16952 v.1 | 19980901 | Preliminary specification | | | |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|-----------------------------------|-----------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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