



# 74AVCH20T245

20-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 7 — 25 June 2024

Product data sheet

## 1. General description

The 74AVCH20T245 is a 20-bit, dual supply transceiver that enables bi-directional voltage level translation. The device can be used as two 10-bit transceivers or as a single 20-bit transceiver. It features four 10-bit input-output ports (1An, 1Bn and 2An, 2Bn), two output enable inputs (nOE), two direction inputs (nDIR) and dual supplies ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  and  $V_{CC(B)}$  can be independently supplied at any voltage between 0.8 V and 3.6 V making the device suitable for bi-directional voltage level translation between any of the low voltage nodes: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V. The 1An and 2An ports, nOE and nDIR are referenced to  $V_{CC(A)}$ , the 1Bn and 2Bn ports are referenced to  $V_{CC(B)}$ . A HIGH on a 1DIR allows transmission from 1An to 1Bn and a LOW on 1DIR allows transmission from 1Bn to 1An. A HIGH on nOE causes the outputs to assume a HIGH impedance OFF-state.

The device is fully specified for partial power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either  $V_{CC(A)}$  or  $V_{CC(B)}$  are at GND level, all output ports will assume a high impedance OFF-state. The bus hold circuitry on the powered-up side always stays active.

The 74AVCH20T245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

## 2. Features and benefits

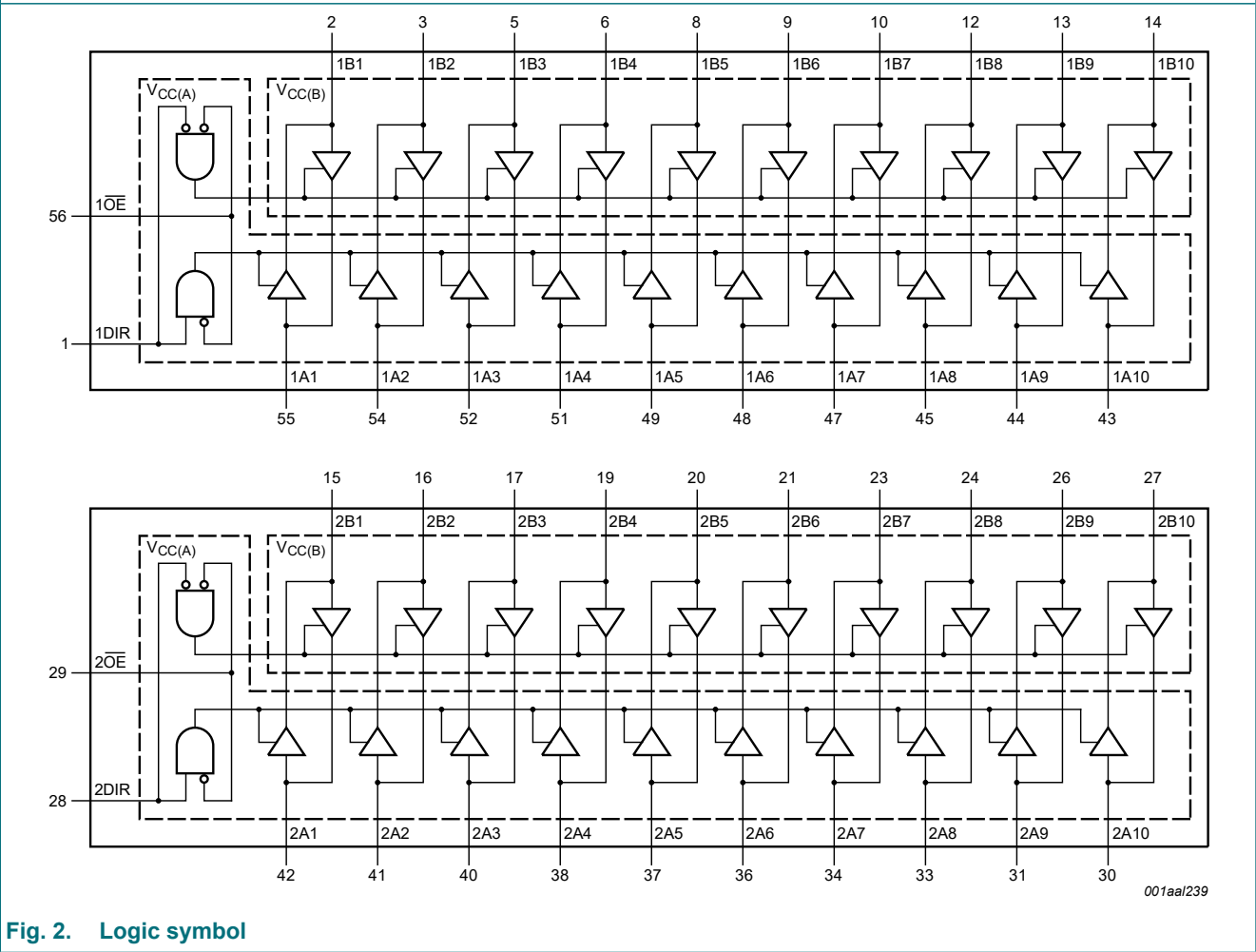
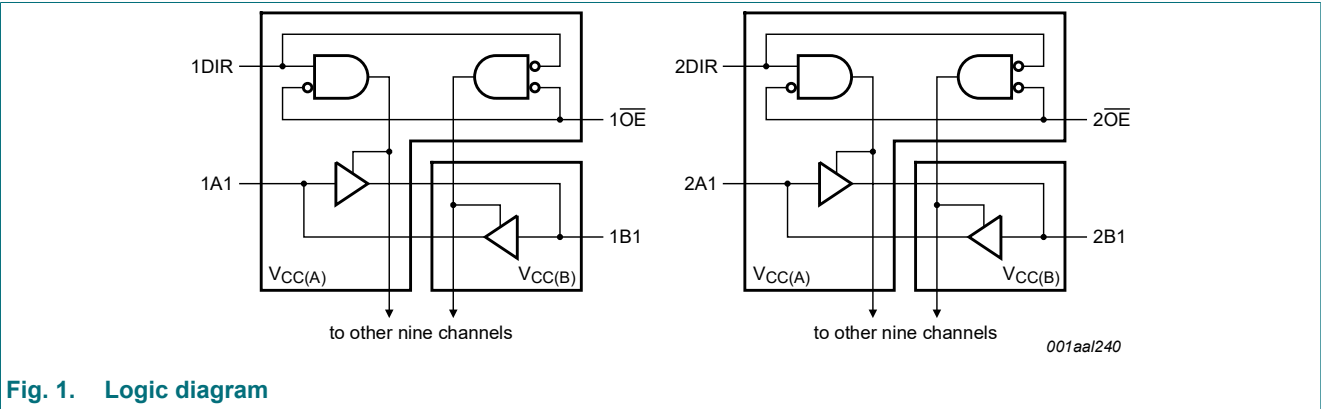
- Wide supply voltage range:  $V_{CC(A)}$ : 0.8 V to 3.6 V;  $V_{CC(B)}$ : 0.8 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- Maximum data rates:
  - 380 Mbit/s ( $\geq 1.8$  V to 3.3 V translation)
  - 260 Mbit/s ( $\geq 1.1$  V to 3.3 V translation)
  - 260 Mbit/s ( $\geq 1.1$  V to 2.5 V translation)
  - 210 Mbit/s ( $\geq 1.1$  V to 1.8 V translation)
  - 120 Mbit/s ( $\geq 1.1$  V to 1.5 V translation)
  - 100 Mbit/s ( $\geq 1.1$  V to 1.2 V translation)
- Suspend mode
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

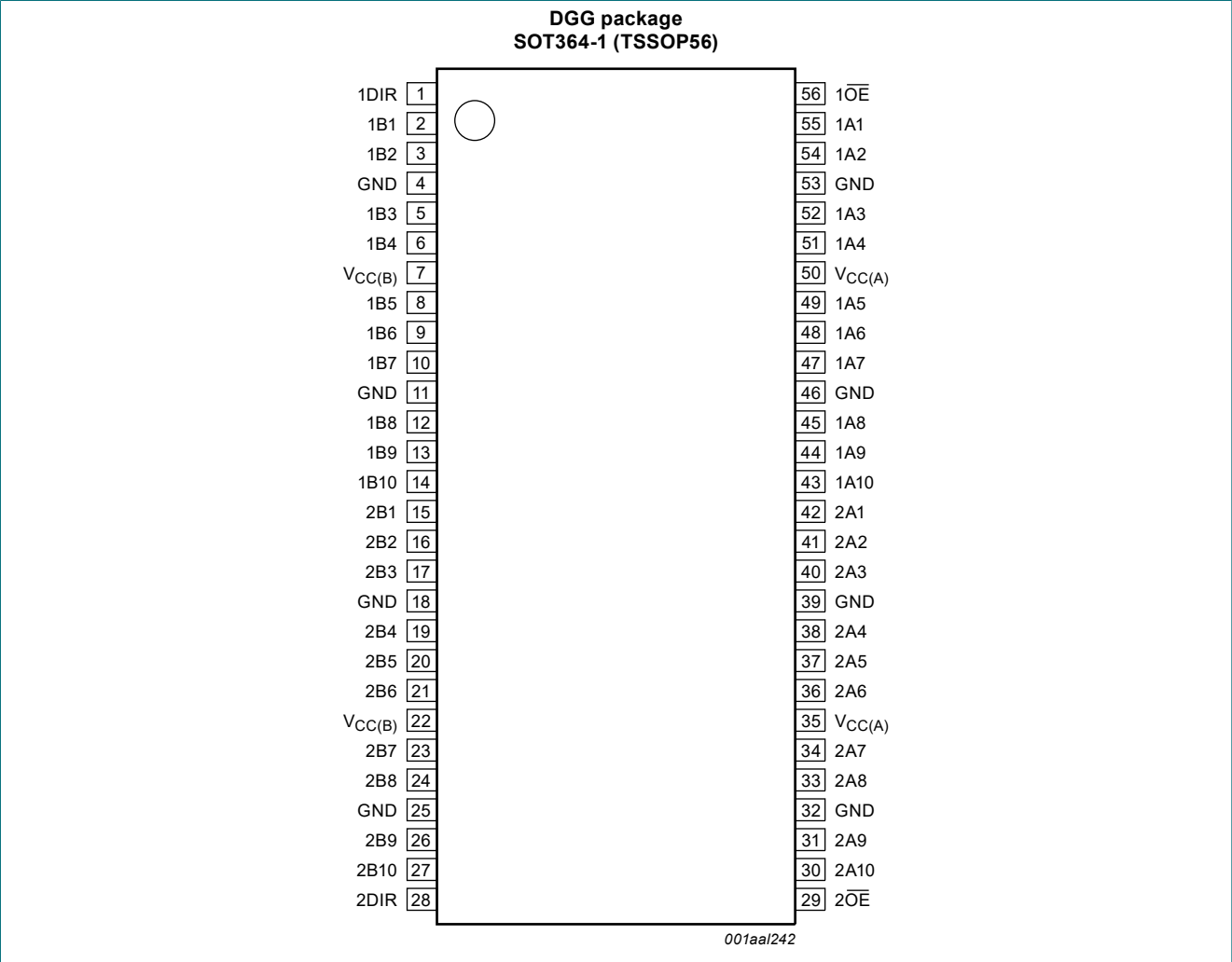
Type number	Package			
	Temperature range	Name	Description	Version
74AVCH20T245DGG	-40 °C to +125 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	<a href="#">SOT364-1</a>

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 28	direction control
1B1 to 1B10	2, 3, 5, 6, 8, 9, 10, 12, 13, 14	data input or output
2B1 to 2B10	15, 16, 17, 19, 20, 21, 23, 24,26, 27	data input or output
GND[1]	4, 11, 18, 25, 32, 39, 46, 53	ground (0 V)
V <sub>CC(B)</sub>	7, 22	supply voltage B (nBn inputs are referenced to V <sub>CC(B)</sub> )
1OE, 2OE	56, 29	output enable input (active LOW)
1A1 to 1A10	55, 54, 52, 51, 49, 48, 47, 45,44, 43	data input or output
2A1 to 2A10	42, 41, 40, 38, 37, 36, 34, 33,31, 30	data input or output
V <sub>CC(A)</sub>	35, 50	supply voltage A (nAn, nOE and nDIR inputs are referenced to V <sub>CC(A)</sub> )

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output [1]	
V <sub>CC(A)</sub> , V <sub>CC(B)</sub>	nOE [2]	nDIR [2]	nAn [2]	nBn [2]
0.8 V to 3.6 V	L	L	nAn = nBn	input
0.8 V to 3.6 V	L	H	input	nBn = nAn
0.8 V to 3.6 V	H	X	Z	Z
GND [1]	X	X	Z	Z

[1] If at least one of V<sub>CC(A)</sub> or V<sub>CC(B)</sub> is at GND level, the device goes into suspend mode.  
[2] The nAn, nDIR and nOE input circuit is referenced to V<sub>CC(A)</sub>; The nBn input circuit is referenced to V<sub>CC(B)</sub>.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC(A)</sub>	supply voltage A		-0.5	+4.6	V
V <sub>CC(B)</sub>	supply voltage B		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage	[1]	-0.5	+4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
V <sub>O</sub>	output voltage	Active mode [1] [2] [3]	-0.5	V <sub>CCO</sub> + 0.5	V
		Suspend or 3-state mode [1]	-0.5	+4.6	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CCO</sub> [2]	-	±50	mA
I <sub>CC</sub>	supply current	I <sub>CC(A)</sub> or I <sub>CC(B)</sub>	-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C [4]	-	500	mW

- [1] The minimum input and minimum output voltage ratings may be exceeded if the input and output clamping current ratings are observed.
- [2] V<sub>CCO</sub> is the supply voltage associated with the output port.
- [3] V<sub>CCO</sub> + 0.5 V should not exceed 4.6 V.
- [4] For SOT364-1 (TSSOP56) packages: P<sub>tot</sub> derates linearly with 12.2 mW/K above 109 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC(A)</sub>	supply voltage A		0.8	3.6	V
V <sub>CC(B)</sub>	supply voltage B		0.8	3.6	V
V <sub>I</sub>	input voltage		0	3.6	V
V <sub>O</sub>	output voltage	Active mode [1]	0	V <sub>CCO</sub>	V
		Suspend or 3-state mode	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CCI</sub> = 0.8 V to 3.6 V [2]	-	5	ns/V

- [1] V<sub>CCO</sub> is the supply voltage associated with the output port.
- [2] V<sub>CCI</sub> is the supply voltage associated with the input port.

## 9. Static characteristics

**Table 6. Typical static characteristics at  $T_{amb} = 25\text{ }^{\circ}\text{C}$**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = -1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.69	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O = 1.5\text{ mA}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$	-	0.07	-	V
$I_I$	input leakage current	nDIR, nOE input; $V_I = 0\text{ V}$ or $3.6\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.025$	$\pm 0.25$	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	A or B port; $V_I = 0.42\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ [3]	-	26	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	A or B port; $V_I = 0.78\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ [4]	-	-24	-	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ [5]	-	27	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)} = 1.2\text{ V}$ [6]	-	-26	-	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = V_{CC(B)} = 3.6\text{ V}$ [7]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode A port; $V_O = 0\text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ [7]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
		suspend mode B port; $V_O = 0\text{ V}$ or $V_{CCO}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 3.6\text{ V}$ [7]	-	$\pm 0.5$	$\pm 2.5$	$\mu\text{A}$
$I_{OFF}$	power-off leakage current	A port; $V_I$ or $V_O = 0\text{ V}$ to $3.6\text{ V}$ ; $V_{CC(A)} = 0\text{ V}$ ; $V_{CC(B)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
		B port; $V_I$ or $V_O = 0\text{ V}$ to $3.6\text{ V}$ ; $V_{CC(B)} = 0\text{ V}$ ; $V_{CC(A)} = 0.8\text{ V}$ to $3.6\text{ V}$	-	$\pm 0.1$	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	nDIR, nOE input; $V_I = 0\text{ V}$ or $3.3\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	2.0	-	pF
$C_{I/O}$	input/output capacitance	A and B port; $V_O = 3.3\text{ V}$ or $0\text{ V}$ ; $V_{CC(A)} = V_{CC(B)} = 3.3\text{ V}$	-	4.0	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output port.

[2]  $V_{CCI}$  is the supply voltage associated with the data input port.

[3] The bus hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_I$  to GND and then raising it to  $V_{IL}$  max.

[4] The bus hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_I$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

[5] An external driver must source at least  $I_{BHLO}$  to switch this node from LOW to HIGH.

[6] An external driver must sink at least  $I_{BHHO}$  to switch this node from HIGH to LOW.

[7] For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

20-bit dual supply translating transceiver with configurable voltage translation; 3-state

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).[1] [2]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	0.70V <sub>CCI</sub>	-	0.70V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	0.65V <sub>CCI</sub>	-	0.65V <sub>CCI</sub>	-	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	2	-	2	-	V
		nDIR, nOE input					
		V <sub>CC(A)</sub> = 0.8 V	0.70V <sub>CC(A)</sub>	-	0.70V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	0.65V <sub>CC(A)</sub>	-	0.65V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V <sub>CC(A)</sub> = 3.0 V to 3.6 V	2	-	2	-	V
V <sub>IL</sub>	LOW-level input voltage	data input					
		V <sub>CCI</sub> = 0.8 V	-	0.30V <sub>CCI</sub>	-	0.30V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CCI</sub>	-	0.35V <sub>CCI</sub>	V
		V <sub>CCI</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V <sub>CCI</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		nDIR, nOE input					
		V <sub>CC(A)</sub> = 0.8 V	-	0.30V <sub>CC(A)</sub>	-	0.30V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 1.1 V to 1.95 V	-	0.35V <sub>CC(A)</sub>	-	0.35V <sub>CC(A)</sub>	V
		V <sub>CC(A)</sub> = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V <sub>CC(A)</sub> = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -100 µA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	V <sub>CCO</sub> - 0.1	-	V <sub>CCO</sub> - 0.1	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	0.85	-	0.85	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	1.05	-	1.05	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	1.2	-	1.2	-	V
		I <sub>O</sub> = -9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	1.75	-	1.75	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	2.3	-	2.3	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 100 µA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	0.1	-	0.1	V
		I <sub>O</sub> = 3 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.1 V	-	0.25	-	0.25	V
		I <sub>O</sub> = 6 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-	0.35	-	0.35	V
		I <sub>O</sub> = 8 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-	0.45	-	0.45	V
		I <sub>O</sub> = 9 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-	0.55	-	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-	0.7	-	0.7	V
I <sub>I</sub>	input leakage current	nDIR, nOE input; V <sub>I</sub> = 0 V or 3.6 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±1	-	±5	µA

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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>BHL</sub>	bus hold LOW current	A or B port [3]					
		V <sub>I</sub> = 0.49 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	15	-	15	-	µA
		V <sub>I</sub> = 0.58 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	25	-	25	-	µA
		V <sub>I</sub> = 0.70 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	45	-	45	-	µA
		V <sub>I</sub> = 0.80 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	100	-	90	-	µA
I <sub>BHH</sub>	bus hold HIGH current	A or B port [4]					
		V <sub>I</sub> = 0.91 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.4 V	-15	-	-15	-	µA
		V <sub>I</sub> = 1.07 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.65 V	-25	-	-25	-	µA
		V <sub>I</sub> = 1.60 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.3 V	-45	-	-45	-	µA
		V <sub>I</sub> = 2.00 V; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.0 V	-100	-	-100	-	µA
I <sub>BHLO</sub>	bus hold LOW overdrive current	A or B port [5]					
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.6 V	125	-	125	-	µA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.95 V	200	-	200	-	µA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.7 V	300	-	300	-	µA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	500	-	500	-	µA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	A or B port [6]					
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.6 V	-125	-	-125	-	µA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 1.95 V	-200	-	-200	-	µA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 2.7 V	-300	-	-300	-	µA
		V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V	-500	-	-500	-	µA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = V <sub>CC(B)</sub> = 3.6 V [7]	-	±5	-	±30	µA
		suspend mode A port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V [7]	-	±5	-	±30	µA
		suspend mode B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V [7]	-	±5	-	±30	µA
I <sub>OFF</sub>	power-off leakage current	A port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	µA
		B port; V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC(B)</sub> = 0 V; V <sub>CC(A)</sub> = 0.8 V to 3.6 V	-	±5	-	±30	µA



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Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>CC</sub>	supply current	A port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	45	-	190	µA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	35	-	140	µA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	35	-	140	µA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-5	-	-20	-	µA
		B port; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A					
		V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	45	-	190	µA
		V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	35	-	140	µA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-5	-	-20	-	µA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 3.6 V	-	35	-	140	µA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 0.8 V to 3.6 V; V <sub>CC(B)</sub> = 0.8 V to 3.6 V	-	80	-	270	µA
		A plus B port (I <sub>CC(A)</sub> + I <sub>CC(B)</sub> ); I <sub>O</sub> = 0 A; V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; V <sub>CC(A)</sub> = 1.1 V to 3.6 V; V <sub>CC(B)</sub> = 1.1 V to 3.6 V	-	65	-	220	µA

- [1] V<sub>CCO</sub> is the supply voltage associated with the output port.
- [2] V<sub>CCI</sub> is the supply voltage associated with the data input port.
- [3] The bus hold circuit can sink at least the minimum low sustaining current at V<sub>IL</sub> max. I<sub>BHL</sub> should be measured after lowering V<sub>I</sub> to GND and then raising it to V<sub>IL</sub> max.
- [4] The bus hold circuit can source at least the minimum high sustaining current at V<sub>IH</sub> min. I<sub>BHH</sub> should be measured after raising V<sub>I</sub> to V<sub>CC</sub> and then lowering it to V<sub>IH</sub> min.
- [5] An external driver must source at least I<sub>BHLO</sub> to switch this node from LOW to HIGH.
- [6] An external driver must sink at least I<sub>BHHO</sub> to switch this node from HIGH to LOW.
- [7] For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

Table 8. Typical total supply current (I<sub>CC(A)</sub> + I<sub>CC(B)</sub>)

V <sub>CC(A)</sub>	V <sub>CC(B)</sub>							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	µA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	µA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	µA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	µA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	µA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	µA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	µA

## 10. Dynamic characteristics

**Table 9. Typical power dissipation capacitance at  $V_{CC(A)} = V_{CC(B)}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$** 

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$C_{PD}$	power dissipation capacitance	A port: (direction A to B); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction A to B); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		A port: (direction B to A); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		A port: (direction B to A); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction A to B); output enabled	9.5	9.7	9.8	9.9	10.7	11.9	pF
		B port: (direction A to B); output disabled	0.6	0.6	0.6	0.6	0.7	0.7	pF
		B port: (direction B to A); output enabled	0.2	0.2	0.2	0.2	0.3	0.4	pF
		B port: (direction B to A); output disabled	0.2	0.2	0.2	0.2	0.3	0.4	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

[2]  $f_i = 10\text{ MHz}$ ;  $V_i = \text{GND to } V_{CC}$ ;  $t_r = t_f = 1\text{ ns}$ ;  $C_L = 0\text{ pF}$ ;  $R_L = \infty\text{ }\Omega$ .

**Table 10. Typical dynamic characteristics at  $V_{CC(A)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$** 

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		nBn to nAn	14.4	12.4	12.1	11.9	11.8	11.8	ns
$t_{dis}$	disable time	n $\overline{\text{OE}}$ to nAn	16.2	16.2	16.2	16.2	16.2	16.2	ns
		n $\overline{\text{OE}}$ to nBn	17.6	10.0	9.0	9.1	8.7	9.3	ns
$t_{en}$	enable time	n $\overline{\text{OE}}$ to nAn	21.9	21.9	21.9	21.9	21.9	21.9	ns
		n $\overline{\text{OE}}$ to nBn	22.2	11.1	9.8	9.4	9.4	9.6	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

**Table 11. Typical dynamic characteristics at  $V_{CC(B)} = 0.8\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$** 

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
$t_{pd}$	propagation delay	nAn to nBn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		nBn to nAn	14.4	7.0	6.2	6.0	5.9	6.0	ns
$t_{dis}$	disable time	n $\overline{\text{OE}}$ to nAn	16.2	5.9	4.4	4.2	3.1	3.5	ns
		n $\overline{\text{OE}}$ to nBn	17.6	14.2	13.7	13.6	13.3	13.1	ns
$t_{en}$	enable time	n $\overline{\text{OE}}$ to nAn	21.9	6.4	4.4	3.5	2.6	2.3	ns
		n $\overline{\text{OE}}$ to nBn	22.2	17.7	17.2	17.0	16.8	16.7	ns

[1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ ;  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ ;  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

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Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C  
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>CC(A)</sub> = 1.1 V to 1.3 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.4	0.5	7.1	0.5	6.2	0.5	5.2	0.5	5.1	ns
		nBn to nAn	0.5	9.4	0.5	8.9	0.5	8.7	0.5	8.4	0.5	8.2	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	2.0	11.9	2.0	11.9	2.0	11.9	2.0	11.9	2.0	11.9	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.7	1.5	9.8	1.5	9.6	1.0	8.1	1.0	9.0	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.5	15.3	1.5	15.3	1.5	15.3	1.5	15.3	1.5	15.3	ns
		n $\overline{\text{OE}}$ to nBn	1.0	15.6	1.0	11.5	1.0	10.0	0.5	8.4	0.5	8.0	ns
V <sub>CC(A)</sub> = 1.4 V to 1.6 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.9	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	ns
		nBn to nAn	0.5	7.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	2.0	9.0	2.0	9.0	2.0	9.0	2.0	9.0	2.0	9.0	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.7	1.5	9.0	1.5	7.8	1.0	6.4	1.0	6.0	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.5	10.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.3	1.0	10.3	1.0	8.4	0.5	6.1	0.5	5.3	ns
V <sub>CC(A)</sub> = 1.65 V to 1.95 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.7	0.5	6.1	0.5	5.0	0.5	3.9	0.5	3.5	ns
		nBn to nAn	0.5	6.2	0.5	5.4	0.5	5.0	0.5	4.7	0.5	4.6	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	2.0	7.4	2.0	7.4	2.0	7.4	2.0	7.4	2.0	7.4	ns
		n $\overline{\text{OE}}$ to nBn	1.5	11.3	1.5	8.7	1.5	7.4	1.0	5.8	1.0	5.6	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	8.1	1.0	8.1	1.0	7.9	1.0	7.9	1.0	7.9	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.8	0.5	10.0	0.5	7.9	0.5	5.7	0.5	4.8	ns
V <sub>CC(A)</sub> = 2.3 V to 2.7 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.4	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3.0	ns
		nBn to nAn	0.5	5.2	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	ns
		n $\overline{\text{OE}}$ to nBn	1.2	10.8	1.2	8.2	1.2	6.9	1.0	5.3	1.0	5.2	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	5.4	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	ns
		n $\overline{\text{OE}}$ to nBn	0.5	13.3	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	ns
V <sub>CC(A)</sub> = 3.0 V to 3.6 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	8.2	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	ns
		nBn to nAn	0.5	5.1	0.5	3.9	0.5	3.5	0.5	3.0	0.5	2.9	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.8	5.0	0.8	5.0	0.8	5.0	0.8	5.0	0.8	5.0	ns
		n $\overline{\text{OE}}$ to nBn	1.2	10.5	1.2	8.1	1.2	6.7	1.0	5.1	0.8	5.0	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.4	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	ns
		n $\overline{\text{OE}}$ to nBn	1.0	13.1	1.0	9.6	0.5	7.5	0.5	5.1	0.5	4.1	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

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Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C  
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for wave forms see Fig. 3 and Fig. 4. [1]

Symbol	Parameter	Conditions	V <sub>CC(B)</sub>										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>CC(A)</sub> = 1.1 V to 1.3 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	10.4	0.5	7.9	0.5	6.9	0.5	5.8	0.5	5.7	ns
		nBn to nAn	0.5	10.4	0.5	9.8	0.5	9.6	0.5	9.3	0.5	9.1	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	2.0	13.1	2.0	13.1	2.0	13.1	2.0	13.1	2.0	13.1	ns
		n $\overline{\text{OE}}$ to nBn	1.5	14.0	1.5	10.8	1.5	10.6	1.0	9.0	1.0	9.9	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.5	16.9	1.5	16.9	1.5	16.9	1.5	16.9	1.5	16.9	ns
		n $\overline{\text{OE}}$ to nBn	1.0	17.2	1.0	12.7	1.0	11.0	0.5	9.3	0.5	8.8	ns
V <sub>CC(A)</sub> = 1.4 V to 1.6 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.8	0.5	7.1	0.5	6.0	0.5	4.8	0.5	4.3	ns
		nBn to nAn	0.5	7.9	0.5	7.1	0.5	6.8	0.5	6.4	0.5	6.3	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	2.0	9.9	2.0	9.9	2.0	9.9	2.0	9.9	2.0	9.9	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.9	1.5	9.9	1.5	8.6	1.0	7.1	1.0	6.6	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.5	11.4	1.5	11.4	1.5	11.4	1.5	11.3	1.5	11.3	ns
		n $\overline{\text{OE}}$ to nBn	1.0	15.8	1.0	11.4	1.0	9.3	0.5	6.8	0.5	5.9	ns
V <sub>CC(A)</sub> = 1.65 V to 1.95 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.6	0.5	6.8	0.5	5.5	0.5	4.3	0.5	3.9	ns
		nBn to nAn	0.5	6.9	0.5	6.0	0.5	5.5	0.5	5.2	0.5	5.1	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	2.0	8.2	2.0	8.2	2.0	8.2	2.0	8.2	2.0	8.2	ns
		n $\overline{\text{OE}}$ to nBn	1.5	12.5	1.5	9.6	1.5	8.2	1.0	6.4	1.0	6.2	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	1.0	9.0	1.0	9.0	1.0	8.7	1.0	8.7	1.0	8.7	ns
		n $\overline{\text{OE}}$ to nBn	0.5	15.2	0.5	11.0	0.5	8.7	0.5	6.3	0.5	5.3	ns
V <sub>CC(A)</sub> = 2.3 V to 2.7 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.3	0.5	6.4	0.5	5.2	0.5	3.9	0.5	3.3	ns
		nBn to nAn	0.5	5.8	0.5	4.8	0.5	4.3	0.5	3.9	0.5	3.8	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	1.1	5.8	1.1	5.8	1.1	5.8	1.1	5.8	1.1	5.8	ns
		n $\overline{\text{OE}}$ to nBn	1.2	11.9	1.2	9.1	1.2	7.6	1.0	5.9	1.0	5.8	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	6.0	0.5	6.0	0.5	5.9	0.5	5.8	0.5	5.8	ns
		n $\overline{\text{OE}}$ to nBn	0.5	14.7	0.5	10.6	0.5	8.4	0.5	5.9	0.5	4.8	ns
V <sub>CC(A)</sub> = 3.0 V to 3.6 V													
t <sub>pd</sub>	propagation delay	nAn to nBn	0.5	9.1	0.5	6.3	0.5	5.1	0.5	3.8	0.5	3.2	ns
		nBn to nAn	0.5	5.7	0.5	4.3	0.5	3.9	0.5	3.3	0.5	3.2	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nAn	0.8	5.5	0.8	5.5	0.8	5.5	0.8	5.5	0.8	5.5	ns
		n $\overline{\text{OE}}$ to nBn	1.2	11.6	1.2	9.0	1.2	7.4	1.0	5.7	0.8	5.5	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nAn	0.5	4.9	0.5	4.9	0.5	4.8	0.5	4.7	0.5	4.6	ns
		n $\overline{\text{OE}}$ to nBn	1.0	14.5	1.0	10.6	0.5	8.3	0.5	5.7	0.5	4.6	ns

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>; t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>; t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

10.1. Waveforms and test circuit

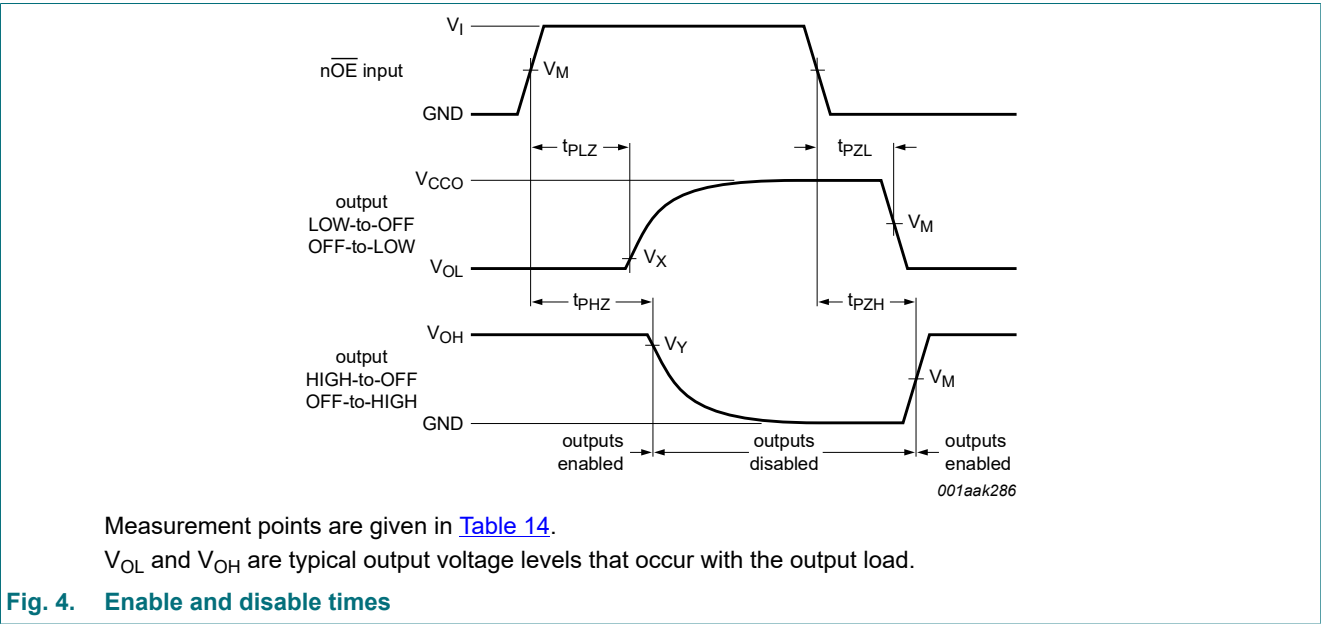
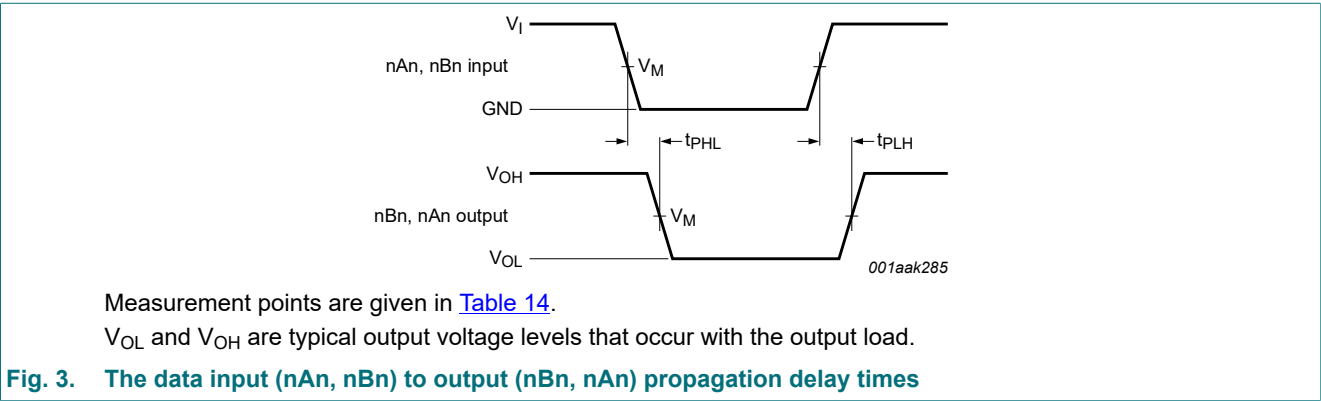


Table 14. Measurement points

Supply voltage	Input [1]	Output [2]		
$V_{CC(A)}, V_{CC(B)}$	$V_M$	$V_M$	$V_X$	$V_Y$
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.1\text{ V}$	$V_{OH} - 0.1\text{ V}$
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.15\text{ V}$	$V_{OH} - 0.15\text{ V}$
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
[2]  $V_{CCO}$  is the supply voltage associated with the output port.

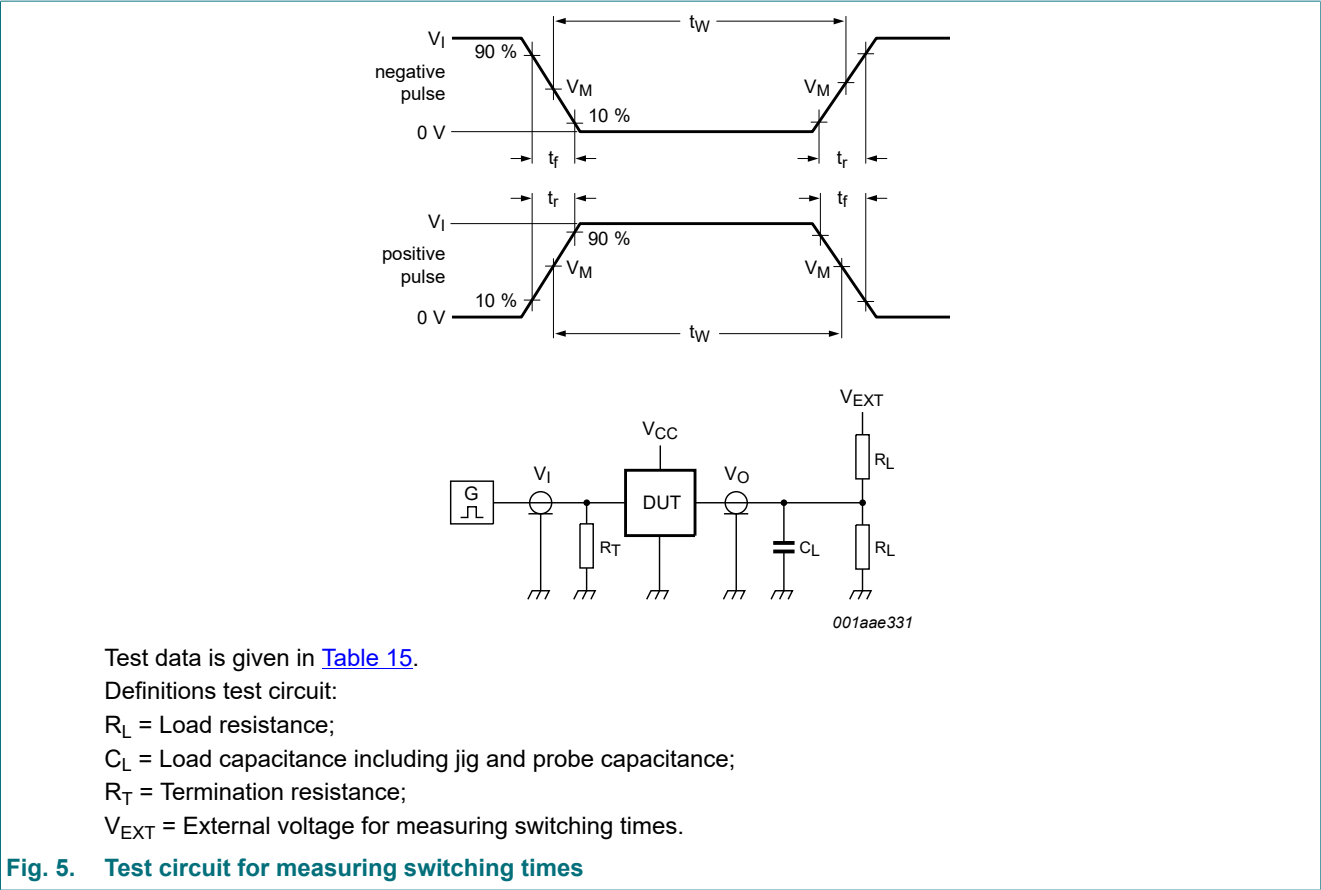


Table 15. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC(A)}, V_{CC(B)}$	$V_I$ [1]	$\Delta t/\Delta V$ [2]	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ [3]
0.8 V to 1.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	$V_{CCI}$	$\leq 1.0 \text{ ns/V}$	15 pF	2 k $\Omega$	open	GND	$2V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.  
[2]  $dV/dt \geq 1.0 \text{ V/ns}$   
[3]  $V_{CCO}$  is the supply voltage associated with the output port.

11. Typical propagation delay characteristics

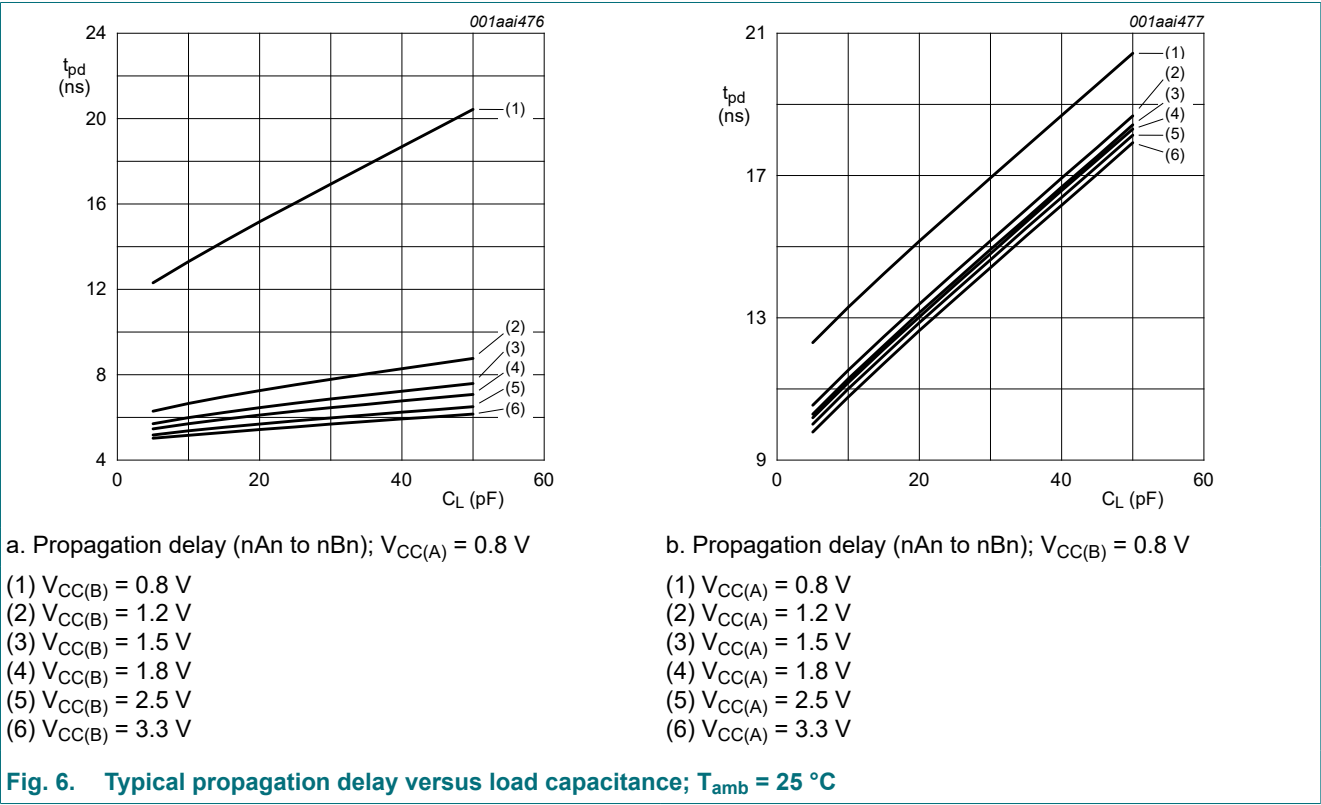
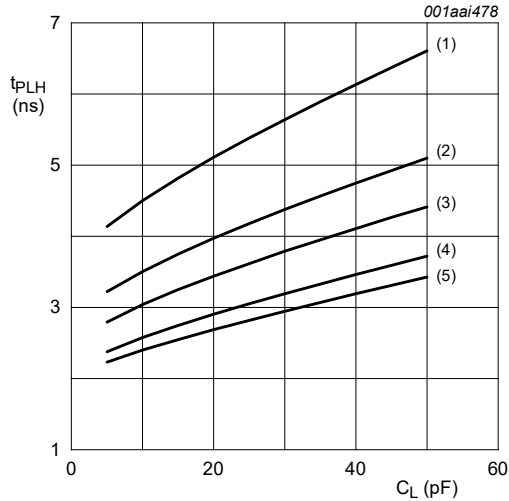
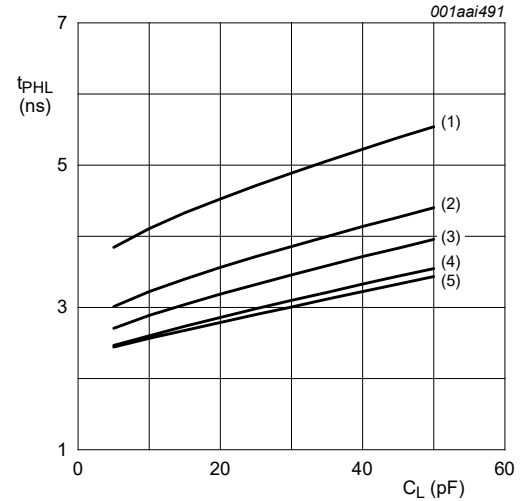


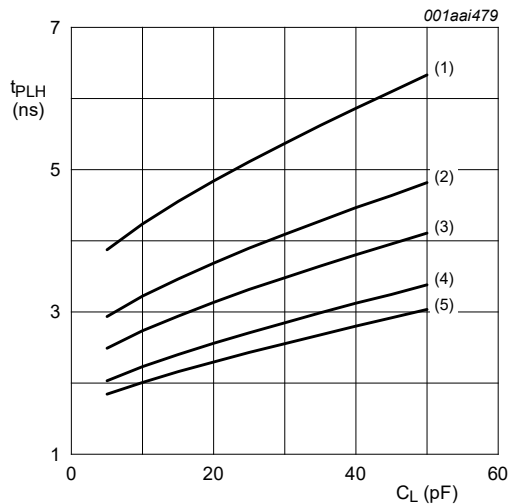
Fig. 6. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^{\circ}\text{C}$



a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.2 \text{ V}$

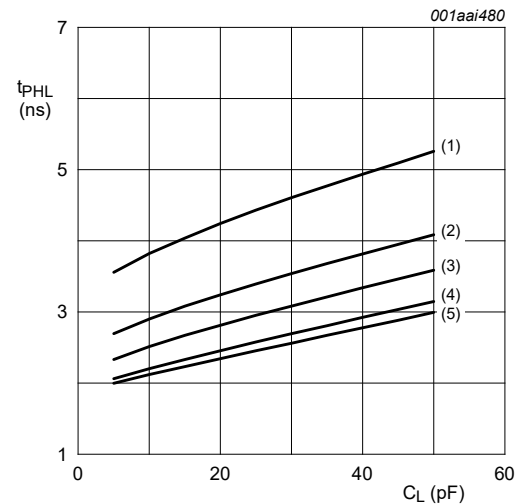


b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.2 \text{ V}$



c. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.5 \text{ V}$

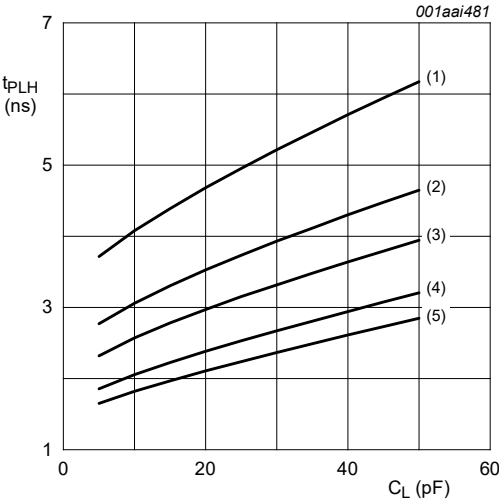
- (1)  $V_{CC(B)} = 1.2 \text{ V}$
- (2)  $V_{CC(B)} = 1.5 \text{ V}$
- (3)  $V_{CC(B)} = 1.8 \text{ V}$
- (4)  $V_{CC(B)} = 2.5 \text{ V}$
- (5)  $V_{CC(B)} = 3.3 \text{ V}$



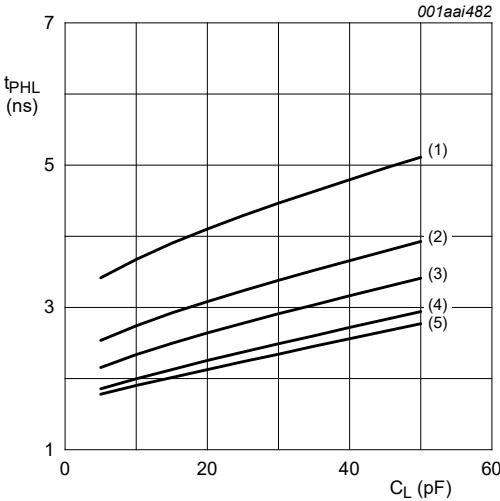
d. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.5 \text{ V}$

**Fig. 7. Typical propagation delay versus load capacitance;  $T_{amb} = 25^\circ\text{C}$**

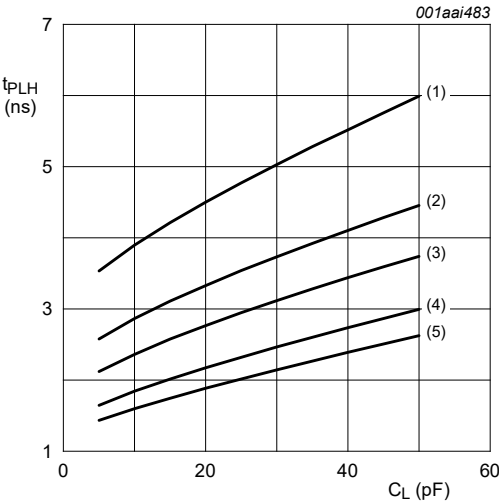




a. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.8\text{ V}$

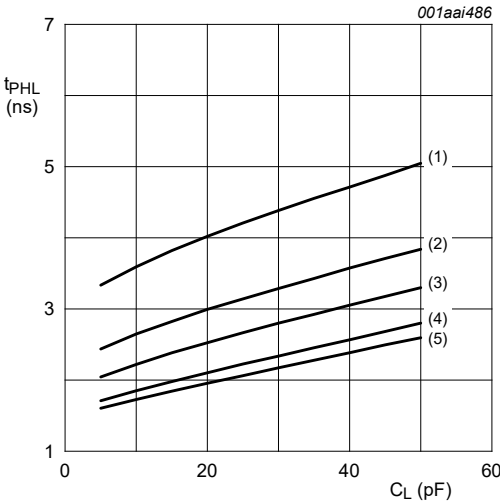


b. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 1.8\text{ V}$



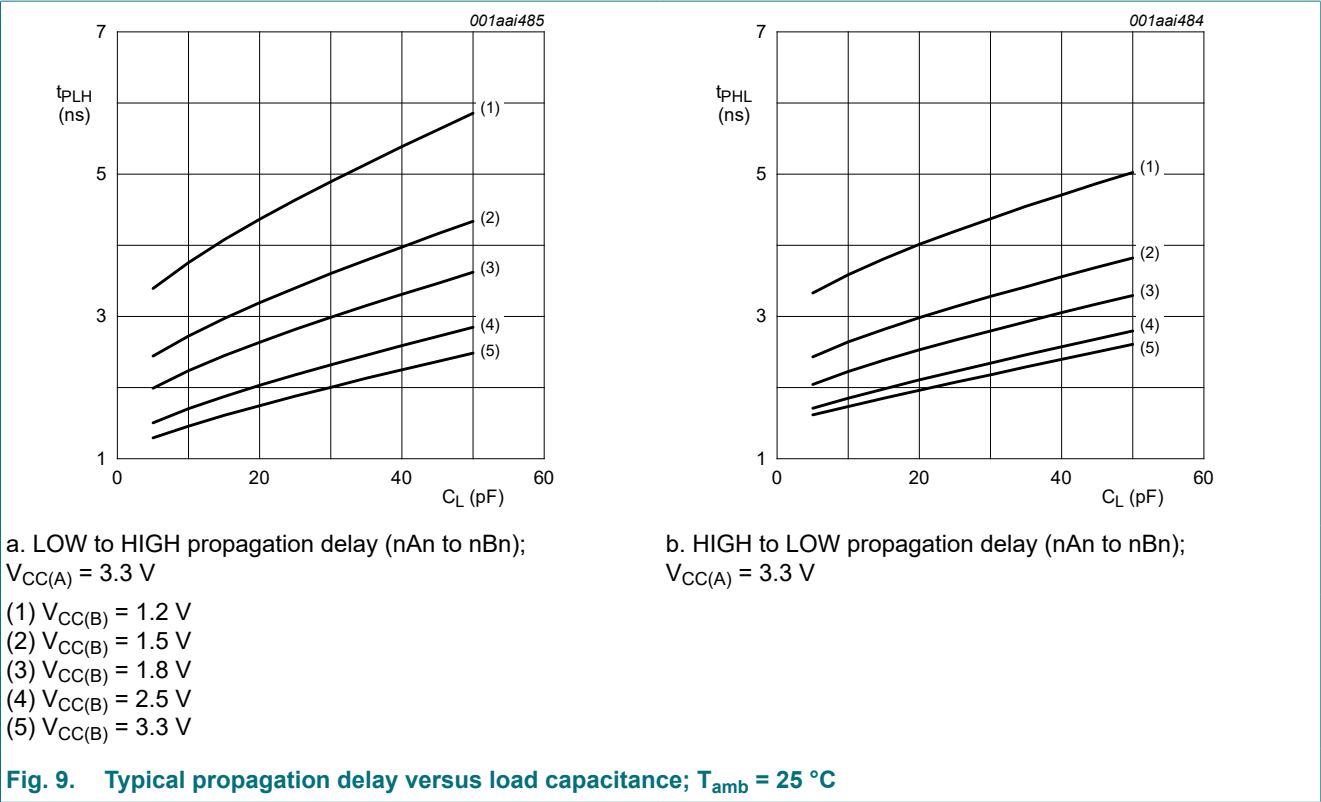
c. LOW to HIGH propagation delay (nAn to nBn);  
 $V_{CC(A)} = 2.5\text{ V}$

- (1)  $V_{CC(B)} = 1.2\text{ V}$
- (2)  $V_{CC(B)} = 1.5\text{ V}$
- (3)  $V_{CC(B)} = 1.8\text{ V}$
- (4)  $V_{CC(B)} = 2.5\text{ V}$
- (5)  $V_{CC(B)} = 3.3\text{ V}$



d. HIGH to LOW propagation delay (nAn to nBn);  
 $V_{CC(A)} = 2.5\text{ V}$

Fig. 8. Typical propagation delay versus load capacitance;  $T_{amb} = 25\text{ }^{\circ}\text{C}$



12. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

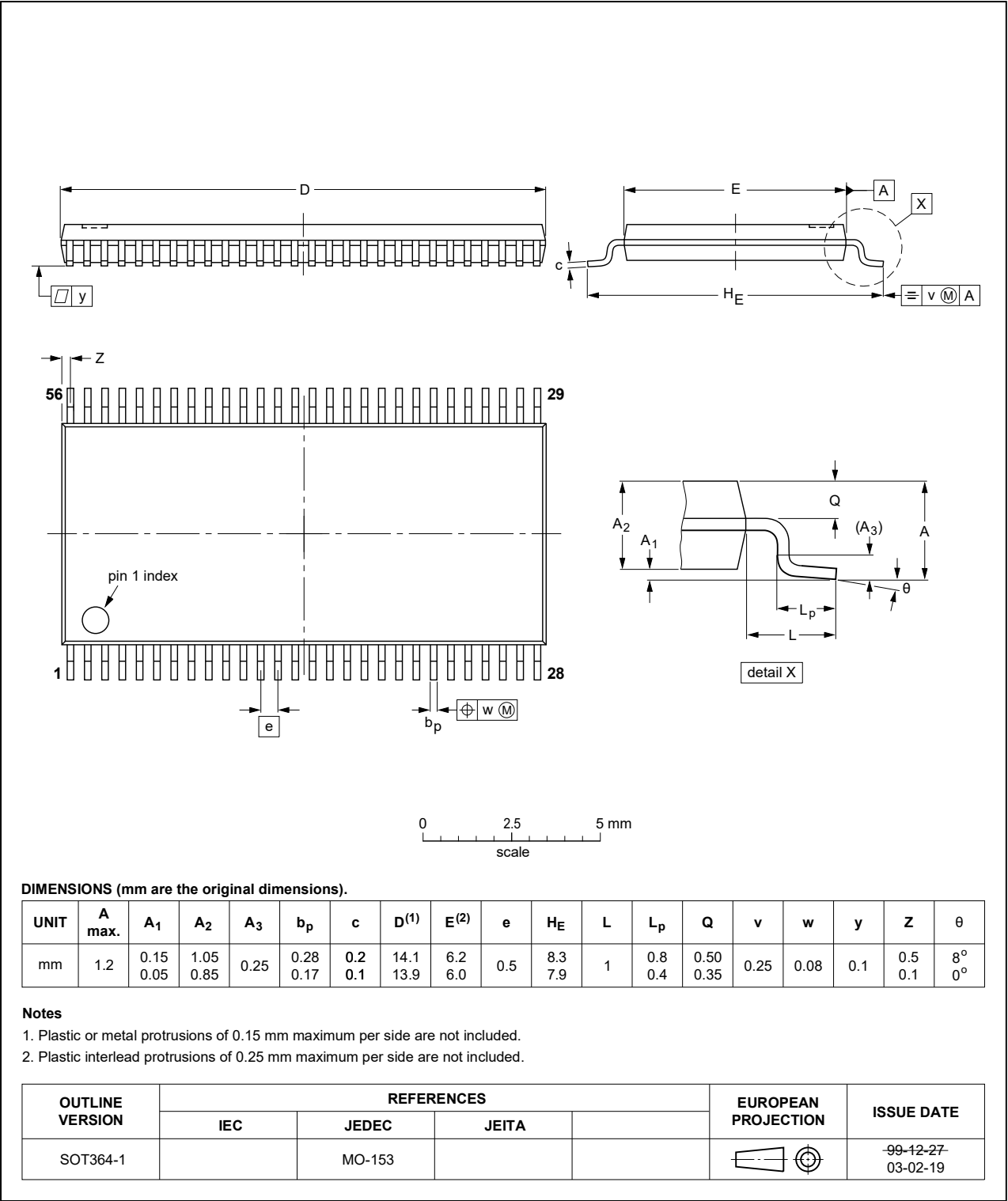


Fig. 10. Package outline SOT364-1 (TSSOP56)

13. Abbreviations

Table 16. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH20T245 v.7	20240625	Product data sheet	-	74AVCH20T245 v.6
Modifications:	<ul style="list-style-type: none"><li>Section 2: ESD specification updated according to the latest JEDEC standard.</li><li>Section 7: <math>P_{tot}</math> and derating values for <math>P_{tot}</math> total power dissipation updated.</li></ul>			
74AVCH20T245 v.6	20190114	Product data sheet	-	74AVCH20T245 v.5
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Type numbers 74AVCH20T245DGV and 74AVCH20T245BX removed.</li></ul>			
74AVCH20T245 v.5	20160223	Product data sheet	-	74AVCH20T245 v.4
Modifications:	<ul style="list-style-type: none"><li>General description updated.</li></ul>			
74AVCH20T245 v.4	20111214	Product data sheet	-	74AVCH20T245 v.3
Modifications:	<ul style="list-style-type: none"><li>Legal pages updated.</li></ul>			
74AVCH20T245 v.3	20110623	Product data sheet	-	74AVCH20T245 v.2
74AVCH20T245 v.2	20100315	Product data sheet	-	74AVCH20T245 v.1
74AVCH20T245 v.1	20100113	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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