74AVCH8T245

8-bit dual supply translating transceiver with configurable voltage translation; 3-state

Rev. 6 — 2 July 2024 Product data sheet

1. General description

The 74AVCH8T245 is an 8-bit, dual supply transceiver that enables bidirectional level translation. It features two 8-bit input-output ports (An and Bn), a direction control input (DIR), a output enable input ($\overline{OE}$) and dual supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). Both $V_{CC(A)}$ and $V_{CC(B)}$ can be supplied at any voltage between 0.8 V and 3.6 V making the device suitable for translating between any of the low voltage nodes (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V). Pins An, $\overline{OE}$ and DIR are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A HIGH on DIR allows transmission from An to Bn and a LOW on DIR allows transmission from Bn to An. The output enable input ($\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated.

The device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either $V_{CC(A)}$ or $V_{CC(B)}$ are at GND level, both An and Bn outputs are in the high-impedance OFF-state. The bus-hold circuitry on the powered-up side always stays active.

The 74AVCH8T245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 0.8 V to 3.6 V
  - $V_{CC(B)}$: 0.8 V to 3.6 V
- Maximum data rates:
  - 380 Mbit/s (≥ 1.8 V to 3.3 V translation)
  - 260 Mbit/s (≥ 1.1 V to 3.3 V translation)
  - 260 Mbit/s (≥ 1.1 V to 2.5 V translation)
  - 210 Mbit/s (≥ 1.1 V to 1.8 V translation)
  - 150 Mbit/s (≥ 1.1 V to 1.5 V translation)
  - 100 Mbit/s (≥ 1.1 V to 1.2 V translation)
- Suspend mode
- Bus hold on data inputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3B exceeds 8000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVCH8T245PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74AVCH8T245BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

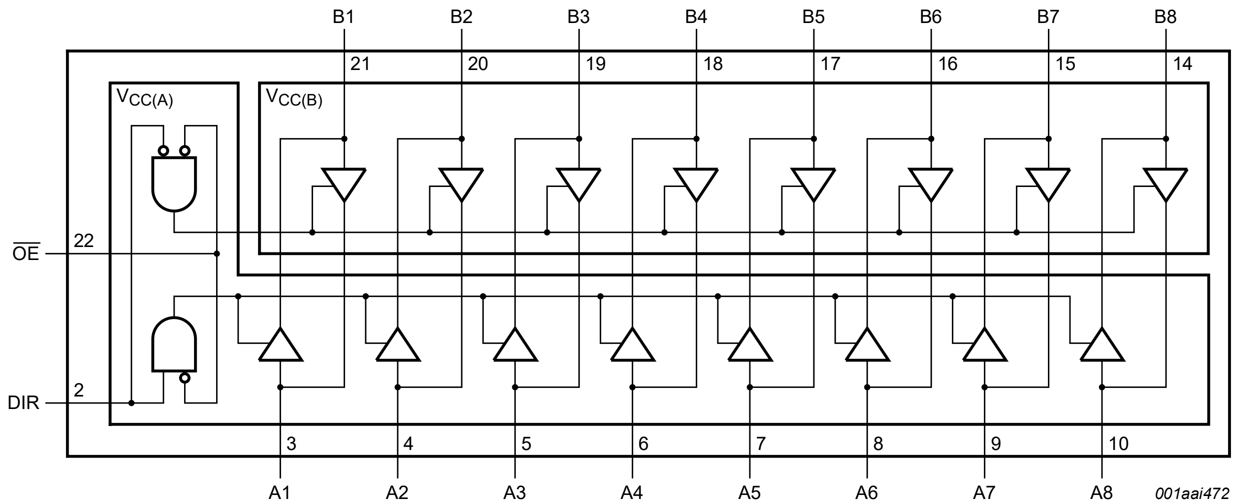


Fig. 1. Logic symbol

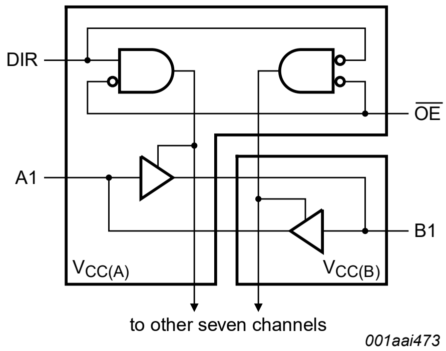
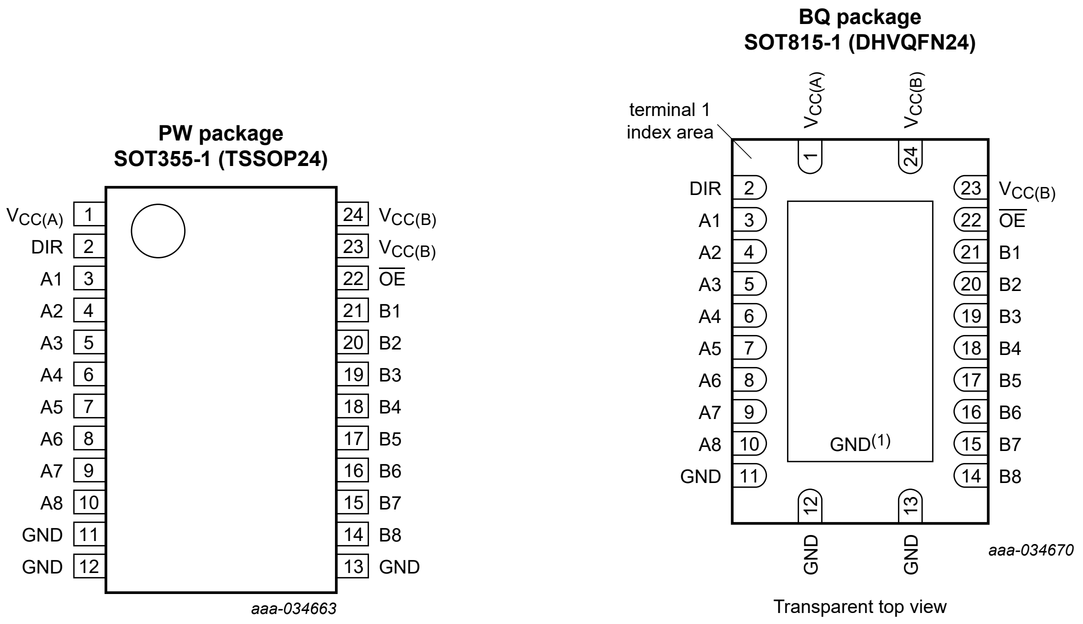


Fig. 2. Logic diagram (one channel)

5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A (An, $\overline{\text{OE}}$ and DIR inputs are referenced to $V_{CC(A)}$)
DIR	2	direction control
A1, A2, A3, A4, A5, A6, A7, A8	3, 4, 5, 6, 7, 8, 9, 10	data input or output
GND [1]	11, 12, 13	ground (0 V)
B1, B2, B3, B4, B5, B6, B7, B8	21, 20, 19, 18, 17, 16, 15, 14	data input or output
$\overline{\text{OE}}$	22	output enable input (active LOW)
$V_{CC(B)}$	23, 24	supply voltage B (Bn inputs are referenced to $V_{CC(B)}$)

[1] All GND pins must be connected to ground (0 V).

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Supply voltage	Input		Input/output [1]	
$V_{CC(A)}$, $V_{CC(B)}$	$\overline{OE}$ [2]	DIR [2]	An [2]	Bn
0.8 V to 3.6 V	L	L	An = Bn	input
0.8 V to 3.6 V	L	H	input	Bn = An
0.8 V to 3.6 V	H	X	Z	Z
GND [1]	X	X	Z	Z

[1] If at least one of $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into suspend mode.
[2] The An, DIR and $\overline{OE}$ input circuit is referenced to $V_{CC(A)}$; The Bn input circuit is referenced to $V_{CC(B)}$.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			-0.5	+4.6	V
$V_{CC(B)}$	supply voltage B			-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
V_O	output voltage	Active mode	[1][2][3]	-0.5	V_{CCO} + 0.5	V
		Suspend or 3-state mode	[1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current	per $V_{CC(A)}$ or $V_{CC(B)}$ pin		-	100	mA
I_{GND}	ground current	per GND pin		-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[4]	-	500	mW

[1] The minimum input voltage ratings and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output port.
[3] V_{CCO} + 0.5 V should not exceed 4.6 V.
[4] For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: P_{tot} derates linearly with 15.0 mW/K above 117 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			0.8	3.6	V
$V_{CC(B)}$	supply voltage B			0.8	3.6	V
V_I	input voltage			0	3.6	V
V_O	output voltage	Active mode	[1]	0	V_{CCO}	V
		Suspend or 3-state mode		0	3.6	V
T_{amb}	ambient temperature			-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CCI} = 0.8 V to 3.6 V	[2]	-	5	ns/V

[1] V_{CCO} is the supply voltage associated with the output port.
[2] V_{CCI} is the supply voltage associated with the input port.

9. Static characteristics

Table 6. Typical static characteristics at T_{amb} = 25 °C
V_{CCO} is the supply voltage associated with the output port.
V_{CCI} is the supply voltage associated with the data input port.
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = -1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V		-	0.69	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 1.5 mA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V		-	0.07	-	V
I_I	input leakage current	DIR, $\overline{OE}$ input; V_I = 0 V or 3.6 V; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.025	±0.25	μA
I_{BHL}	bus hold LOW current	A or B port; V_I = 0.42 V; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V	[1]	-	26	-	μA
I_{BHH}	bus hold HIGH current	A or B port; V_I = 0.78 V; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V	[2]	-	-24	-	μA
I_{BHLO}	bus hold LOW overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V	[3]	-	27	-	μA
I_{BHHO}	bus hold HIGH overdrive current	A or B port; $V_{CC(A)} = V_{CC(B)}$ = 1.2 V	[4]	-	-26	-	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)} = V_{CC(B)}$ = 3.6 V	[5]	-	±0.5	±2.5	μA
		suspend mode A port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	[5]	-	±0.5	±2.5	μA
		suspend mode B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	[5]	-	±0.5	±2.5	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0.8 V to 3.6 V		-	±0.1	±1	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	input capacitance	DIR, $\overline{OE}$ input; V_I = 0 V or 3.3 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V	-	1.5	-	pF
$C_{I/O}$	input/output capacitance	A and B port; V_O = 3.3 V or 0 V; $V_{CC(A)} = V_{CC(B)}$ = 3.3 V	-	4.3	-	pF

[1] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL} max.
[2] The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH} min.
[3] An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.
[4] An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.
[5] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 7. Static characteristics

V_{CCO} is the supply voltage associated with the output port.
V_{CCI} is the supply voltage associated with the data input port.
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	data input					
		V_{CCI} = 0.8 V	$0.70V_{CCI}$	-	$0.70V_{CCI}$	-	V
		V_{CCI} = 1.1 V to 1.95 V	$0.65V_{CCI}$	-	$0.65V_{CCI}$	-	V
		V_{CCI} = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		V_{CCI} = 3.0 V to 3.6 V	2	-	2	-	V
		DIR, $\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	$0.70V_{CC(A)}$	-	$0.70V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	1.6	-	1.6	-	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	2	-	2	-	V
V_{IL}	LOW-level input voltage	data input					
		V_{CCI} = 0.8 V	-	$0.30V_{CCI}$	-	$0.30V_{CCI}$	V
		V_{CCI} = 1.1 V to 1.95 V	-	$0.35V_{CCI}$	-	$0.35V_{CCI}$	V
		V_{CCI} = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		V_{CCI} = 3.0 V to 3.6 V	-	0.8	-	0.8	V
		DIR, $\overline{OE}$ input					
		$V_{CC(A)}$ = 0.8 V	-	$0.30V_{CC(A)}$	-	$0.30V_{CC(A)}$	V
		$V_{CC(A)}$ = 1.1 V to 1.95 V	-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
		$V_{CC(A)}$ = 2.3 V to 2.7 V	-	0.7	-	0.7	V
		$V_{CC(A)}$ = 3.0 V to 3.6 V	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = -100 μA; $V_{CC(A)} = V_{CC(B)}$ = 0.8 V to 3.6 V	V_{CCO} - 0.1	-	V_{CCO} - 0.1	-	V
		I_O = -3 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.1 V	0.85	-	0.85	-	V
		I_O = -6 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.4 V	1.05	-	1.05	-	V
		I_O = -8 mA; $V_{CC(A)} = V_{CC(B)}$ = 1.65 V	1.2	-	1.2	-	V
		I_O = -9 mA; $V_{CC(A)} = V_{CC(B)}$ = 2.3 V	1.75	-	1.75	-	V
		I_O = -12 mA; $V_{CC(A)} = V_{CC(B)}$ = 3.0 V	2.3	-	2.3	-	V

Symbol	Parameter	Conditions		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100\ \mu A$; $V_{CC(A)} = V_{CC(B)} = 0.8\ V$ to $3.6\ V$		-	0.1	-	0.1	V
		$I_O = 3\ mA$; $V_{CC(A)} = V_{CC(B)} = 1.1\ V$		-	0.25	-	0.25	V
		$I_O = 6\ mA$; $V_{CC(A)} = V_{CC(B)} = 1.4\ V$		-	0.35	-	0.35	V
		$I_O = 8\ mA$; $V_{CC(A)} = V_{CC(B)} = 1.65\ V$		-	0.45	-	0.45	V
		$I_O = 9\ mA$; $V_{CC(A)} = V_{CC(B)} = 2.3\ V$		-	0.55	-	0.55	V
		$I_O = 12\ mA$; $V_{CC(A)} = V_{CC(B)} = 3.0\ V$		-	0.7	-	0.7	V
I_I	input leakage current	DIR, $\overline{OE}$ input; $V_I = 0\ V$ or $3.6\ V$; $V_{CC(A)} = V_{CC(B)} = 0.8\ V$ to $3.6\ V$		-	±1	-	±5	μA
I_{BHL}	bus hold LOW current	A or B port	[1]					
		$V_I = 0.49\ V$; $V_{CC(A)} = V_{CC(B)} = 1.4\ V$		15	-	15	-	μA
		$V_I = 0.58\ V$; $V_{CC(A)} = V_{CC(B)} = 1.65\ V$		25	-	25	-	μA
		$V_I = 0.70\ V$; $V_{CC(A)} = V_{CC(B)} = 2.3\ V$		45	-	45	-	μA
		$V_I = 0.80\ V$; $V_{CC(A)} = V_{CC(B)} = 3.0\ V$		100	-	90	-	μA
I_{BHH}	bus hold HIGH current	A or B port	[2]					
		$V_I = 0.91\ V$; $V_{CC(A)} = V_{CC(B)} = 1.4\ V$		-15	-	-15	-	μA
		$V_I = 1.07\ V$; $V_{CC(A)} = V_{CC(B)} = 1.65\ V$		-25	-	-25	-	μA
		$V_I = 1.60\ V$; $V_{CC(A)} = V_{CC(B)} = 2.3\ V$		-45	-	-45	-	μA
		$V_I = 2.00\ V$; $V_{CC(A)} = V_{CC(B)} = 3.0\ V$		-100	-	-100	-	μA
I_{BHLO}	bus hold LOW overdrive current	A or B port	[3]					
		$V_{CC(A)} = V_{CC(B)} = 1.6\ V$		125	-	125	-	μA
		$V_{CC(A)} = V_{CC(B)} = 1.95\ V$		200	-	200	-	μA
		$V_{CC(A)} = V_{CC(B)} = 2.7\ V$		300	-	300	-	μA
		$V_{CC(A)} = V_{CC(B)} = 3.6\ V$		500	-	500	-	μA
I_{BHHO}	bus hold HIGH overdrive current	A or B port	[4]					
		$V_{CC(A)} = V_{CC(B)} = 1.6\ V$		-125	-	-125	-	μA
		$V_{CC(A)} = V_{CC(B)} = 1.95\ V$		-200	-	-200	-	μA
		$V_{CC(A)} = V_{CC(B)} = 2.7\ V$		-300	-	-300	-	μA
		$V_{CC(A)} = V_{CC(B)} = 3.6\ V$		-500	-	-500	-	μA
I_{OZ}	OFF-state output current	A or B port; $V_O = 0\ V$ or V_{CCO}; $V_{CC(A)} = V_{CC(B)} = 3.6\ V$	[5]	-	±5	-	±30	μA
		suspend mode A port; $V_O = 0\ V$ or V_{CCO}; $V_{CC(A)} = 3.6\ V$; $V_{CC(B)} = 0\ V$	[5]	-	±5	-	±30	μA
		suspend mode B port; $V_O = 0\ V$ or V_{CCO}; $V_{CC(A)} = 0\ V$; $V_{CC(B)} = 3.6\ V$	[5]	-	±5	-	±30	μA
I_{OFF}	power-off leakage current	A port; V_I or $V_O = 0\ V$ to $3.6\ V$; $V_{CC(A)} = 0\ V$; $V_{CC(B)} = 0.8\ V$ to $3.6\ V$		-	±5	-	±30	μA
		B port; V_I or $V_O = 0\ V$ to $3.6\ V$; $V_{CC(B)} = 0\ V$; $V_{CC(A)} = 0.8\ V$ to $3.6\ V$		-	±5	-	±30	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	A port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	10	-	55	μA
		$V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	8	-	50	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-	8	-	50	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	-2	-	-12	-	μA
		B port; V_I = 0 V or V_{CCI}; I_O = 0 A					
		$V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	10	-	55	μA
		$V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	8	-	50	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	-2	-	-12	-	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 3.6 V	-	8	-	50	μA
		A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 0.8 V to 3.6 V; $V_{CC(B)}$ = 0.8 V to 3.6 V	-	20	-	70	μA
		A plus B port ($I_{CC(A)}$ + $I_{CC(B)}$); I_O = 0 A; V_I = 0 V or V_{CCI}; $V_{CC(A)}$ = 1.1 V to 3.6 V; $V_{CC(B)}$ = 1.1 V to 3.6 V	-	16	-	65	μA

[1] The bus hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_I to GND and then raising it to V_{IL} max.
[2] The bus hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_I to V_{CC} and then lowering it to V_{IH} min.
[3] An external driver must source at least I_{BHLO} to switch this node from LOW to HIGH.
[4] An external driver must sink at least I_{BHHO} to switch this node from HIGH to LOW.
[5] For I/O ports, the parameter I_{OZ} includes the input leakage current.

Table 8. Typical total supply current ($I_{CC(A)}$ + $I_{CC(B)}$)

$V_{CC(A)}$	$V_{CC(B)}$							Unit
	0 V	0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	0.1	0.1	0.1	0.1	0.1	0.1	μA
0.8 V	0.1	0.1	0.1	0.1	0.1	0.3	1.6	μA
1.2 V	0.1	0.1	0.1	0.1	0.1	0.1	0.8	μA
1.5 V	0.1	0.1	0.1	0.1	0.1	0.1	0.4	μA
1.8 V	0.1	0.1	0.1	0.1	0.1	0.1	0.2	μA
2.5 V	0.1	0.3	0.1	0.1	0.1	0.1	0.1	μA
3.3 V	0.1	1.6	0.8	0.4	0.2	0.1	0.1	μA

10. Dynamic characteristics

Table 9. Typical dynamic characteristics at $V_{CC(A)}$ = 0.8 V and T_{amb} = 25 °C

t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	An to Bn	14.4	7.0	6.2	6.0	5.9	6.0	ns
		Bn to An	14.4	12.4	12.1	11.9	11.8	11.8	ns
t_{dis}	disable time	$\overline{OE}$ to An	16.2	16.2	16.2	16.2	16.2	16.2	ns
		$\overline{OE}$ to Bn	17.6	10.0	9.0	9.1	8.7	9.3	ns
t_{en}	enable time	$\overline{OE}$ to An	21.9	21.9	21.9	21.9	21.9	21.9	ns
		$\overline{OE}$ to Bn	22.2	11.1	9.8	9.4	9.4	9.6	ns

Table 10. Typical dynamic characteristics at $V_{CC(B)}$ = 0.8 V and T_{amb} = 25 °C

t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4.

Symbol	Parameter	Conditions	$V_{CC(A)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
t_{pd}	propagation delay	An to Bn	14.4	12.4	12.1	11.9	11.8	11.8	ns
		Bn to An	14.4	7.0	6.2	6.0	5.9	6.0	ns
t_{dis}	disable time	$\overline{OE}$ to An	16.2	5.9	4.4	4.2	3.1	3.5	ns
		$\overline{OE}$ to Bn	17.6	14.2	13.7	13.6	13.3	13.1	ns
t_{en}	enable time	$\overline{OE}$ to An	21.9	6.4	4.4	3.5	2.6	2.3	ns
		$\overline{OE}$ to Bn	22.2	17.7	17.2	17.0	16.8	16.7	ns

Table 11. Typical power dissipation capacitance at $V_{CC(A)}$ = $V_{CC(B)}$ and T_{amb} = 25 °C

Voltages are referenced to GND (ground = 0 V). [1] [2]

Symbol	Parameter	Conditions	$V_{CC(A)} = V_{CC(B)}$						Unit
			0.8 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
C_{PD}	power dissipation capacitance	A port: (direction An to Bn); output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction An to Bn); output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		A port: (direction Bn to An); output enabled	9	9	10	10	11	13	pF
		A port: (direction Bn to An); output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction An to Bn); output enabled	9	9	10	10	11	13	pF
		B port: (direction An to Bn); output disabled	0.6	0.6	0.6	0.7	0.7	0.8	pF
		B port: (direction Bn to An); output enabled	0.2	0.2	0.2	0.3	0.4	0.5	pF
		B port: (direction Bn to An); output disabled	0.2	0.2	0.2	0.3	0.4	0.5	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] f_i = 10 MHz; V_I = GND to V_{CC}; $t_r = t_f$ = 1 ns; C_L = 0 pF; $R_L = \infty\ \Omega$.

Table 12. Dynamic characteristics for temperature range -40 °C to +85 °C

t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4.

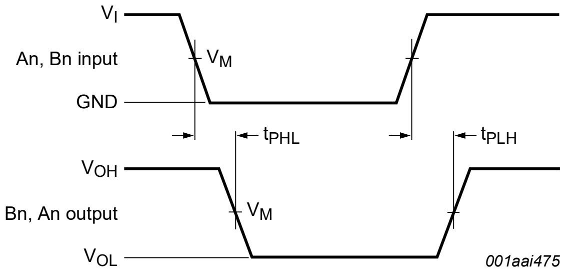
Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	An to Bn	0.5	9.0	0.5	6.7	0.5	5.8	0.5	4.9	0.5	4.8	ns
		Bn to An	0.5	9.0	0.5	8.5	0.5	8.3	0.5	8.0	0.5	7.8	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	0.5	11.8	ns
		$\overline{OE}$ to Bn	0.5	12.3	0.5	9.5	0.5	9.4	0.5	8.0	0.5	8.9	ns
t_{en}	enable time	$\overline{OE}$ to An	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	1.1	14.4	ns
		$\overline{OE}$ to Bn	1.1	14.2	1.1	10.4	1.1	9.0	1.0	7.7	1.0	7.3	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	An to Bn	0.5	8.5	0.5	5.6	0.5	4.7	0.5	4.4	0.5	4.1	ns
		Bn to An	0.5	6.7	0.5	5.6	0.5	5.3	0.5	5.2	0.5	5.0	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	0.5	8.6	ns
		$\overline{OE}$ to Bn	0.5	11.2	0.5	8.4	0.5	7.6	0.5	7.2	0.5	7.8	ns
t_{en}	enable time	$\overline{OE}$ to An	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	1.1	8.7	ns
		$\overline{OE}$ to Bn	1.1	12.8	1.1	8.1	1.1	7.1	1.0	5.6	1.0	5.2	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	An to Bn	0.5	8.3	0.5	5.3	0.5	4.5	0.5	3.8	0.5	3.5	ns
		Bn to An	0.5	5.8	0.5	4.7	0.5	4.5	0.5	4.3	0.5	4.1	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	0.5	7.1	ns
		$\overline{OE}$ to Bn	0.5	10.9	0.5	7.8	0.5	6.9	0.5	6.0	0.5	5.8	ns
t_{en}	enable time	$\overline{OE}$ to An	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	1.0	6.8	ns
		$\overline{OE}$ to Bn	1.1	12.4	1.1	8.2	1.0	6.7	0.5	5.1	0.5	4.5	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	An to Bn	0.5	8.0	0.5	5.2	0.5	4.3	0.5	3.3	0.5	2.9	ns
		Bn to An	0.5	4.9	0.5	4.4	0.5	3.8	0.5	3.3	0.5	3.1	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	0.5	5.1	ns
		$\overline{OE}$ to Bn	0.5	10.4	0.5	7.1	0.5	6.3	0.5	5.1	0.5	5.2	ns
t_{en}	enable time	$\overline{OE}$ to An	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	0.5	4.8	ns
		$\overline{OE}$ to Bn	1.1	11.9	1.1	7.9	0.5	6.4	0.5	4.6	0.5	4.0	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	An to Bn	0.5	7.8	0.5	5.0	0.5	4.1	0.5	3.1	0.5	2.7	ns
		Bn to An	0.5	4.8	0.5	4.1	0.5	3.5	0.5	2.9	0.5	2.7	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	0.5	4.9	ns
		$\overline{OE}$ to Bn	0.5	10.1	0.5	6.9	0.5	6.0	0.5	4.8	0.5	5.0	ns
t_{en}	enable time	$\overline{OE}$ to An	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	0.5	4.0	ns
		$\overline{OE}$ to Bn	1.1	11.7	1.1	7.8	0.5	6.2	0.5	4.5	0.5	3.9	ns

Table 13. Dynamic characteristics for temperature range -40 °C to +125 °C

t_{pd} is the same as t_{PLH} and t_{PHL}; t_{dis} is the same as t_{PLZ} and t_{PHZ}; t_{en} is the same as t_{PZL} and t_{PZH}.
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5; for waveforms see Fig. 3 and Fig. 4

Symbol	Parameter	Conditions	$V_{CC(B)}$										Unit
			1.2 V ± 0.1 V		1.5 V ± 0.1 V		1.8 V ± 0.15 V		2.5 V ± 0.2 V		3.3 V ± 0.3 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.1 V to 1.3 V													
t_{pd}	propagation delay	An to Bn	0.5	9.9	0.5	7.4	0.5	6.4	0.5	5.4	0.5	5.3	ns
		Bn to An	0.5	9.9	0.5	9.4	0.5	9.2	0.5	8.8	0.5	8.6	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	0.5	13.0	ns
		$\overline{OE}$ to Bn	0.5	13.6	0.5	10.5	0.5	10.4	0.5	8.8	0.5	9.8	ns
t_{en}	enable time	$\overline{OE}$ to An	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	1.1	15.9	ns
		$\overline{OE}$ to Bn	1.1	15.7	1.1	11.5	1.1	9.9	1.0	8.5	1.0	8.1	ns
$V_{CC(A)}$ = 1.4 V to 1.6 V													
t_{pd}	propagation delay	An to Bn	0.5	9.4	0.5	6.2	0.5	5.2	0.5	4.9	0.5	4.6	ns
		Bn to An	0.5	7.4	0.5	6.2	0.5	5.9	0.5	5.8	0.5	5.5	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	0.5	9.5	ns
		$\overline{OE}$ to Bn	0.5	12.4	0.5	9.3	0.5	8.4	0.5	8.0	0.5	8.6	ns
t_{en}	enable time	$\overline{OE}$ to An	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	1.1	9.6	ns
		$\overline{OE}$ to Bn	1.1	14.1	1.1	9.0	1.1	7.9	1.0	6.2	1.0	5.8	ns
$V_{CC(A)}$ = 1.65 V to 1.95 V													
t_{pd}	propagation delay	An to Bn	0.5	9.2	0.5	5.9	0.5	5.0	0.5	4.2	0.5	3.9	ns
		Bn to An	0.5	6.4	0.5	5.2	0.5	5.0	0.5	4.8	0.5	4.6	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	0.5	7.9	ns
		$\overline{OE}$ to Bn	0.5	12.0	0.5	8.6	0.5	7.6	0.5	6.6	0.5	6.4	ns
t_{en}	enable time	$\overline{OE}$ to An	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	1.0	7.5	ns
		$\overline{OE}$ to Bn	1.1	13.7	1.1	9.1	1.0	7.4	0.5	5.7	0.5	5.0	ns
$V_{CC(A)}$ = 2.3 V to 2.7 V													
t_{pd}	propagation delay	An to Bn	0.5	8.8	0.5	5.8	0.5	4.8	0.5	3.7	0.5	3.2	ns
		Bn to An	0.5	5.4	0.5	4.9	0.5	4.2	0.5	3.7	0.5	3.5	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	0.5	5.7	ns
		$\overline{OE}$ to Bn	0.5	11.5	0.5	7.9	0.5	7.0	0.5	5.7	0.5	5.8	ns
t_{en}	enable time	$\overline{OE}$ to An	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	0.5	5.3	ns
		$\overline{OE}$ to Bn	1.1	13.1	1.1	8.7	0.5	7.1	0.5	5.1	0.5	4.4	ns
$V_{CC(A)}$ = 3.0 V to 3.6 V													
t_{pd}	propagation delay	An to Bn	0.5	8.6	0.5	5.5	0.5	4.6	0.5	3.5	0.5	3.0	ns
		Bn to An	0.5	5.3	0.5	4.6	0.5	3.9	0.5	3.2	0.5	3.0	ns
t_{dis}	disable time	$\overline{OE}$ to An	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	0.5	5.4	ns
		$\overline{OE}$ to Bn	0.5	11.2	0.5	7.6	0.5	6.6	0.5	5.3	0.5	5.5	ns
t_{en}	enable time	$\overline{OE}$ to An	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	0.5	4.4	ns
		$\overline{OE}$ to Bn	1.1	12.9	1.1	8.6	0.5	6.9	0.5	5.0	0.5	4.3	ns

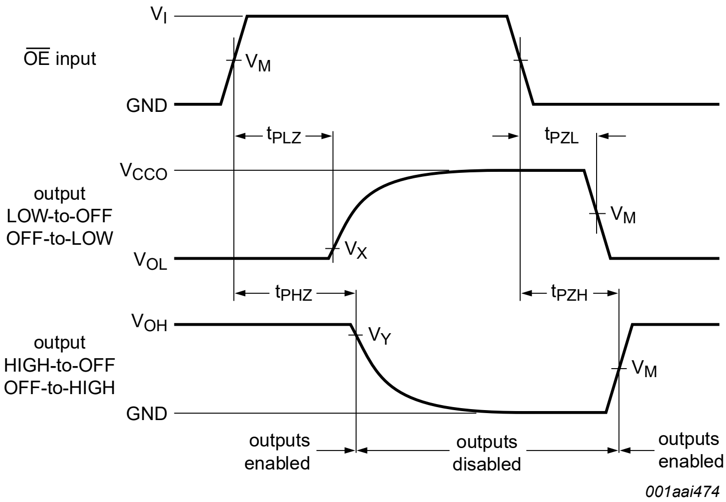
10.1. Waveforms and test circuit



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. The data input (An, Bn) to output (Bn, An) propagation delay times



Measurement points are given in Table 14.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

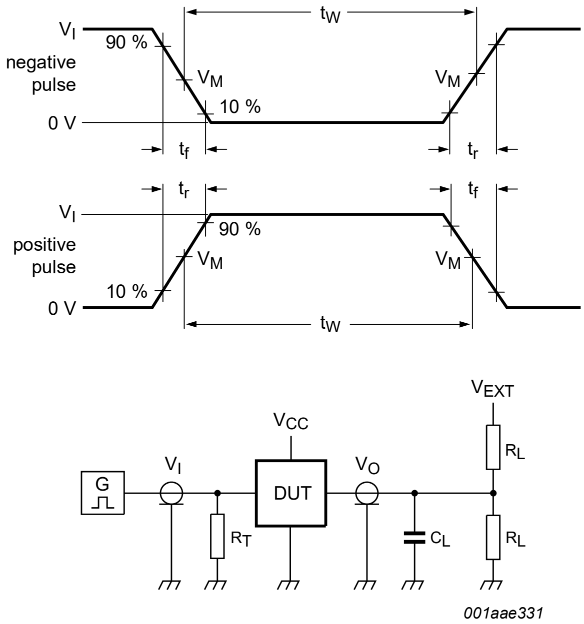
Fig. 4. Enable and disable times

Table 14. Measurement points

Supply voltage	**Input [1]**	**Output [2]**		
$V_{CC(A)}$, $V_{CC(B)}$	V_M	V_M	V_X	V_Y
0.8 V to 1.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} - 0.1 V
1.65 V to 2.7 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} - 0.3 V

[1] V_{CCI} is the supply voltage associated with the data input port.

[2] V_{CCO} is the supply voltage associated with the output port.



Test data is given in Table 15.:
Definitions test circuit:
R_L = Load resistance;
C_L = Load capacitance including jig and probe capacitance;
R_T = Termination resistance;
V_{EXT} = External voltage for measuring switching times.

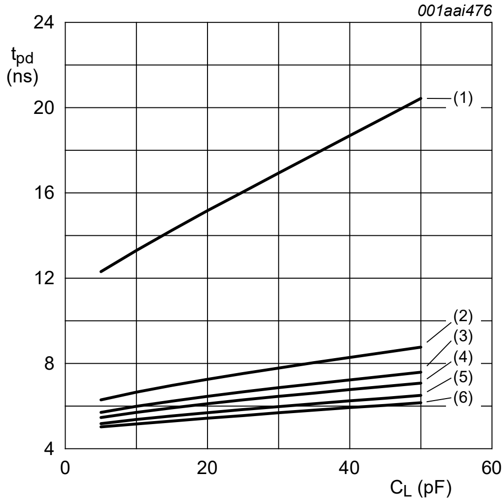
Fig. 5. Test circuit for measuring switching times

Table 15. Test data

Supply voltage	Input		Load		V_{EXT}		
$V_{CC(A)}$, $V_{CC(B)}$	V_I [1]	$\Delta t/\Delta V$ [2]	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ} [3]
0.8 V to 1.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
1.65 V to 2.7 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$
3.0 V to 3.6 V	V_{CCI}	≤ 1.0 ns/V	15 pF	2 kΩ	open	GND	$2V_{CCO}$

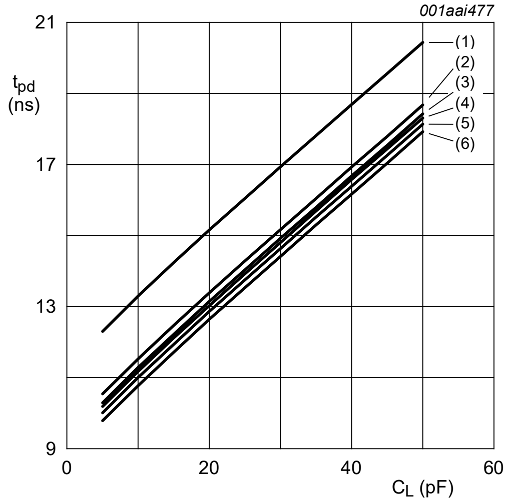
[1] V_{CCI} is the supply voltage associated with the data input port.
[2] dV/dt ≥ 1.0 V/ns
[3] V_{CCO} is the supply voltage associated with the output port.

10.2. Typical propagation delay characteristics



a. Propagation delay (An to Bn); $V_{CC(A)}$ = 0.8 V

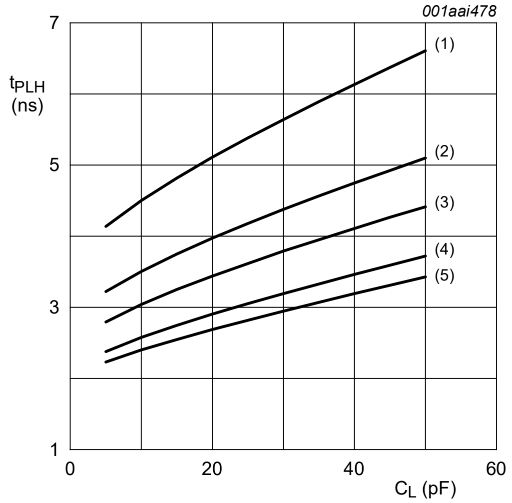
(1) $V_{CC(B)}$ = 0.8 V
(2) $V_{CC(B)}$ = 1.2 V
(3) $V_{CC(B)}$ = 1.5 V
(4) $V_{CC(B)}$ = 1.8 V
(5) $V_{CC(B)}$ = 2.5 V
(6) $V_{CC(B)}$ = 3.3 V



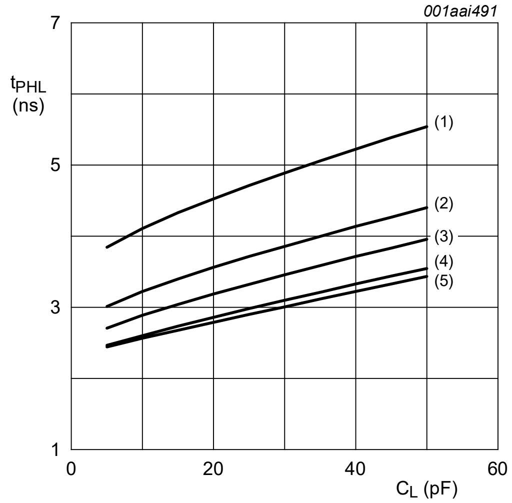
b. Propagation delay (An to Bn); $V_{CC(B)}$ = 0.8 V

(1) $V_{CC(A)}$ = 0.8 V
(2) $V_{CC(A)}$ = 1.2 V
(3) $V_{CC(A)}$ = 1.5 V
(4) $V_{CC(A)}$ = 1.8 V
(5) $V_{CC(A)}$ = 2.5 V
(6) $V_{CC(A)}$ = 3.3 V

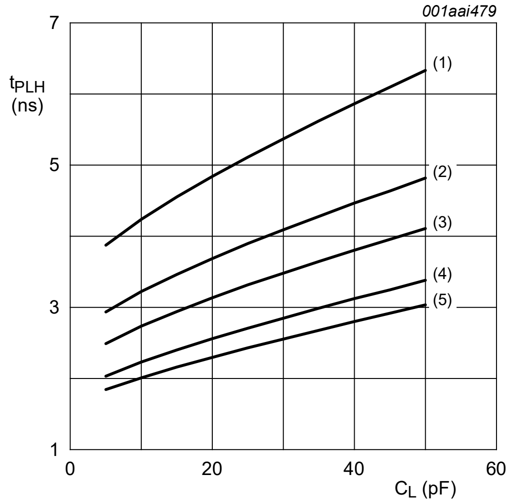
Fig. 6. Typical propagation delay vs load capacitance; T_{amb} = 25 °C



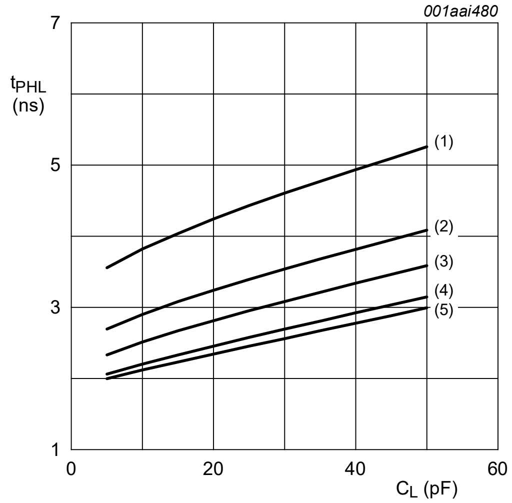
a. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$ = 1.2 V



b. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$ = 1.2 V



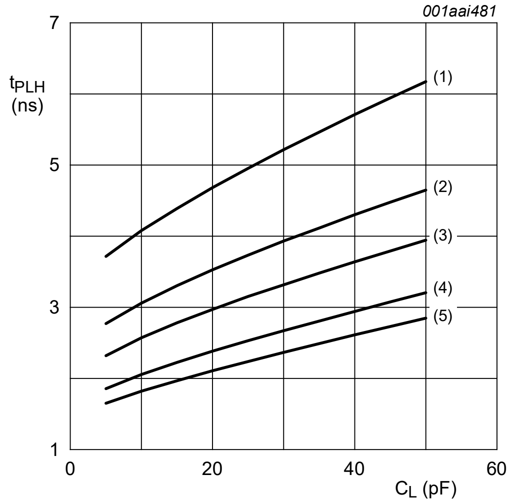
c. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$ = 1.5 V



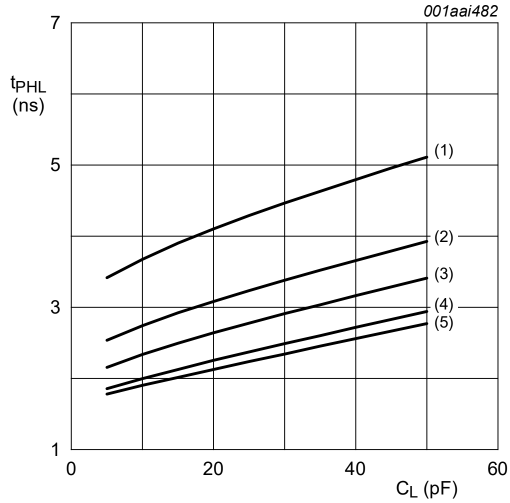
d. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$ = 1.5 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

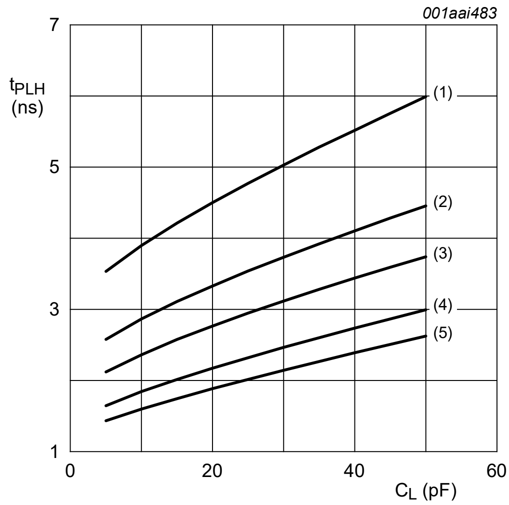
Fig. 7. Typical propagation delay vs load capacitance; T_{amb} = 25 °C



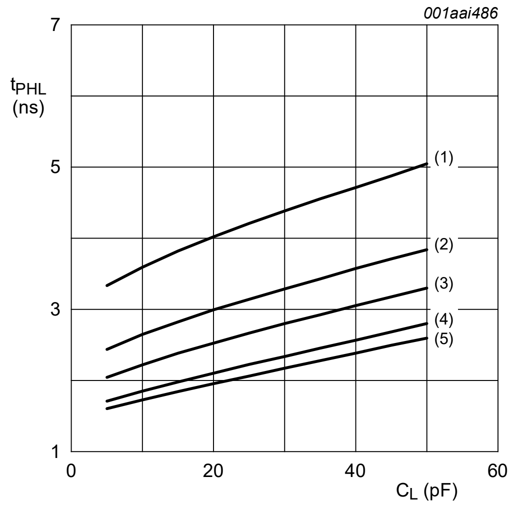
a. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$ = 1.8 V



b. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$ = 1.8 V



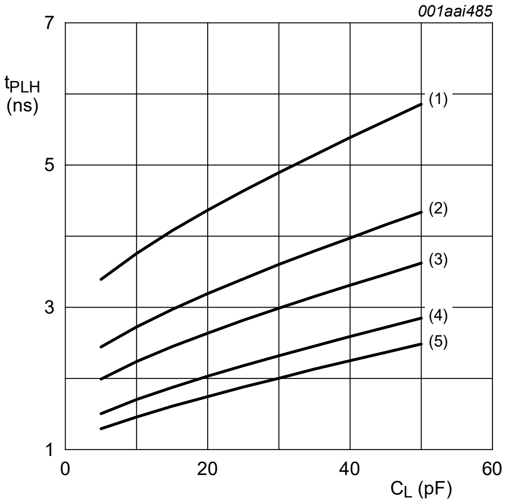
c. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$ = 2.5 V



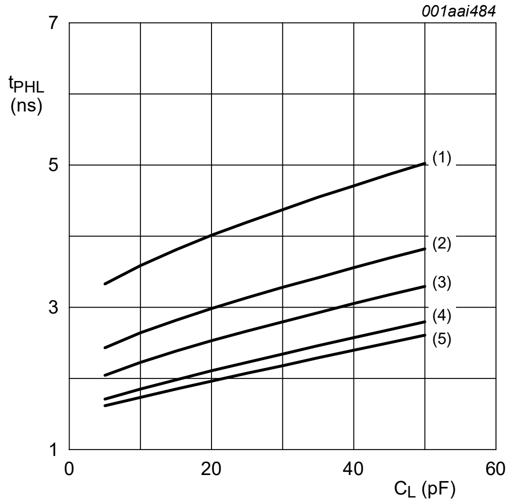
d. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$ = 2.5 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

Fig. 8. Typical propagation delay vs load capacitance; T_{amb} = 25 °C



a. LOW to HIGH propagation delay (An to Bn); $V_{CC(A)}$ = 3.3 V



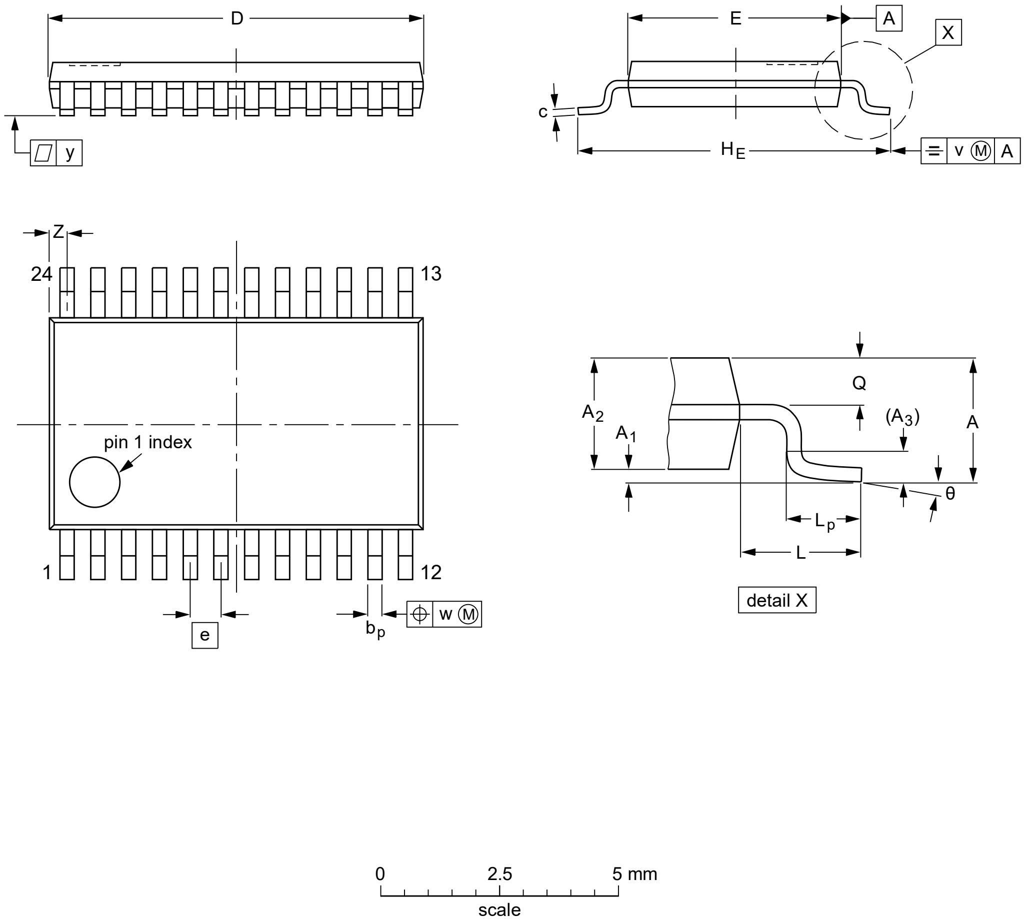
b. HIGH to LOW propagation delay (An to Bn); $V_{CC(A)}$ = 3.3 V

(1) $V_{CC(B)}$ = 1.2 V
(2) $V_{CC(B)}$ = 1.5 V
(3) $V_{CC(B)}$ = 1.8 V
(4) $V_{CC(B)}$ = 2.5 V
(5) $V_{CC(B)}$ = 3.3 V

Fig. 9. Typical propagation delay vs load capacitance; T_{amb} = 25 °C

11. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

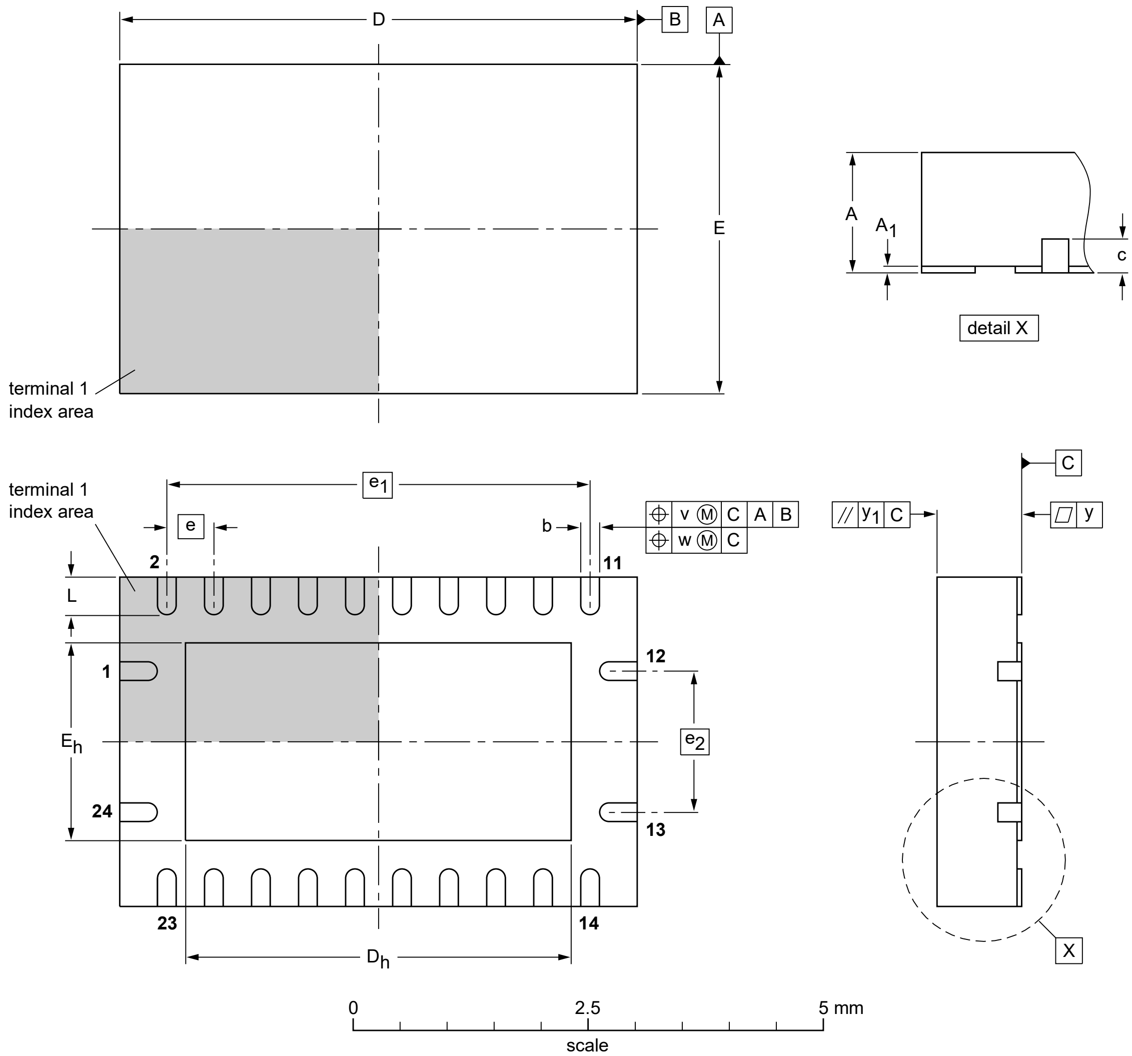
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

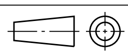
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig. 11. Package outline SOT815-1 (DHVQFN24)

12. Abbreviations

Table 16. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVCH8T245 v.6	20240702	Product data sheet	-	74AVCH8T245 v.5
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Section 7: Derating values for P_{tot} total power dissipation updated. • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74AVCH8T245 v.5	20121227	Product data sheet	-	74AVCH8T245 v.4
Modifications:	• Table 4: conditions I_{CC} and I_{GND} changed (errata).			
74AVCH8T245 v.4	20111214	Product data sheet	-	74AVCH8T245 v.3
Modifications:	• Legal pages updated.			
74AVCH8T245 v.3	20110927	Product data sheet	-	74AVCH8T245 v.2
74AVCH8T245 v.2	20090428	Product data sheet	-	74AVCH8T245 v.1
74AVCH8T245 v.1	20080709	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 2 July 2024