# **Dual 4-input NOR gate**

Rev. 8 — 19 March 2024

**Product data sheet** 

## 1. General description

The 74HC4002 is a dual 4-input NOR gate. Inputs also include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

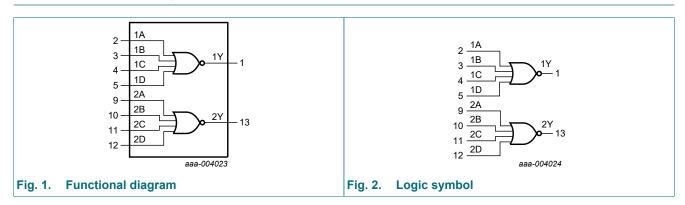
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- CMOS input levels
- · Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +80 °C and from -40 °C to +125 °C.

# 3. Ordering information

Table 1. Ordering information

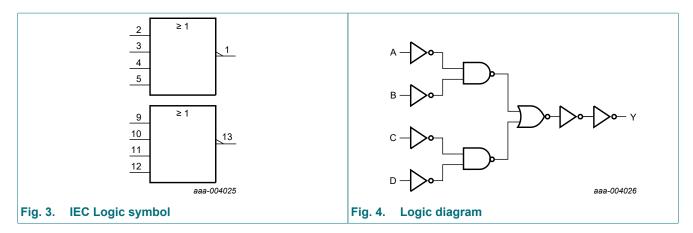
Type number	ber Package							
	Temperature range	Name	Description	Version				
74HC4002D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1				
74HC4002PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1				

# 4. Functional diagram



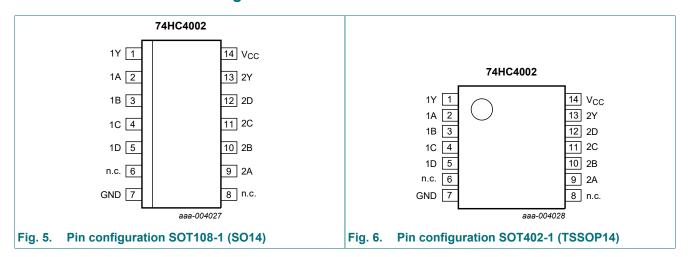


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# 5. Pinning information

## 5.1. Pinning



## 5.2. Pin description

**Table 2. Pin description** 

Symbol	Pin	Description
1Y, 2Y	1, 13	data output
1A, 1B, 1C, 1D	2, 3, 4, 5	data input
n.c.	6, 8	not connected
GND	7	ground (0 V)
2A, 2B, 2C, 2D	9, 10, 11, 12	data input
V <sub>CC</sub>	14	supply voltage

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# 6. Functional description

#### **Table 3. Function table**

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care.$ 

Input	Output			
nA	nB	nC	nD	nY
L	L	L	L	Н
Н	Х	Х	Х	L
X	Н	Х	Х	L
X	Х	Н	Х	L
X	Х	Х	Н	L

## 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
l <sub>OK</sub>	output clamping current	$V_{O}$ < -0.5 V or $V_{O}$ > $V_{CC}$ + 0.5 V	[1]	-	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±25	mA
I <sub>CC</sub>	supply current			-	50	mA
I <sub>GND</sub>	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation		[2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	ns/V

<sup>[2]</sup> For SOT108-1 (SO14) package: P<sub>tot</sub> derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) package: P<sub>tot</sub> derates linearly with 7.3 mW/K above 81 °C.

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## 9. Static characteristics

**Table 6. Static characteristics** 

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
$V_{OL}$	LOW-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	2	-	20	-	40	μΑ
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

# 10. Dynamic characteristics

## **Table 7. Dynamic characteristics**

GND = 0 V;  $C_L$  = 50 pF; for test circuit see Fig. 8.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB, nC or nD to nY; [1] see Fig. 7								
		V <sub>CC</sub> = 2.0 V	-	30	100	-	125	-	150	ns
		V <sub>CC</sub> = 4.5 V	-	11	20	-	25	-	30	ns
		V <sub>CC</sub> = 6.0 V	-	9	17	-	21	-	26	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	9	-	-	-	-	-	ns

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Symbol	Symbol Parameter Conditions		arameter Conditions 25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
t <sub>t</sub>	transition	nY; see Fig. 7 [2]								
	time	V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns
C <sub>PD</sub>	power dissipation capacitance	per package; [3] V <sub>I</sub> = GND to V <sub>CC</sub>	-	16	-	-	-	-	-	pF

- $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .
- t<sub>t</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.
   C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

 $P_D = C_{PD} x V_{CC}^2 x f_i x N + \Sigma (C_L x V_{CC}^2 x f_o)$  where:

f<sub>i</sub> = input frequency in MHz;

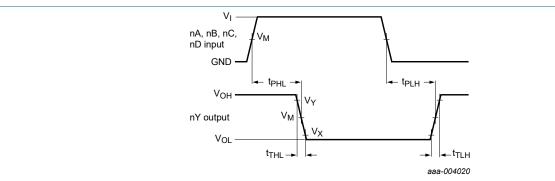
f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;  $\Sigma(C_L \ x \ V_{CC} \ ^2 \ x \ f_o) = sum \ of \ outputs.$ 

### 10.1. Waveforms and test circuit



Measurement points are given in Table 8.

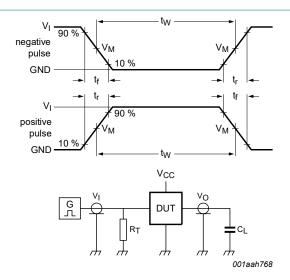
V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Waveforms showing the input (nA, nB, nC, nD) to output (nY) propagation delays and the output transition Fig. 7. times

Table 8. Measurement points

Input	Output	Dutput					
$V_{M}$	V <sub>M</sub>	V <sub>X</sub>	$V_{Y}$				
0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	0.1V <sub>CC</sub>	0.9V <sub>CC</sub>				

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Test data is given in Table 9.

Definitions test circuit:

 $R_{T}$  = termination resistance should be equal to output impedance  $Z_{o}$  of the pulse generator.

 $C_L$  = load capacitance including jig and probe capacitance.

## Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Input		Load	Test
		CL	
V <sub>CC</sub>	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>

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# 11. Package outline

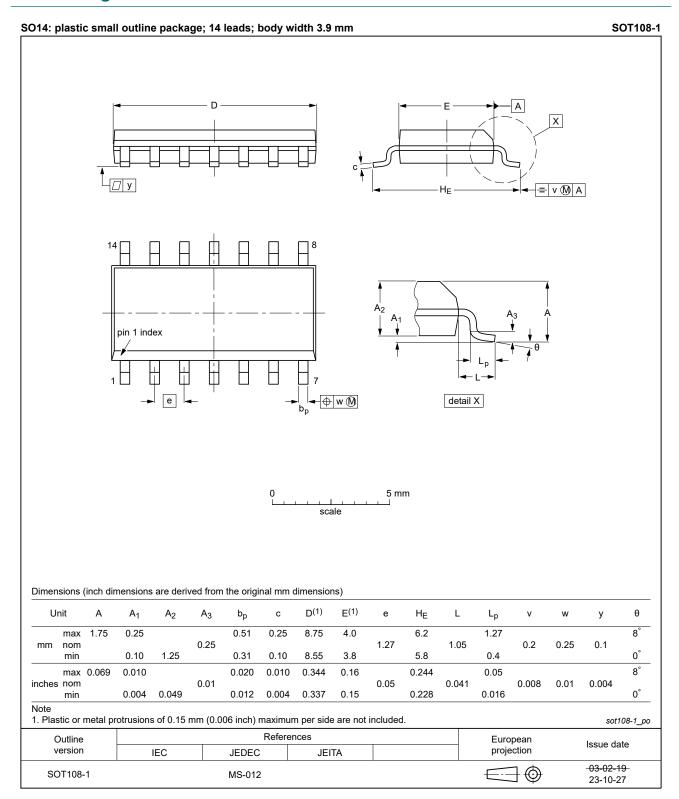


Fig. 9. Package outline SOT108-1 (SO14)

## **Dual 4-input NOR gate**

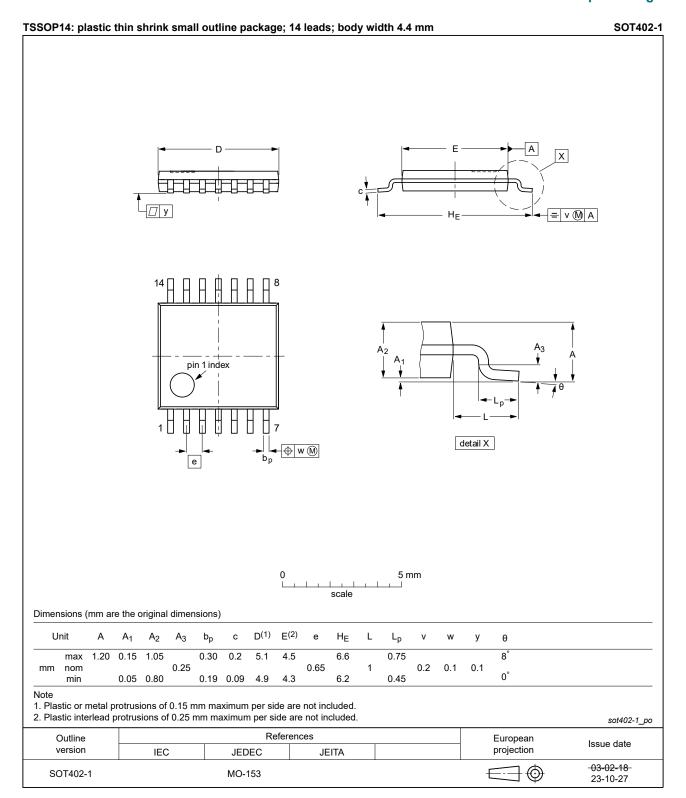


Fig. 10. Package outline SOT402-1 (TSSOP14)

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## 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description			
CDM	Charged Device Model			
CMOS	plementary Metal Oxide Semiconductor			
DUT	Device Under Test			
ESD	ElectroStatic Discharge			
НВМ	Human Body Model			

# 13. Revision history

#### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC4002 v.8	20240319	Product data sheet	-	74HC_HCT4002 v.7	
Modifications:	MO-153.	0: Aligned SO and TSSOP SD specification updated a		ngs to JEDEC MS-012 and EDEC standard.	
74HC4002 v.7	20210913	Product data sheet	-	74HC_HCT4002 v.6	
Modifications:	Type number	r 74HC4002DB (SOT337-1	/ SSOP14) removed.		
74HC4002 v.6	20210311	Product data sheet	-	74HC_HCT4002 v.5	
	<ul><li>Section 2 up</li><li>Section 7: D</li></ul>	erating values for P <sub>tot</sub> total ers 74HCT4002D (SOT108-	power dissipation have	changed.	
74HC_HCT4002 v.5	20160526	Product data sheet	-	74HC_HCT4002 v.4	
Modifications:	Type number	rs 74HC4002N and 74HCT	4002N (SOT27-1) rem	oved.	
74HC_HCT4002 v.4	20120917	Product data sheet	-	74HC_HCT4002 v.3	
Modifications:	• Table 1: Typ	e number 74HC20DB chan	ged into 74HC4002DB		
74HC_HCT4002 v.3	20120904	Product data sheet	-	74HC_HCT4002_CNV v.2	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>				
74HC_HCT4002_CNV v.2	19970829	Product specification			

#### **Dual 4-input NOR gate**

## 14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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