

74HC253-Q100; 74HCT253-Q100

Dual 4-input multiplexer; 3-state

Rev. 5 — 11 March 2024

Product data sheet

1. General description

The 74HC253-Q100; 74HCT253-Q100 is a dual 4-bit multiplexer, each with four binary inputs (nI0 to nI3), an output enable input (nOE) and shared select inputs (S0 and S1). One of the four binary inputs is selected by the select inputs and routed to the output nY. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Non-inverting data path
- 3-state outputs interface directly with system bus
- Common select inputs
- Separate output enable inputs
- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC253-Q100: CMOS level
 - For 74HCT253-Q100: TTL level
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Applications

- Data selectors
- Data multiplexers

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC253D-Q100 74HCT253D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC253BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

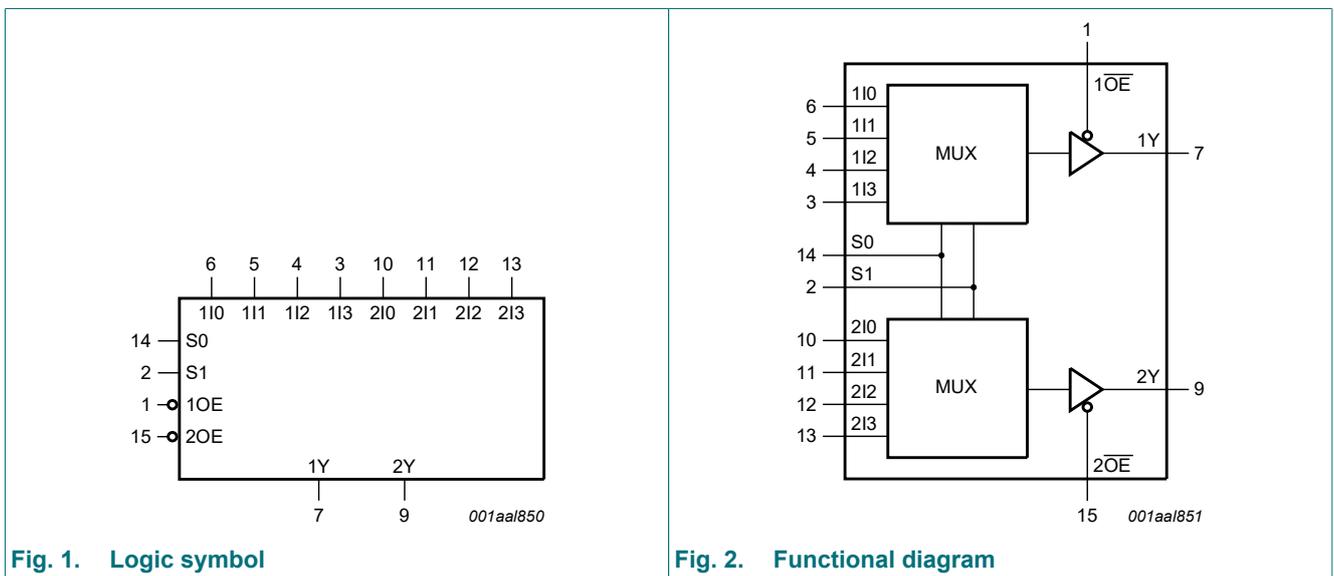


Fig. 1. Logic symbol

Fig. 2. Functional diagram

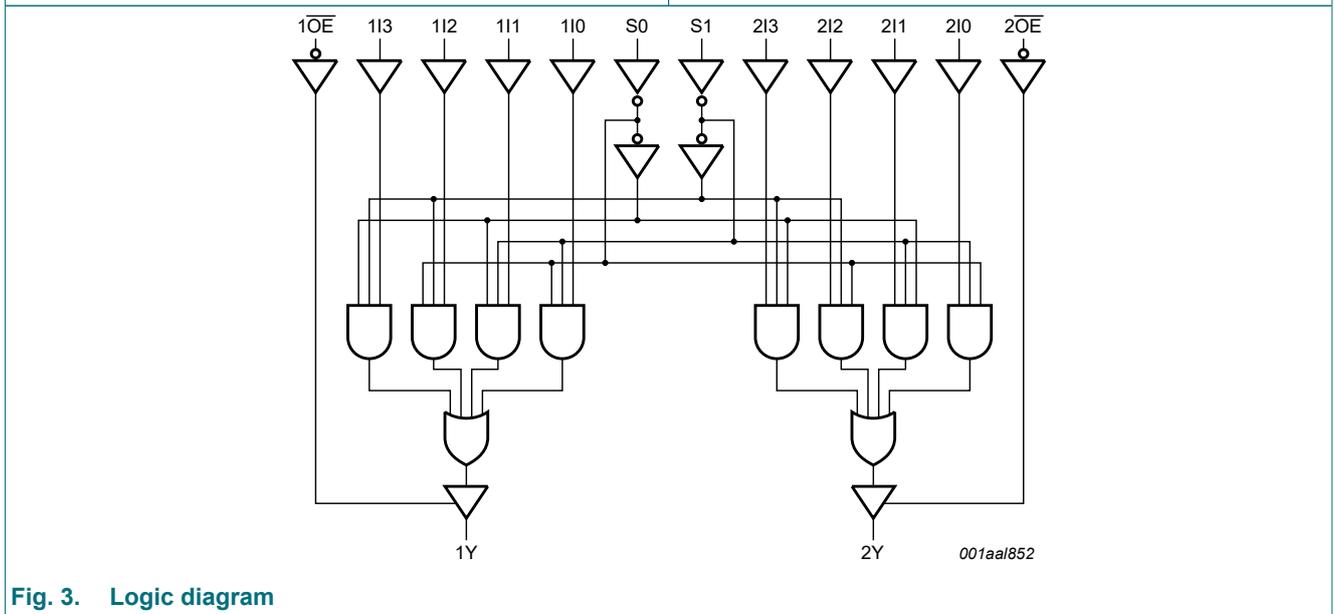
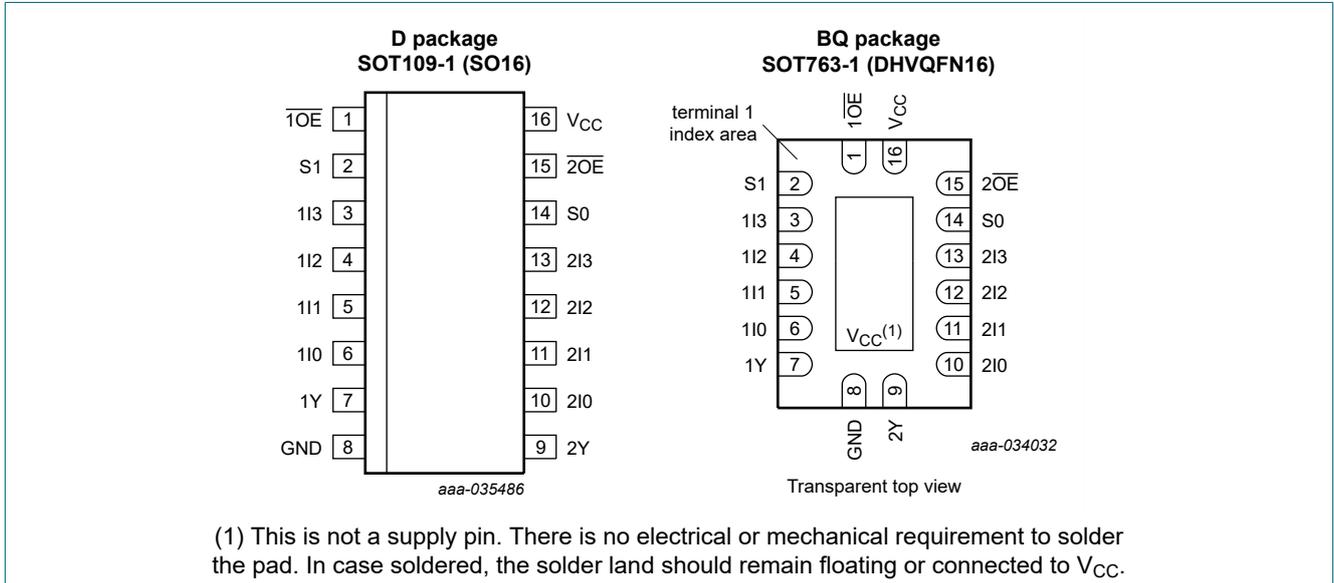


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1 \overline{OE} , 2 \overline{OE}	1, 15	output enable inputs (active LOW)
S0, S1	14, 2	data select inputs
110, 111, 112, 113	6, 5, 4, 3	data inputs source 1
1Y	7	multiplexer output source 1
GND	8	ground (0 V)
2Y	9	multiplexer output source 2
210, 211, 212, 213	10, 11, 12, 13	data inputs source 2
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

select Inputs		data inputs				output enable	output
S0	S1	nI0	nI1	nI2	nI3	nOE	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 50	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	± 35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC253-Q100			74HCT253-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC253-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -6.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -7.8 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 7.8 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT253-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 6.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.5	-	±5.0	-	±10	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A								
		per input pin; 1In, 2In inputs	-	40	144	-	180	-	196	µA
		per input pin; $\overline{\text{noE}}$ input	-	110	396	-	495	-	539	µA
		per input pin; Sn input	-	110	396	-	495	-	539	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

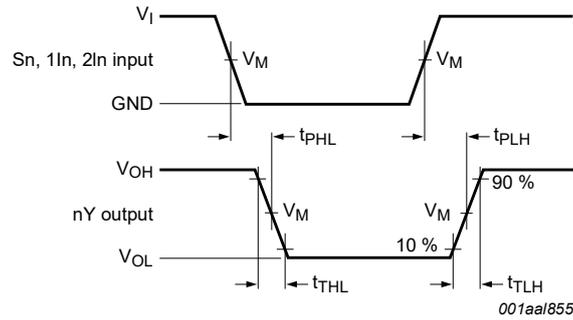
Voltages are referenced to GND (ground = 0 V); For test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
74HC253-Q100							
t_{pd}	propagation delay	1In to 1Y or 2In to 2Y; see Fig. 4 [1]					
		$V_{CC} = 2.0\text{ V}$	55	175	220	265	ns
		$V_{CC} = 4.5\text{ V}$	20	35	44	53	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	17	-	-	-	ns
		$V_{CC} = 6.0\text{ V}$	16	30	37	45	ns
		Sn to nY; see Fig. 4					
		$V_{CC} = 2.0\text{ V}$	58	175	220	265	ns
		$V_{CC} = 4.5\text{ V}$	21	35	44	53	ns
		$V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$	18	-	-	-	ns
	$V_{CC} = 6.0\text{ V}$	17	30	37	45	ns	
t_{en}	enable time	n \overline{OE} to nY; see Fig. 5 [2]					
		$V_{CC} = 2.0\text{ V}$	30	100	125	150	ns
		$V_{CC} = 4.5\text{ V}$	11	20	25	30	ns
		$V_{CC} = 6.0\text{ V}$	9	17	21	26	ns
t_{dis}	disable time	n \overline{OE} to nY; see Fig. 5 [3]					
		$V_{CC} = 2.0\text{ V}$	41	150	190	225	ns
		$V_{CC} = 4.5\text{ V}$	15	30	38	45	ns
		$V_{CC} = 6.0\text{ V}$	12	26	33	38	ns
t_t	transition time	see Fig. 4 [4]					
		$V_{CC} = 2.0\text{ V}$	14	60	75	90	ns
		$V_{CC} = 4.5\text{ V}$	5	12	15	18	ns
		$V_{CC} = 6.0\text{ V}$	4	10	13	15	ns
C_{PD}	power dissipation capacitance	per multiplexer; $V_I = \text{GND to } V_{CC}$ [5]	55	-	-	-	pF

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
74HCT253-Q100							
t _{pd}	propagation delay	1In to 1Y or 2In to 2Y; see Fig. 4 [1]					
		V _{CC} = 4.5 V	20	38	48	57	ns
		V _{CC} = 5.0 V; C _L = 15 pF	17	-	-	-	ns
		Sn to nY; see Fig. 4					
		V _{CC} = 4.5 V	22	40	50	60	ns
	V _{CC} = 5.0 V; C _L = 15 pF	19	-	-	-	ns	
t _{en}	enable time	n \overline{OE} to nY; V _{CC} = 4.5 V; see Fig. 5 [2]	14	30	38	45	ns
t _{dis}	disable time	n \overline{OE} to nY; V _{CC} = 4.5 V; see Fig. 5 [3]	13	30	38	45	ns
t _t	transition time	V _{CC} = 4.5 V; see Fig. 4	5	12	15	18	ns
C _{PD}	power dissipation capacitance	per multiplexer; V _I = GND to V _{CC} - 1.5 V [5]	55	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL}, t_{PLH}.
- [2] t_{en} is the same as t_{PZH}, t_{PZL}.
- [3] t_{dis} is the same as t_{PHZ}, t_{PLZ}.
- [4] t_t is the same as t_{THL}, t_{TLH}.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

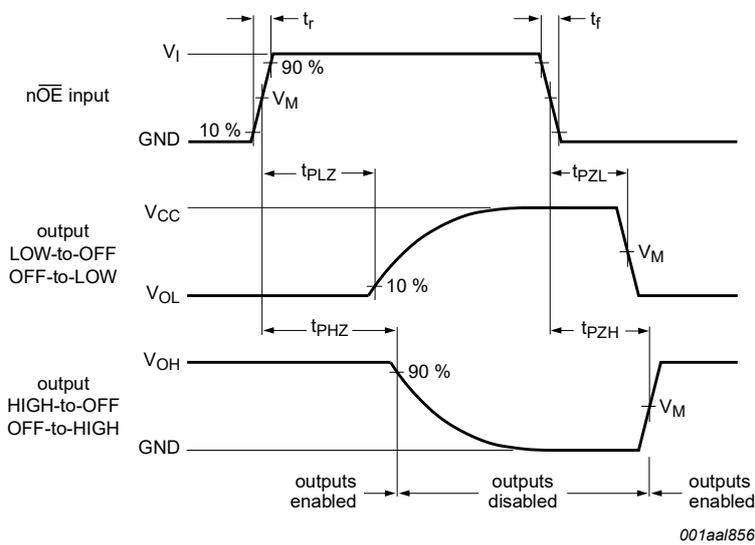
11.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Propagation delays input (S_n , 1In, 2In) to output (nY) and output (nY) transition times



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. 3-state output enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC253-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT253-Q100	1.3 V	1.3 V

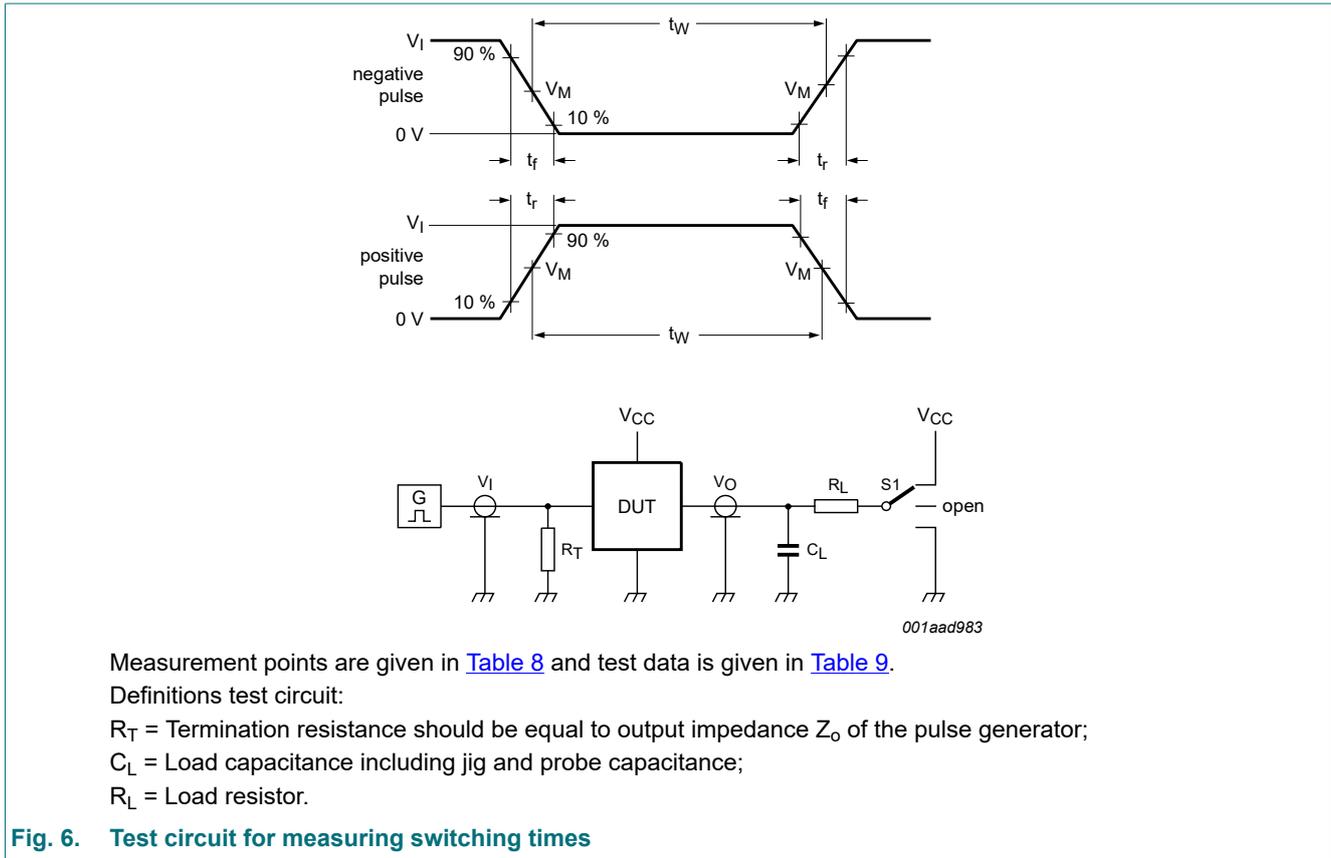


Table 9. Test data

Type	Input		Load		Switch position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC253-Q100	V_{CC}	6 ns	50 pF	1 k Ω	open	GND	V_{CC}
74HCT253-Q100	3 V	6 ns	50 pF	1 k Ω	open	GND	V_{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

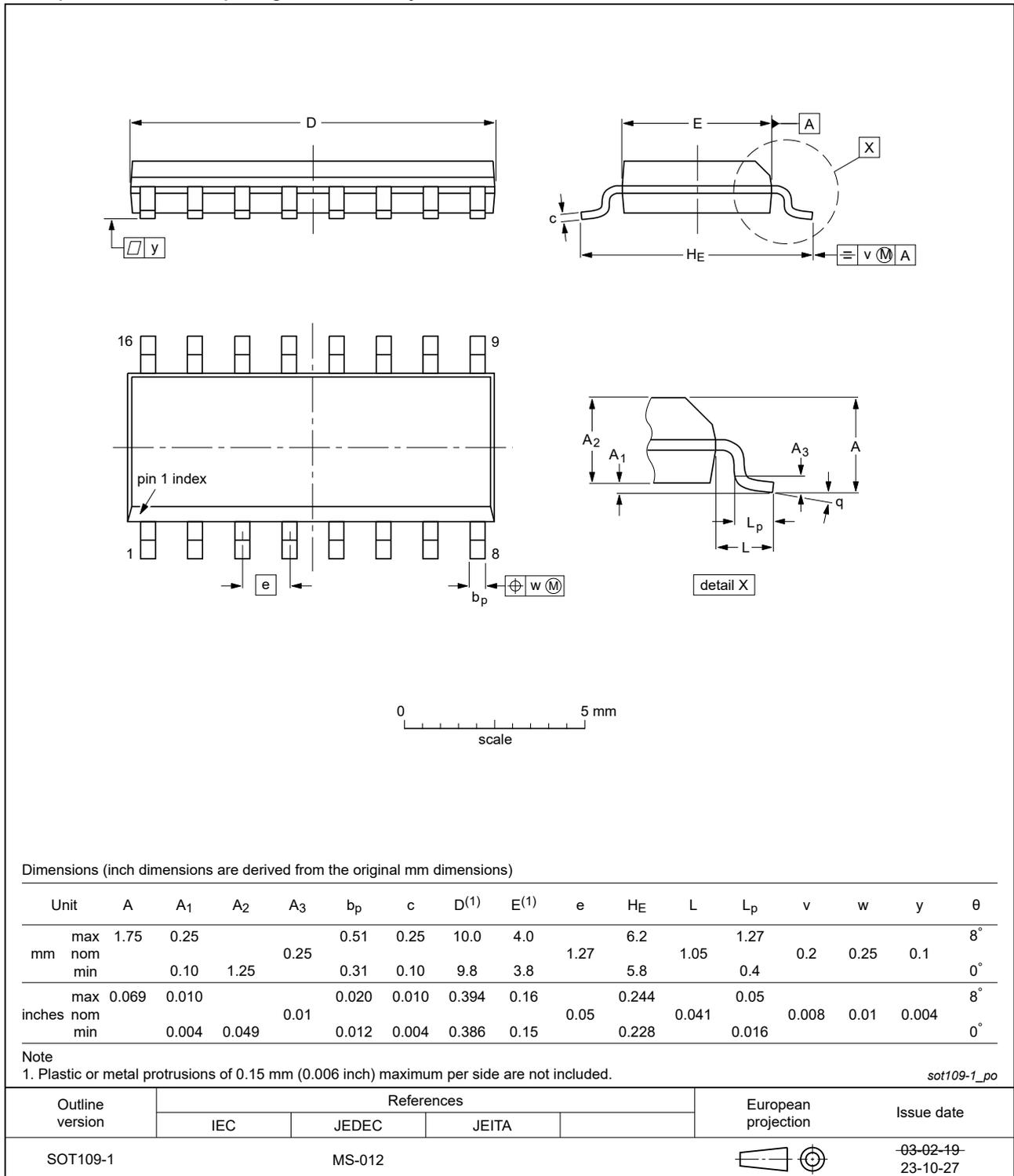


Fig. 7. Package outline SOT109-1 (SO16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

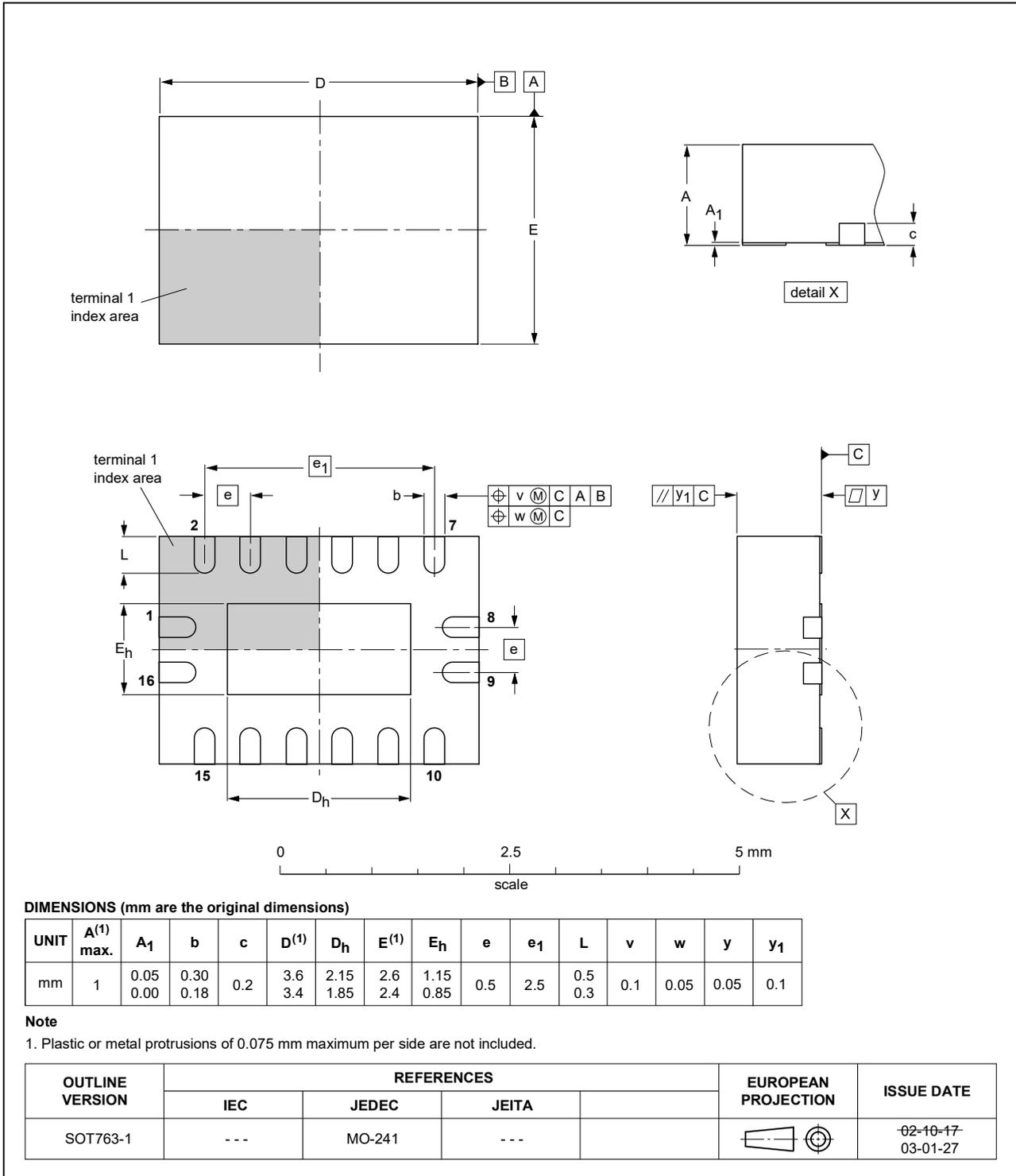


Fig. 8. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT253_Q100 v.5	20240311	Product data sheet	-	74HC_HCT253_Q100 v.4
Modifications:	<ul style="list-style-type: none"> • Fig. 7: Aligned SO package outline drawing to JEDEC MS-012. • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC_HCT253_Q100 v.4	20220927	Product data sheet	-	74HC_HCT253_Q100 v.3
Modifications:	<ul style="list-style-type: none"> • Type number 74HC253BQ-Q100 (SOT763-1/DHVQFN16) added. 			
74HC_HCT253_Q100 v.3	20210816	Product data sheet	-	74HC_HCT253_Q100 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation updated. • Section 10: IOZ conditions for 74HCT253-Q100 corrected. (Errata) 			
74HC_HCT253_Q100 v.2	20150121	Product data sheet	-	74HC_HCT253_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • Section 11: Power dissipation capacitance condition for 74HCT253-Q100 is corrected. 			
74HC_HCT253_Q100 v.1	20120717	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description	1
2. Features and benefits	1
3. Applications	1
4. Ordering information	2
5. Functional diagram	2
6. Pinning information	3
6.1. Pinning.....	3
6.2. Pin description.....	3
7. Functional description	4
8. Limiting values	4
9. Recommended operating conditions	5
10. Static characteristics	5
11. Dynamic characteristics	7
11.1. Waveforms and test circuit.....	9
12. Package outline	11
13. Abbreviations	13
14. Revision history	13
15. Legal information	14

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