74LV4066

Quad bilateral switches

Rev. 6 — 8 April 2024 Product data sheet

1. General description

The 74LV4066 is a quad single pole, single throw analog switch. Each switch features two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off. Digital inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC}.

2. Features and benefits

- Wide supply voltage range from 1.0 to 6.0 V
- CMOS low power dissipation
- Direct interface with TTL levels
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- Typical V_{OLP} (output ground bounce): < 0.8 V at V_{CC} = 3.3 V and T_{amb} = 25 °C
- Very low ON-resistance:
  - 60 Ω (typical) at V_{CC} = 2.0 V
  - 35 Ω (typical) at V_{CC} = 3.0 V
  - 25 Ω (typical) at V_{CC} = 4.5 V
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +80 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4066D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV4066PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

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4. Functional diagram

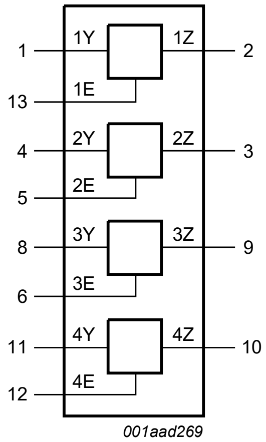


Fig. 1. Logic symbol

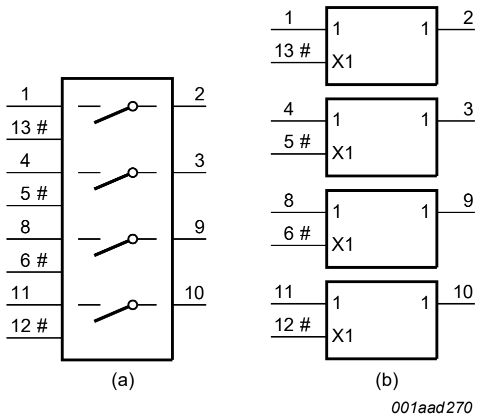


Fig. 2. IEC logic diagram

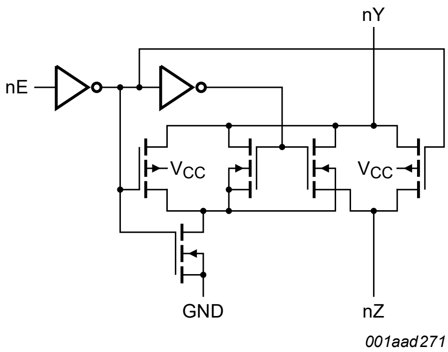
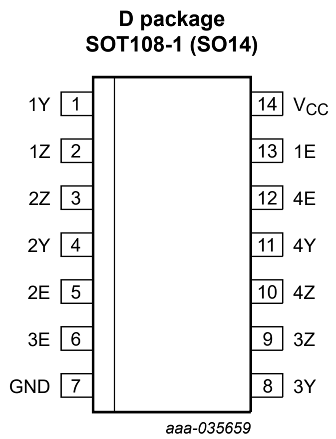
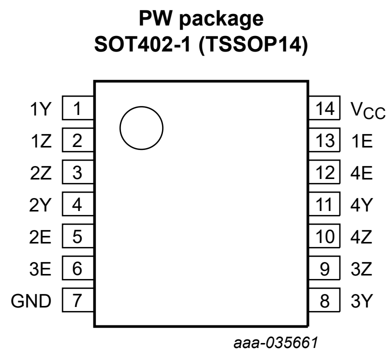


Fig. 3. Logic diagram (one switch)

5. Pinning information

5.1. Pinning





5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 8, 11	independent input or output
1Z, 2Z, 3Z, 4Z	2, 3, 9, 10	independent output or input
GND	7	ground (0 V)
1E, 2E, 3E, 4E	13, 5, 6, 12	enable input
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

Input nE	Switch
LOW	off
HIGH	on

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V	-	±50	mA
I_{SW}	switch current	V_O = -0.5 V to (V_{CC} + 0.5 V) [1]	-	±25	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V, but LV devices are guaranteed to function down to V_{CC} = 1.0 V (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.90	-	-	V
		V_{CC} = 2.0 V	1.40	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.00	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.20	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.30	V
		V_{CC} = 2.0 V	-	-	0.60	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.80	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	V
I_I	input leakage current	$V_I = V_{CC}$ or GND				
		V_{CC} = 3.6 V	-	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_I = V_{IH}$ or V_{IL}; see Fig. 4				
		V_{CC} = 3.6 V	-	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	μA
$I_{S(ON)}$	ON-state leakage current	$V_I = V_{IH}$ or V_{IL}; see Fig. 5				
		V_{CC} = 3.6 V	-	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A				
		V_{CC} = 3.6 V	-	-	20	μA
		V_{CC} = 6.0 V	-	-	40	μA
ΔI_{CC}	additional supply current	per input; $V_I = V_{CC}$ - 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	500	μA
C_I	input capacitance		-	3.5	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.90	-	-	V
		V_{CC} = 2.0 V	1.40	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.00	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.20			V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.30	V
		V_{CC} = 2.0 V	-	-	0.60	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.80	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.80	V
I_I	input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 3.6 V	-	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_I = V_{IH} or V_{IL}; see Fig. 4				
		V_{CC} = 3.6 V	-	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	μA
$I_{S(ON)}$	ON-state leakage current	V_I = V_{IH} or V_{IL}; see Fig. 5				
		V_{CC} = 3.6 V	-	-	1.0	μA
		V_{CC} = 6.0 V	-	-	2.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A				
		V_{CC} = 3.6 V	-	-	40	μA
		V_{CC} = 6.0 V	-	-	80	μA
ΔI_{CC}	additional supply current	per input; V_I = V_{CC} - 0.6 V; V_{CC} = 2.7 V to 3.6 V	-	-	850	μA

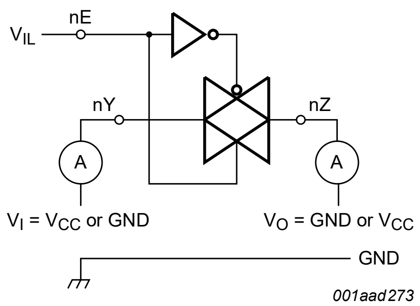


Fig. 4. Test circuit for measuring OFF-state leakage current

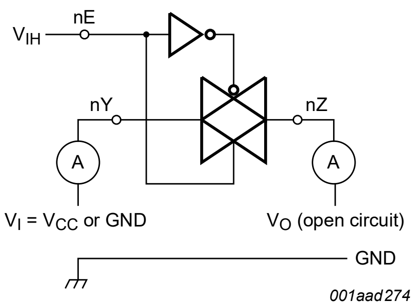


Fig. 5. Test circuit for measuring ON-state leakage current

Table 7. ON-resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C; see Fig. 7							
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 1.2 V	[2]	-	300	-	Ω
		V_{CC} = 2.0 V		-	60	130	Ω
		V_{CC} = 2.7 V		-	41	60	Ω
		V_{CC} = 3.0 V to 3.6 V		-	37	72	Ω
		V_{CC} = 4.5 V		-	25	52	Ω
		V_{CC} = 6.0 V		-	23	47	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_I = V_{IH}$ or V_{IL}; V_{is} = GND					
		V_{CC} = 1.2 V	[2]	-	75	-	Ω
		V_{CC} = 2.0 V		-	35	98	Ω
		V_{CC} = 2.7 V		-	26	60	Ω
		V_{CC} = 3.0 V to 3.6 V		-	24	52	Ω
		V_{CC} = 4.5 V		-	15	40	Ω
		V_{CC} = 6.0 V		-	13	35	Ω
		$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$					
		V_{CC} = 1.2 V	[2]	-	75	-	Ω
		V_{CC} = 2.0 V		-	40	110	Ω
		V_{CC} = 2.7 V		-	35	72	Ω
		V_{CC} = 3.0 V to 3.6 V		-	30	65	Ω
		V_{CC} = 4.5 V		-	22	47	Ω
		V_{CC} = 6.0 V		-	20	40	Ω
$R_{ON(flat)}$	ON resistance (flatness)	$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$					
		V_{CC} = 2.0 V		-	5	-	Ω
		V_{CC} = 2.7 V		-	4	-	Ω
		V_{CC} = 3.0 V to 3.6 V		-	4	-	Ω
		V_{CC} = 4.5 V		-	3	-	Ω
		V_{CC} = 6.0 V		-	2	-	Ω

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
$R_{ON(peak)}$	ON resistance (peak)	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V	-	-	150	Ω
		V_{CC} = 2.7 V	-	-	90	Ω
		V_{CC} = 3.0 V to 3.6 V	-	-	83	Ω
		V_{CC} = 4.5 V	-	-	60	Ω
		V_{CC} = 6.0 V	-	-	54	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_I = V_{IH}$ or V_{IL}; V_{is} = GND				
		V_{CC} = 2.0 V	-	-	115	Ω
		V_{CC} = 2.7 V	-	-	68	Ω
		V_{CC} = 3.0 V to 3.6 V	-	-	60	Ω
		V_{CC} = 4.5 V	-	-	45	Ω
		V_{CC} = 6.0 V	-	-	40	Ω
		$V_I = V_{IH}$ or V_{IL}; $V_{is} = V_{CC}$				
		V_{CC} = 2.0 V	-	-	130	Ω
		V_{CC} = 2.7 V	-	-	85	Ω
		V_{CC} = 3.0 V to 3.6 V	-	-	75	Ω
		V_{CC} = 4.5 V	-	-	55	Ω
		V_{CC} = 6.0 V	-	-	47	Ω

[1] All typical values are measured at T_{amb} = 25 °C.
[2] At supply voltage approaching 1.2 V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

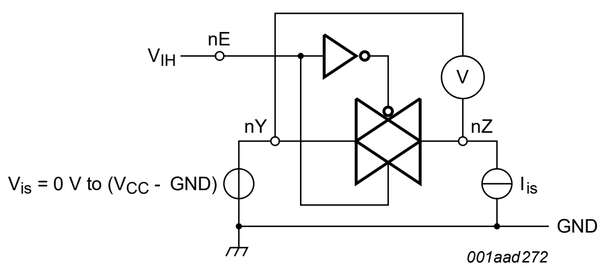


Fig. 6. Test circuit for measuring ON resistance

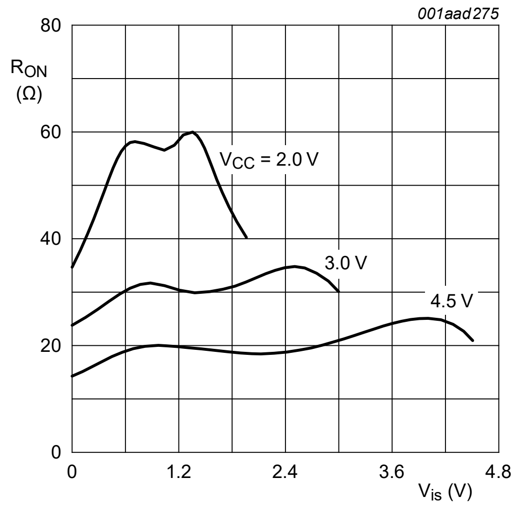


Fig. 7. ON resistance as a function of input voltage

10. Dynamic characteristics

Table 8. Dynamic characteristics

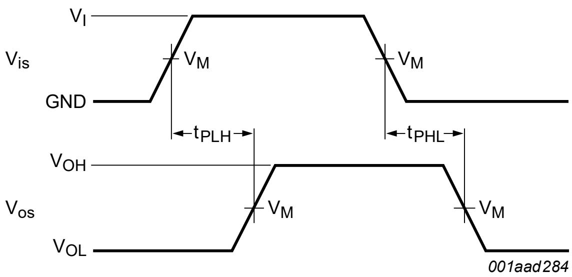
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C							
t_{pd}	propagation delay	V_{is} to V_{os}; see Fig. 8	[2]				
		V_{CC} = 1.2 V		-	8	-	ns
		V_{CC} = 2.0 V		-	5	26	ns
		V_{CC} = 2.7 V to 3.6 V		-	3	15	ns
		V_{CC} = 4.5 V		-	2	13	ns
		V_{CC} = 6.0 V		-	2	10	ns
t_{on}	turn-on time	nE to V_{os}; see Fig. 9	[3]				
		V_{CC} = 1.2 V		-	40	-	ns
		V_{CC} = 2.0 V		-	22	43	ns
		V_{CC} = 2.7 V to 3.6 V		-	12	25	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	10	-	ns
		V_{CC} = 4.5 V		-	10	21	ns
		V_{CC} = 6.0 V		-	8	16	ns
t_{off}	turn-off time	nE to V_{os}; see Fig. 9	[4]				
		V_{CC} = 1.2 V		-	50	-	ns
		V_{CC} = 2.0 V		-	27	65	ns
		V_{CC} = 2.7 V to 3.6 V		-	15	38	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	13	-	ns
		V_{CC} = 4.5 V		-	13	32	ns
		V_{CC} = 6.0 V		-	12	28	ns
C_{PD}	power dissipation capacitance	per switch; V_{CC} = 3.3 V; V_I = GND to V_{CC}; C_L = 15 pF	[5]	-	11	-	pF

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +125 °C						
t_{pd}	propagation delay	V_{is} to V_{os}; see Fig. 8 [2]				
		V_{CC} = 2.0 V	-	-	31	ns
		V_{CC} = 2.7 V to 3.6 V	-	-	18	ns
		V_{CC} = 4.5 V	-	-	15	ns
		V_{CC} = 6.0 V	-	-	12	ns
t_{on}	turn-on time	nE to V_{os}; see Fig. 9 [3]				
		V_{CC} = 2.0 V	-	-	51	ns
		V_{CC} = 2.7 V to 3.6 V	-	-	30	ns
		V_{CC} = 4.5 V	-	-	26	ns
		V_{CC} = 6.0 V	-	-	20	ns
t_{off}	turn-off time	nE to V_{os}; see Fig. 9 [4]				
		V_{CC} = 2.0 V	-	-	81	ns
		V_{CC} = 2.7 V to 3.6 V	-	-	47	ns
		V_{CC} = 4.5 V	-	-	40	ns
		V_{CC} = 6.0 V	-	-	34	ns

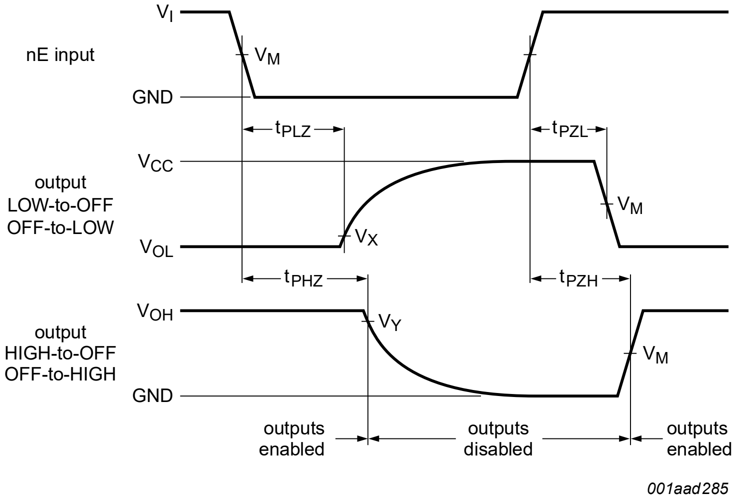
[1] Typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] t_{on} is the same as t_{PZH} and t_{PZL}.
[4] t_{off} is the same as t_{PHZ} and t_{PLZ}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
C_S = maximum switch capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma[(C_L + C_S) \times V_{CC}^2 \times f_o]$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Input to output propagation delays



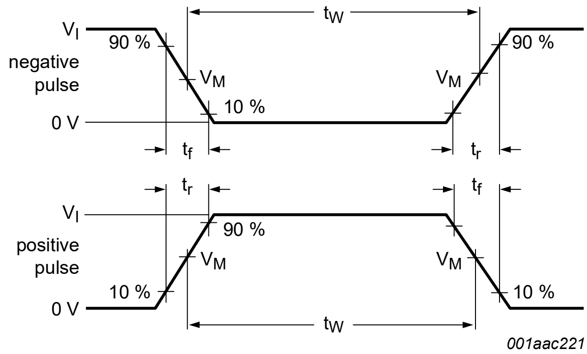
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

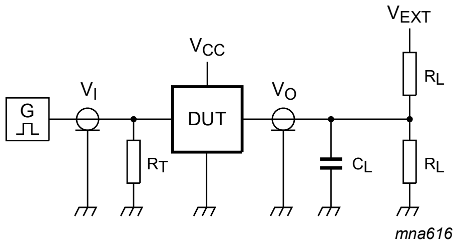
Fig. 9. Turn-on and turn-off times for the inputs to the output

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15	V_{OH} - 0.15 V
≥ 2.7 V	1.5 V	1.5 V	V_{OL} + 0.3	V_{OH} - 0.3 V



a. Input pulse definition



Test data is given in Table 10.
Definitions test circuit:
R_L = Load resistance;
C_L = Load capacitance includes jig and probe capacitance;
R_T = Termination resistance should be equal to Z_o of the pulse generator;
V_{EXT} = Test voltage for switching times.
Test circuit

Fig. 10. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L [1]	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	GND	2 x V_{CC}	open
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	1 kΩ	GND	2 x V_{CC}	open
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 kΩ	GND	2 x V_{CC}	open

[1] $R_L = \infty$ Ω for measuring the propagation delays t_{PLH} and t_{PHL}.

10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

Voltages are referenced to GND (ground = 0 V);
V_{is} is the input voltage at pin nY or nZ, whichever is assigned as an input;
V_{os} is the output voltage at pin nY or nZ, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
d_{sin}	sine-wave distortion	R_L = 10 kΩ; f = 1 kHz; C_L = 50 pF; see Fig. 11				
		V_{CC} = 3.0 V; V_{is} = 2.75 V (p-p)	-	0.04	-	%
		V_{CC} = 6.0 V; V_{is} = 5.50 V (p-p)	-	0.02	-	%
		R_L = 10 kΩ; f = 10 kHz; C_L = 50 pF; see Fig. 11				
		V_{CC} = 3.0 V; V_{is} = 2.75 V (p-p)	-	0.12	-	%
		V_{CC} = 6.0 V; V_{is} = 5.50 V (p-p)	-	0.06	-	%
$\alpha_{OFF(feedthru)}$	switch OFF-state signal feed-through attenuation	R_L = 600 kΩ; f = 1 MHz; C_L = 50 pF; see Fig. 12 and Fig. 13 [1]				
		V_{CC} = 3.0 V	-	-50	-	dB
		V_{CC} = 6.0 V	-	-50	-	dB
$\alpha_{ct(S)}$	crosstalk between switches	R_L = 600 kΩ; f = 1 MHz; C_L = 50 pF; see Fig. 14 [1]				
		V_{CC} = 3.0 V	-	-60	-	dB
		V_{CC} = 6.0 V	-	-60	-	dB
$V_{ct(pp)}$	crosstalk voltage between enable input to any switch (peak-to-peak value)	R_L = 600 kΩ; f = 1 MHz; C_L = 50 pF; see Fig. 15 and Fig. 16 [2]				
		V_{CC} = 3.0 V	-	110	-	mV
		V_{CC} = 6.0 V	-	220	-	mV
f_{max}	minimum frequency response (-3 dB)	R_L = 50 kΩ; C_L = 50 pF; see Fig. 17 and Fig. 18 [3]				
		V_{CC} = 3.0 V	-	180	-	MHz
		V_{CC} = 6.0 V	-	200	-	MHz
C_S	maximum switch capacitance		-	8	-	pF

[1] Adjust input voltage V_{is} is 0 dBm level (0 dBm = 1 mW into 600 Ω).
[2] Pin nE: square wave between V_{CC} and GND, t_r = t_f = 6 ns.
[3] Adjust input voltage V_{is} is 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

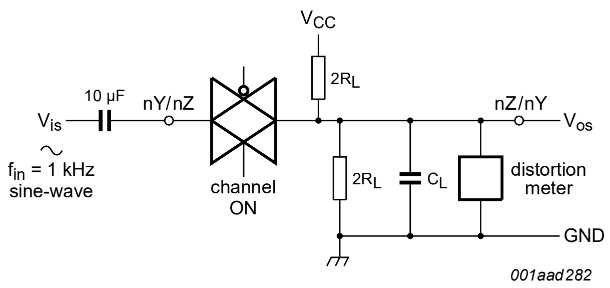


Fig. 11. Test circuit for measuring sine-wave distortion

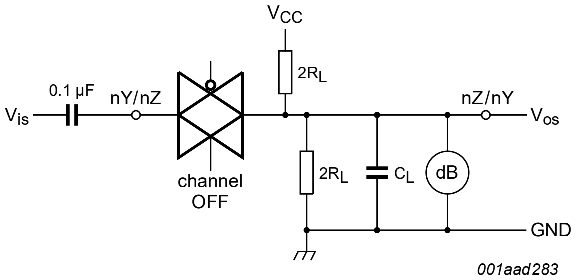
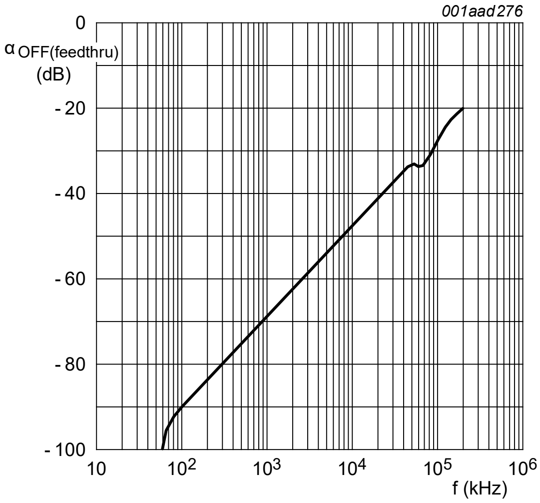
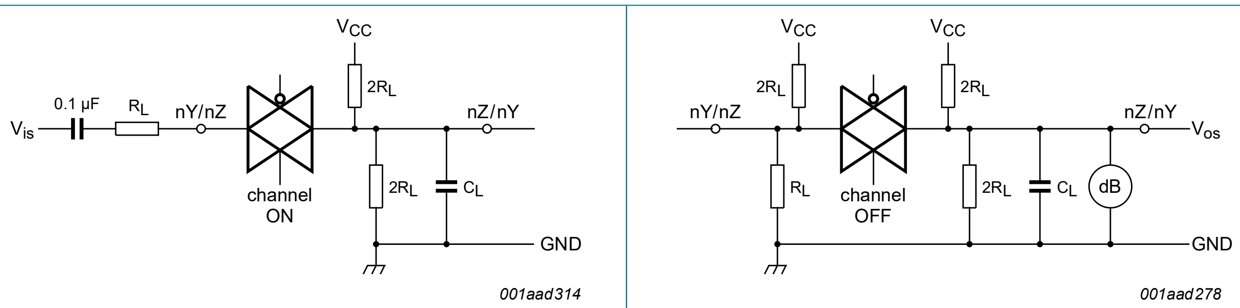


Fig. 12. Test circuit for measuring switch OFF-state signal feed-through



V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω;
R_{SOURCE} = 1 kΩ

Fig. 13. Switch OFF-state signal feed-through as a function of frequency



a. Channel ON condition

b. Channel OFF condition

Fig. 14. Test circuit for measuring crosstalk between switches

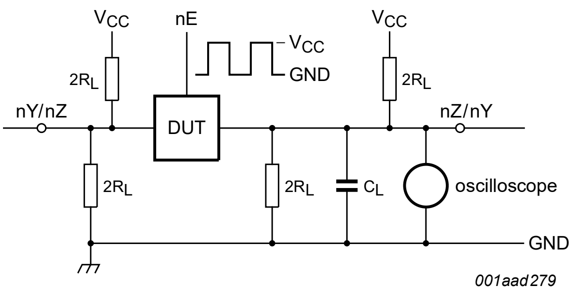


Fig. 15. Test circuit for measuring crosstalk between enable and any switch

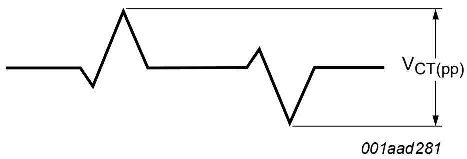


Fig. 16. Crosstalk definition (oscilloscope output)

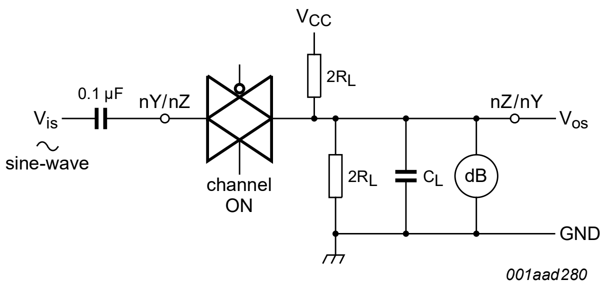
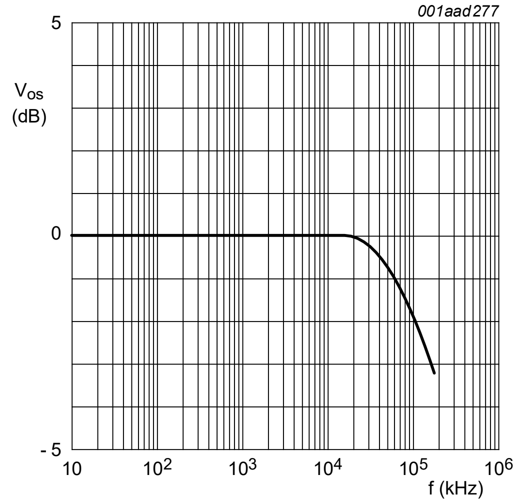


Fig. 17. Test circuit for measuring minimum frequency response

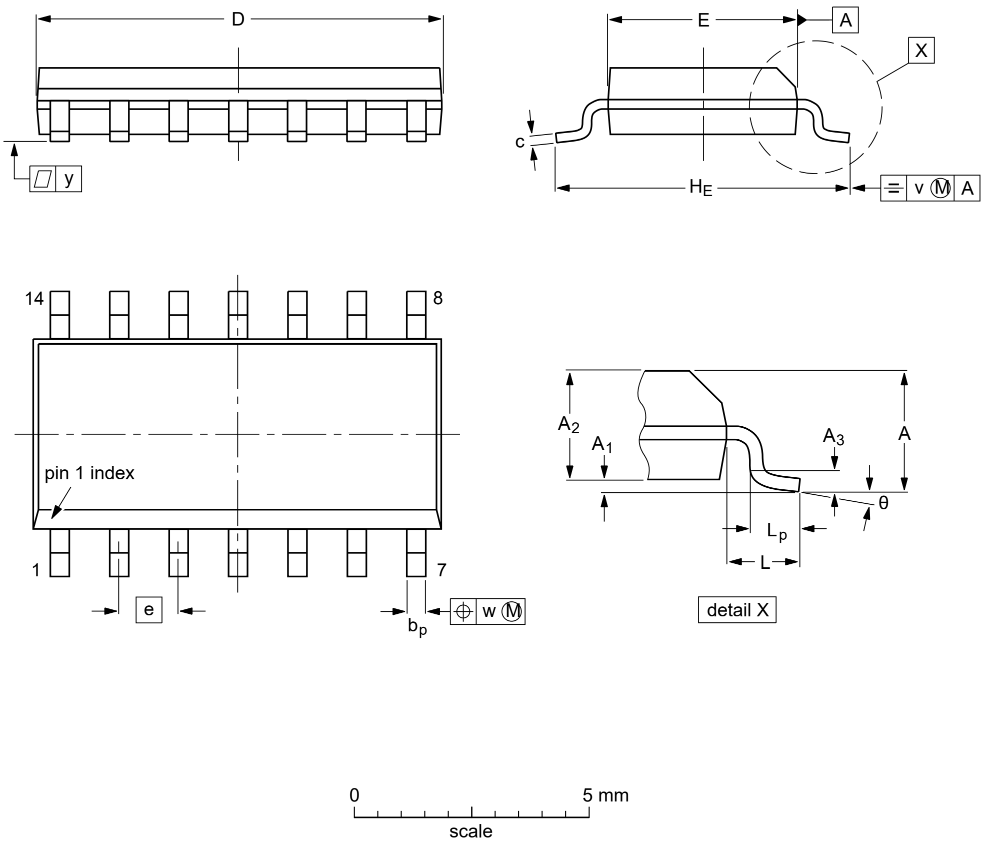


V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω; R_{SOURCE} = 1 kΩ

Fig. 18. Frequency response

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

Note

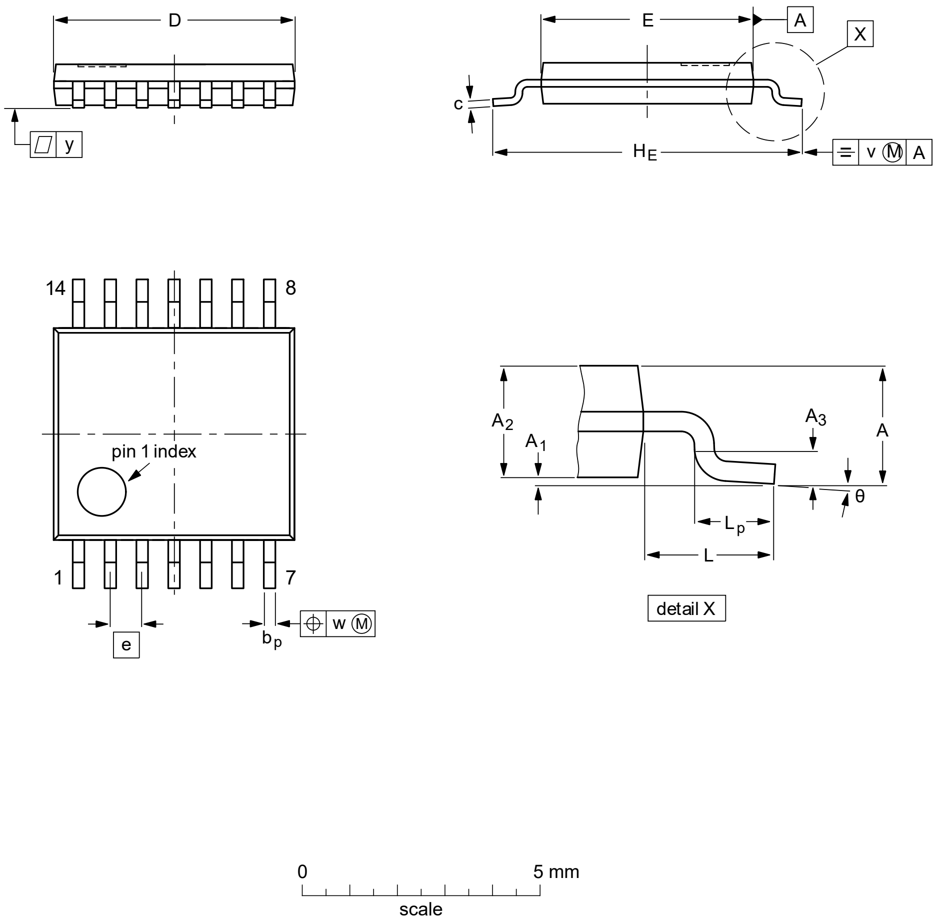
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 19. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 20. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4066 v.6	20240408	Product data sheet	-	74LV4066 v.5
Modifications:	• Fig. 19, Fig. 20: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard. • Type number 74LV4066DB (SOT337-1/SSOP14) removed.			
74LV4066 v.5	20221024	Product data sheet	-	74LV4066 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 5.1 updated. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74LV4066 v.4	20151209	Product data sheet	-	74LV4066 v.3
Modifications:	• Type number 74LV4066N (SOT27-1) removed.			Modifications:
74LV4066 v.3	20050704	Product data sheet	-	74LV4066 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Table 1: corrected package names.			
74LV4066 v.2	19980623	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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