74LVT2241

3.3 V octal buffer/line driver with 30 Ω series termination resistors; 3-state

Rev. 4 — 8 July 2024 Product data sheet

1. General description

The 74LVT2241 is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables (1$\overline{OE}$ and 2OE), each controlling four of the 3-state outputs. A HIGH on 1$\overline{OE}$ or a LOW on 2OE causes the associated outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs.

2. Features and benefits

- Octal bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 V to 3.6 V
- BiCMOS high speed and output drive
- Output capability: +12 mA/–12 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Outputs include series resistance of 30 Ω making external termination resistors unnecessary
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT2241D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT2241PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

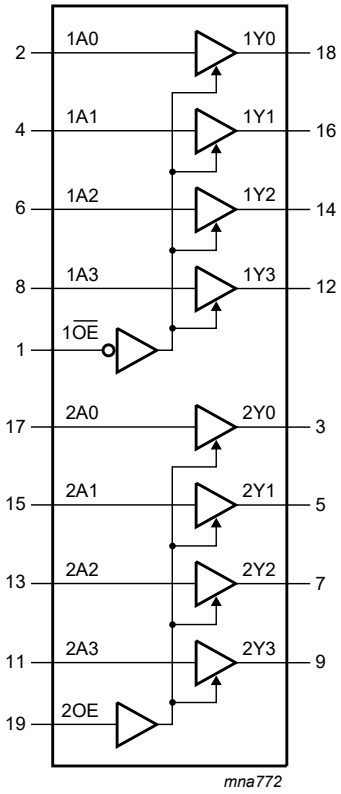


Fig. 1. Logic symbol

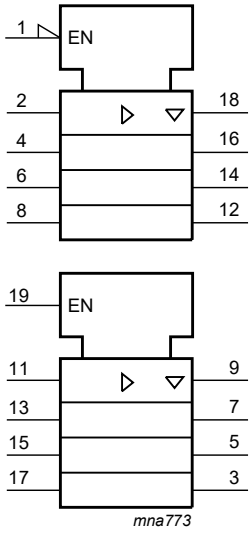


Fig. 2. IEC logic symbol

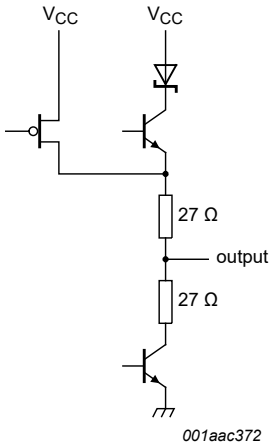
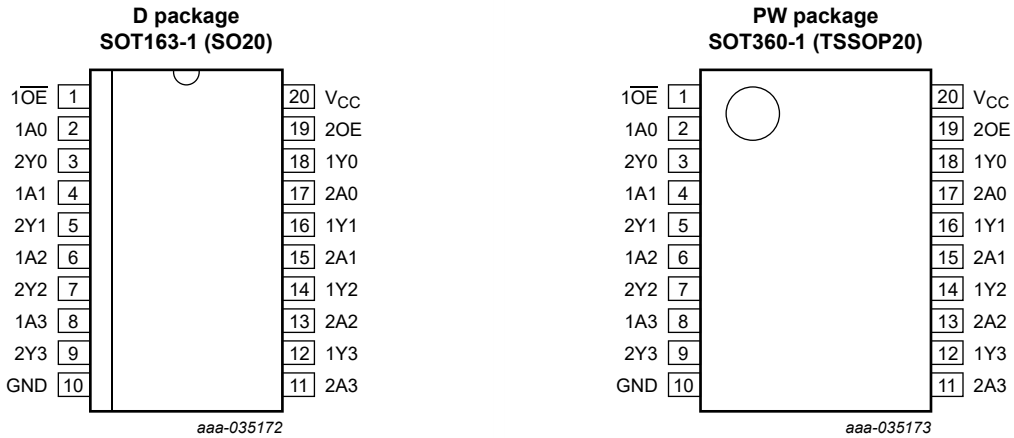


Fig. 3. Schematic of each output

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
GND	10	ground (0 V)
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
2OE	19	output enable input (active HIGH)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = High impedance "OFF" state.

Enable active LOW			Enable active HIGH		
Inputs		Outputs	Inputs		Outputs
$1\overline{OE}$	1An	1Yn	2OE	2An	2Yn
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF or HIGH state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW state	-	128	mA
		output in HIGH state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	+150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.7	3.6	V
V_I	input voltage		0	5.5	V
I_{OH}	HIGH-level output current		-12	-	mA
I_{OL}	LOW-level output current		-	12	mA
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V; I_{OH} = -12 mA	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_{OL} = 12 mA	-	-	0.8	V
I_I	input leakage current	all input pins				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	1	10	µA
		control pins				
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	±0.1	±1	µA
		data pins [2]				
		V_{CC} = 3.6 V; V_I = V_{CC}	-	0.1	1	µA
		V_{CC} = 3.6 V; V_I = 0 V	-5	-1	-	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	1	±100	µA
I_{BHL}	bus hold LOW current	V_{CC} = 3.0 V; V_I = 0.8 V	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 3.0 V; V_I = 2.0 V	-	-150	-75	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [3]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [3]	-	-	-500	µA
I_{EX}	external current	nYn output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 3.0 V	-	60	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; [4] V_I = GND or V_{CC}; $1\overline{OE}$, 2OE = don't care	-	±1	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_O = 3.0 V	-	1	5	µA
		V_{CC} = 3.6 V; V_O = 0.5 V	-5	-1	-	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A				
		outputs HIGH	-	0.12	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled [5]	-	0.12	0.19	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; [6] one input = V_{CC} - 0.6 V; other inputs at V_{CC} or GND	-	0.1	0.25	mA
C_I	input capacitance	V_I = 0 V or 3.0 V	-	4	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	-	8	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Unused pins at V_{CC} or GND.
[3] This is the bus hold overdrive current required to force the input to the opposite logic state.
[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 ms is permitted. This parameter is valid for T_{amb} = +25 °C only.
[5] I_{CC} with the outputs disabled is measured with outputs pulled to V_{CC} or GND.
[6] This is the increase in supply current for each input at V_{CC} - 0.6 V.

10. Dynamic characteristics

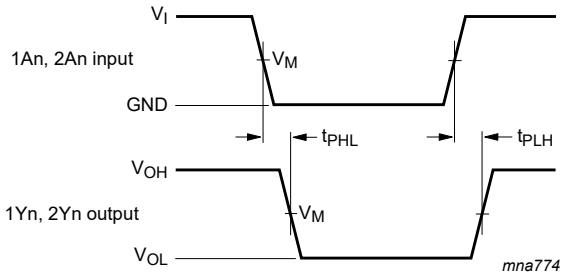
Table 7. Dynamic characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	1An to 1Yn, 2An to 2Yn; see Fig. 4				
		V_{CC} = 2.7 V	-	-	5.0	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.0	4.2	ns
t_{PHL}	HIGH to LOW propagation delay	1An to 1Yn, 2An to 2Yn; see Fig. 4				
		V_{CC} = 2.7 V	-	-	4.7	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.3	4.3	ns
t_{PZH}	OFF-state to HIGH propagation delay	$1\overline{OE}$ to 1Yn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	8.5	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	4.4	6.2	ns
		2OE to 2Yn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	7.9	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	4.4	6.2	ns
t_{PZL}	OFF-state to LOW propagation delay	$1\overline{OE}$ to 1Yn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	6.8	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	4.3	5.9	ns
		2OE to 2Yn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	6.2	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	4.1	5.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$1\overline{OE}$ to 1Yn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	5.2	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.4	5.0	ns
		2OE to 2Yn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	6.4	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.9	5.7	ns
t_{PLZ}	LOW to OFF-state propagation delay	$1\overline{OE}$ to 1Yn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	4.5	ns
		V_{CC} = 3.3 V ± 0.3 V	1.6	3.2	4.5	ns
		2OE to 2Yn; see Fig. 6				
		V_{CC} = 2.7 V	-	-	5.8	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.8	5.1	ns

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

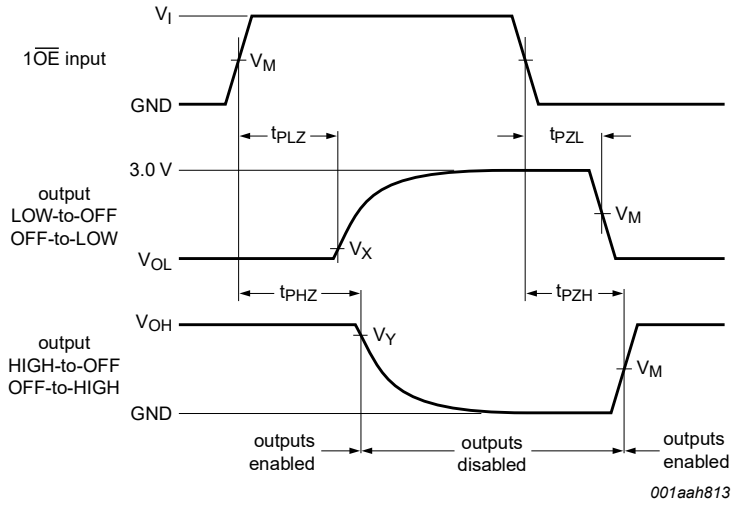
10.1. Waveforms and test circuit



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

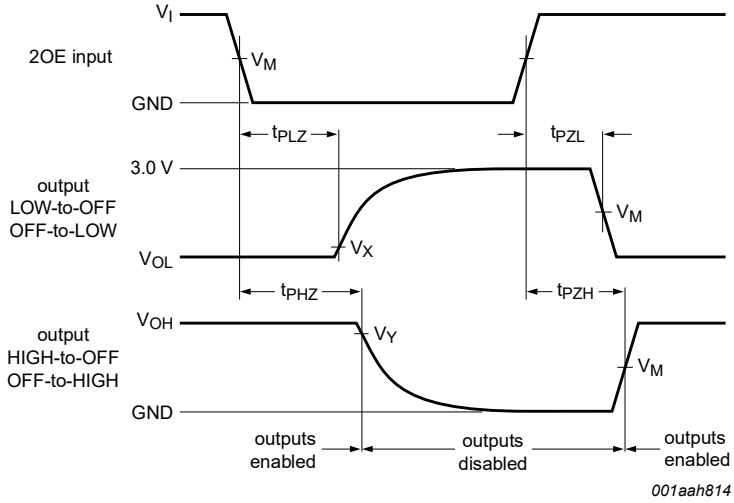
Fig. 4. Input (1An, 2An) to output (1Yn, 2Yn) propagation delays



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. 3-state output (1Yn) enable and disable times



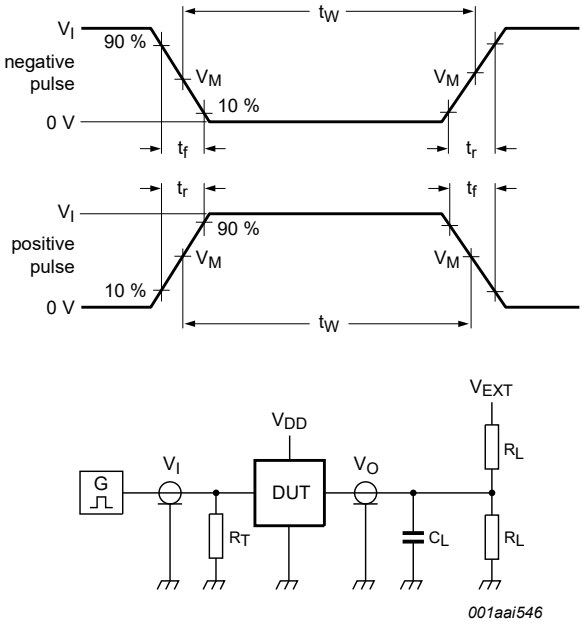
See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. 3-state output (2Yn) enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

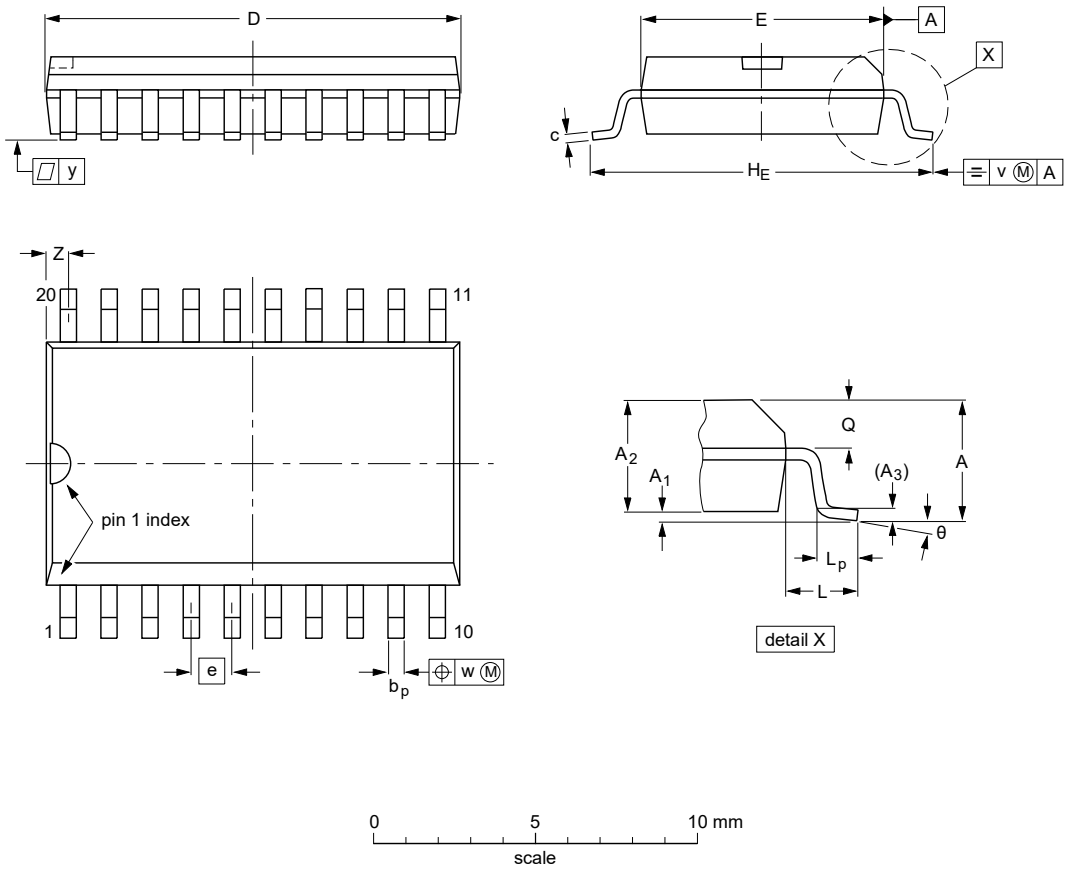
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

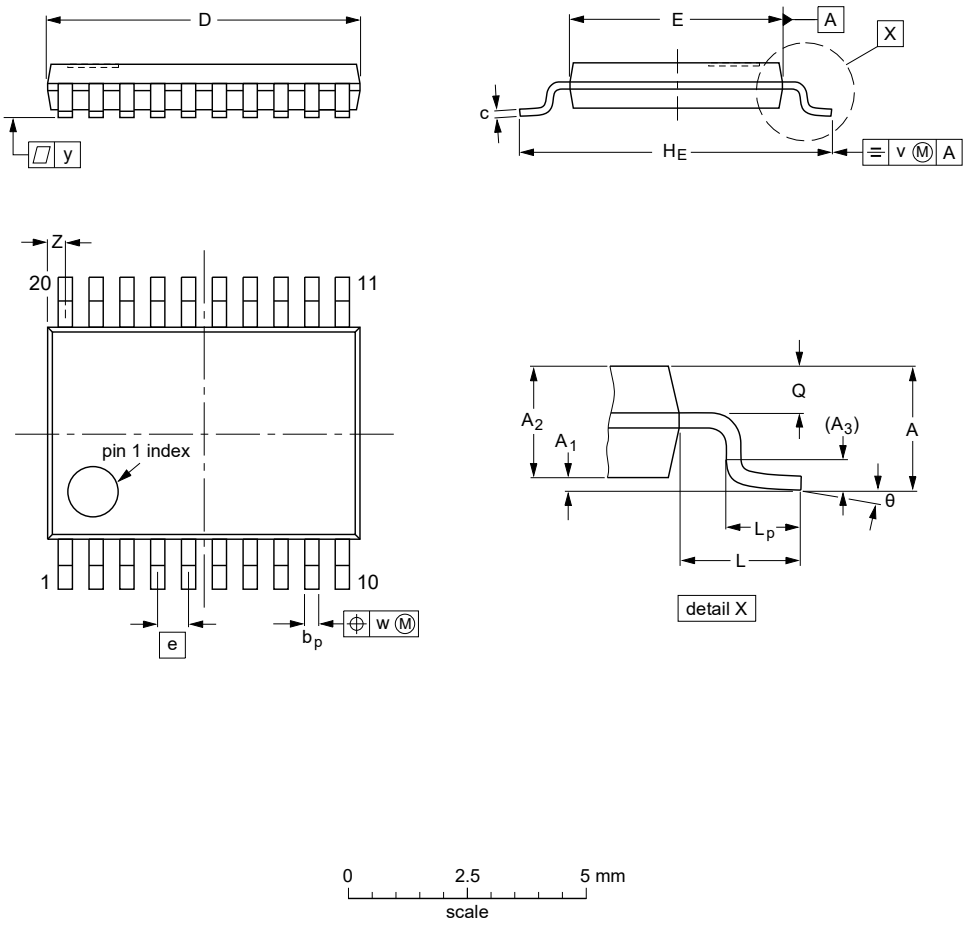
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 9. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT2241 v.4	20240708	Product data sheet	-	74LVT2241 v.3
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVT2241 v.3	20210217	Product data sheet	-	74LVT2241 v.2
Modifications:	• Type number 74LVT2241DB (SOT339-1 / SSOP20) removed. • Section 1 and Section 2 updated.			
74LVT2241 v.2	20180503	Product data sheet	-	74LVT2241 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LVT2241 v.1	19960529	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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