74LVT2245; 74LVTH2245

3.3 V octal transceiver with 30 Ω termination resistors; 3-state

Rev. 8 — 8 July 2024 Product data sheet

1. General description

The 74LVT2245; 74LVTH2245 is an 8-bit transceiver with 30 Ω termination resistors and 3-state outputs. The device features an output enable ($\overline{OE}$) and send/receive (DIR) for direction control. A HIGH on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

2. Features and benefits

- 30 Ω output termination resistors
- Octal bidirectional bus interface
- 3-state buffers
- Wide supply voltage range from 2.7 V to 3.6 V
- BiCMOS high speed and output drive
- Output capability: +12 mA and -12 mA
- TTL input and output switching levels
- Overvoltage tolerant inputs to 5.5 V
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Direct interface with TTL levels
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT2245D 74LVTH2245D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT2245PW 74LVTH2245PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

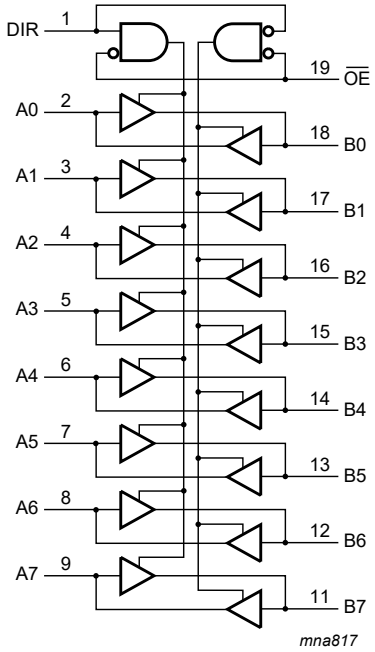


Fig. 1. Logic symbol

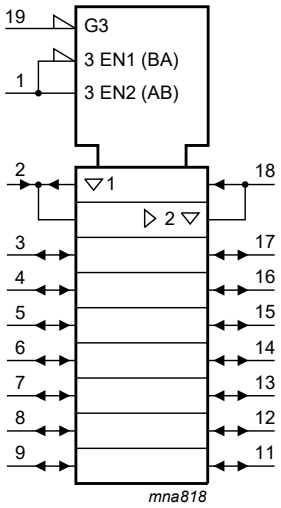


Fig. 2. IEC logic symbol

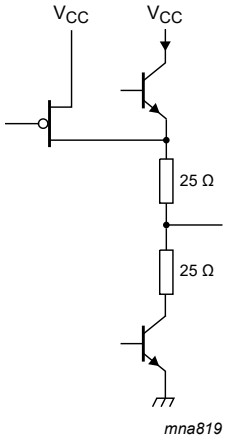
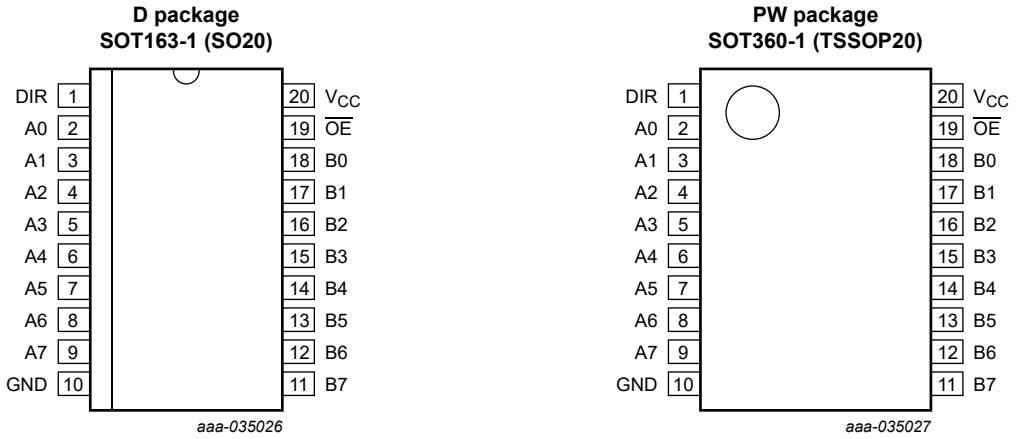


Fig. 3. Schematic of one output

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control input
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B7, B6, B5, B4, B3, B2, B1, B0	11, 12, 13, 14, 15, 16, 17, 18	data input/output
$\overline{OE}$	19	output enable input
V_{CC}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control		Input/output	
$\overline{OE}$	DIR	An	Bn
L	L	output An = Bn	input
L	H	input	output Bn = An
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	150	°C
P_{tot}	total power dissipation	T_{amb} = -40 to +85 °C		500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-12	-	-	mA
I_{OL}	LOW-level output current		-	-	12	mA
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V
T_{amb}	ambient temperature	in free-air	-40	+25	+85	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V; I_{OH} = -12 mA	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_{OL} = 12 mA	-	-	0.8	V
I_I	input leakage current	control pins				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	1	10	µA
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	±0.1	±1	µA
		I/O data pins; V_{CC} = 3.6 V [2]				
		V_I = 5.5 V	-	1	20	µA
		V_I = V_{CC}	-	0.1	1	µA
		V_I = 0 V	-	-1	-5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	1	±100	µA
I_{BHL}	bus hold LOW current	V_{CC} = 3 V; V_I = 0.8 V	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 3 V; V_I = 2.0 V	-	-150	-75	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [3]	-	-	500	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [3]	-500	-	-	µA
I_{CEX}	output high leakage current	output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 3.0 V	-	60	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = don't care [4]	-	15	±100	µA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	3	12	mA
		outputs disabled [5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} - 0.6 V; other inputs at V_{CC} or GND [6]	-	0.1	0.2	mA
C_I	input capacitance	DIR and $\overline{OE}$; V_I = 0 V or 3.0 V	-	4	-	pF
$C_{I/O}$	input/output capacitance	An and Bn; outputs disabled; $V_{I/O}$ = 0 V or 3.0 V	-	10	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
[2] Unused pins at V_{CC} or GND.
[3] This is the bus hold overdrive current required to force the input to the opposite logic state.
[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.0 V to 3.6 V a transition time of 100 µs is permitted.
[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

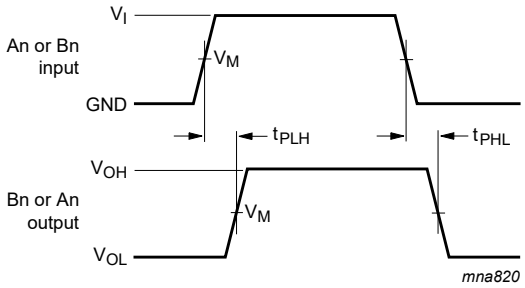
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An; see Fig. 4				
		V_{CC} = 2.7 V	-	-	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	4.6	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An; see Fig. 4				
		V_{CC} = 2.7 V	-	-	4.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.1	4.5	ns
t_{PZH}	OFF-state to HIGH propagation delay	see Fig. 5				
		V_{CC} = 2.7 V	-	-	9.1	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	4.5	7.0	ns
t_{PZL}	OFF-state to LOW propagation delay	see Fig. 5				
		V_{CC} = 2.7 V	-	-	7.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.5	4.3	6.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	see Fig. 5				
		V_{CC} = 2.7 V	-	-	5.6	ns
		V_{CC} = 3.0 V to 3.6 V	2.2	3.7	5.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	see Fig. 5				
		V_{CC} = 2.7 V	-	-	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	3.6	5.0	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

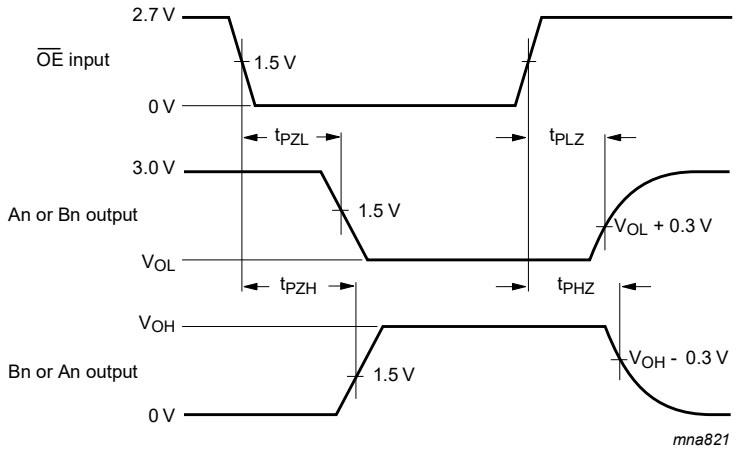
10.1. Waveforms and test circuit



V_M = 1.5 V

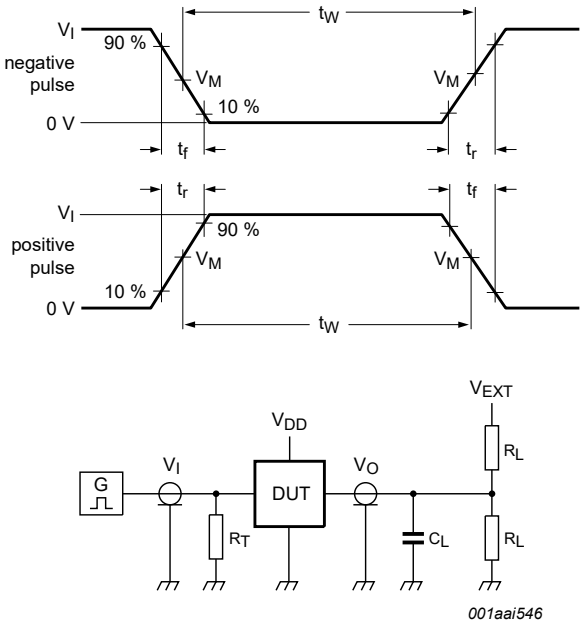
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Input (An or Bn) to output (Bn or An) propagation delays



V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. 3-state output enable and disable times



Test data is given in Table 8.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = Test voltage for switching times.

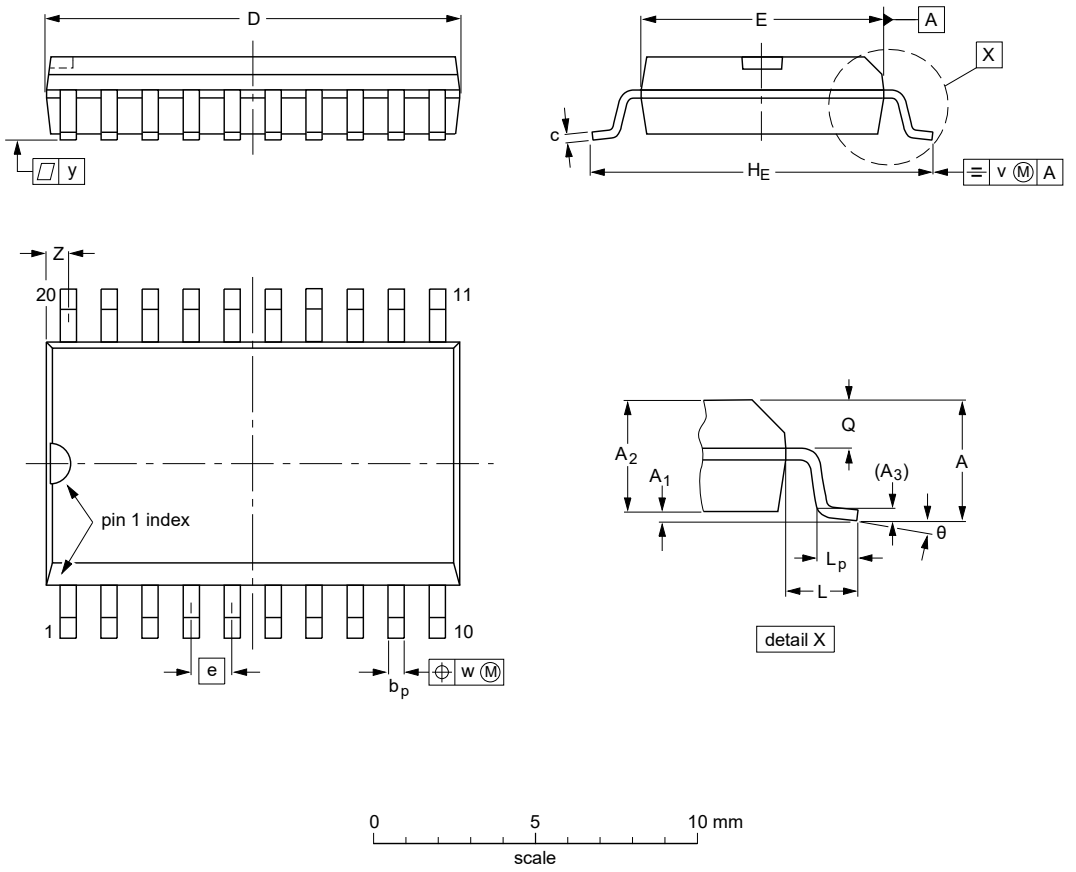
Fig. 6. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

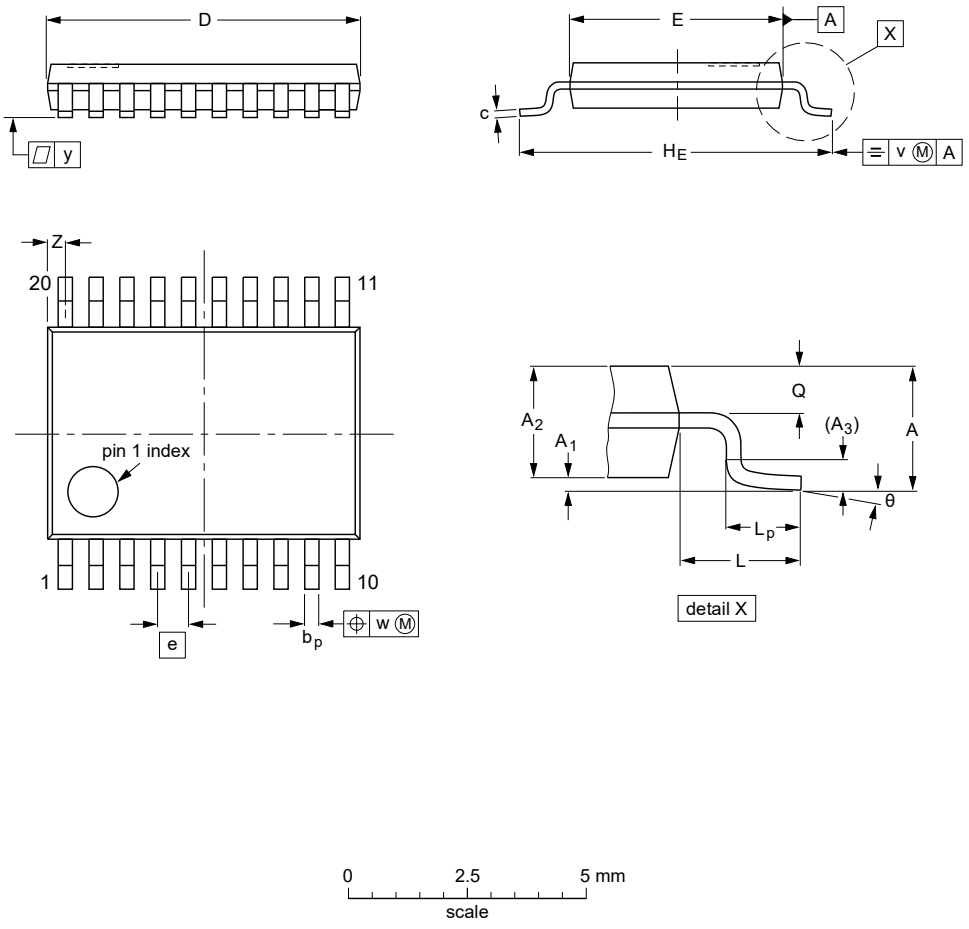
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH2245 v.8	20240708	Product data sheet	-	74LVT_LVTH2245 v.7
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVT_LVTH2245 v.7	20210817	Product data sheet	-	74LVT_LVTH2245 v.6
Modifications:	• Type number 74LVT2245DB (SOT339-1/SSOP20) removed.			
74LVT_LVTH2245 v.6	20210215	Product data sheet	-	74LVT_LVTH2245 v.5
Modifications:	• Type number 74LVTH2245DB (SOT339-1 / SSOP20) removed. • Section 1 and Section 2 updated. • Section 9: Conditions for I_{BHLO} and I_{BHHO} corrected. (errata)			
74LVT_LVTH2245 v.5	20170410	Product data sheet	-	74LVT_LVTH2245 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LVT_LVTH2245 v.4	20060424	Product data sheet	-	74LVT_LVTH2245 v.3
Modifications:	• Text changes have been made to the parameter descriptions of t_{PLH} and t_{PHL} in the Quick reference and Dynamic characteristics tables.			
74LVT_LVTH2245 v.3	20060323	Product data sheet	-	74LVT2245 v.2
74LVT2245 v.2	19980219	Product specification	-	74LVT2245 v.1
74LVT2245 v.1	19960311	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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