# 74VHC08; 74VHCT08

# **Quad 2-input AND gate**

Rev. 3 — 22 April 2024

**Product data sheet** 

### 1. General description

The 74VHC08; 74VHCT08 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard JESD7-A.

The 74VHC08; 74VHCT08 provide the quad 2-input AND function.

### 2. Features and benefits

- Balanced propagation delays
- All inputs have a Schmitt-trigger action
- Inputs accepts voltages higher than V<sub>CC</sub>
- Input levels:
  - The 74VHC08 operates with CMOS logic levels
  - The 74VHCT08 operates with TTL logic levels
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- · Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

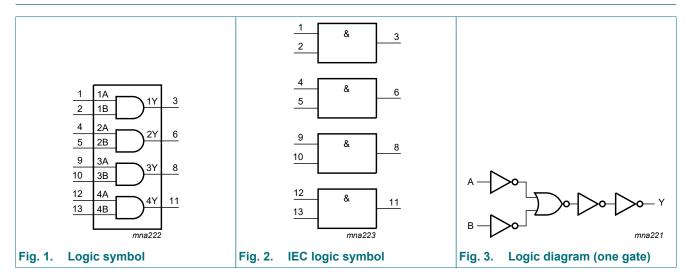
# 3. Ordering information

#### **Table 1. Ordering information**

Type number	Package			
	Temperature range	Description	Version	
74VHC08D 74VHCT08D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74VHC08PW 74VHCT08PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74VHC08BQ 74VHCT08BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

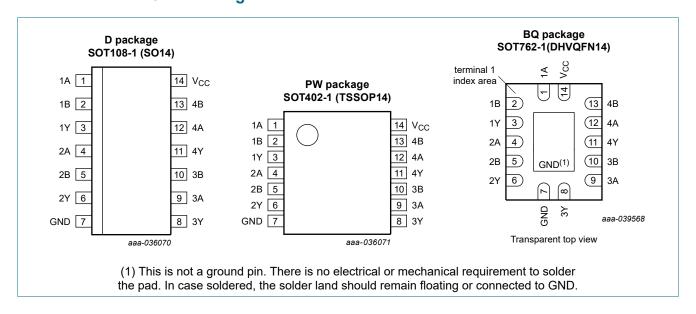


# 4. Functional diagram



# 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

# 6. Functional description

#### **Table 3. Function selection**

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care$ 

Input	Output	
nA	nB	nY
L	X	L
X	L	L
Н	Н	Н

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_1 < -0.5 \text{ V}$ [1]	-20	-	mA
I <sub>OK</sub>	output clamping current	$V_O < -0.5 \text{ V or } V_O > V_{CC} + 0.5 \text{ V}$ [1]	-	±20	mA
Io	output current	$V_O = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$	-	±25	mA
I <sub>CC</sub>	supply current		-	75	mA
I <sub>GND</sub>	ground current		-75	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C [2]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	1	74VHC08			74VHCT08		
			Min	Тур	Max	Min	Тур	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	0	-	5.5	V
$V_{O}$	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	-	-	20	-	-	20	ns/V

<sup>[2]</sup> For SOT108-1 (SO14) package: Ptot derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: Ptot derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: Ptot derates linearly with 9.6 mW/K above 98 °C.

# 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
For type	74VHC08		1				1			
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	$I_O = -50 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
	voltage	$I_O = -50 \mu A; V_{CC} = 3.0 V$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.58	-	-	2.48	-	2.4	-	V
		$I_O = -8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.94	-	-	3.8	-	3.7	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 50 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
	Voltage	$I_O = 50 \mu A; V_{CC} = 3.0 V$	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
		$I_O = 8.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.36	-	0.44	-	0.55	V
l <sub>l</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
For type	74VHCT08		'							'
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
	Voltage	I <sub>O</sub> = -8.0 mA	3.94	-	-	3.8	-	3.7	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	Ι <sub>Ο</sub> = 50 μΑ	-	0	0.1	-	0.1	-	0.1	V
	Voltage	I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μΑ
Icc	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μΑ
ΔI <sub>CC</sub>	additional supply current	per input pin; $V_1 = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other pins at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C <sub>I</sub>	input capacitance		-	3.0	10	-	10	-	10	pF

# 10. Dynamic characteristics

### **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see  $\underline{\text{Fig. 5}}$ .

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	Min	Max	
For type	74VHC08		•								
t <sub>pd</sub>	propagation	nA, nB to nY; see Fig. 4	[2]								
	delay	$V_{CC}$ = 3.0 V to 3.6 V; $C_L$ = 15 pF		-	4.0	8.8	1.0	10.5	1.0	11.0	ns
		$V_{CC}$ = 3.0 V to 3.6 V; $C_L$ = 50 pF		-	5.6	12.3	1.0	14	1.0	15.5	ns
		$V_{CC}$ = 4.5 V to 5.5 V; $C_L$ = 15 pF		-	3.0	5.9	1.0	7.0	1.0	7.5	ns
		$V_{CC}$ = 4.5 V to 5.5 V; $C_L$ = 50 pF			4.2	7.9	1.0	9.0	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$	[3]	-	10.0	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Min	Typ [1]	Max	Min	Max	Min	Max	
For type	74VHCT08										
t <sub>pd</sub> propagation	nA, nB to nY; see Fig. 4	2]									
	delay	$V_{CC}$ = 4.5 V to 5.5 V; $C_L$ = 15 pF		-	3.2	6.9	1.0	8.0	1.0	9.0	ns
		$V_{CC}$ = 4.5 V to 5.5 V; $C_L$ = 50 pF		-	4.2	7.9	1.0	9.0	1.0	10.0	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; $f_i$ = 1 MHz; [V <sub>I</sub> = GND to $V_{CC}$	3]	-	12.0	-	-	-	-	-	pF

- Typical values are measured at nominal supply voltage ( $V_{CC}$  = 3.3 V and  $V_{CC}$  = 5.0 V).
- $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).  $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

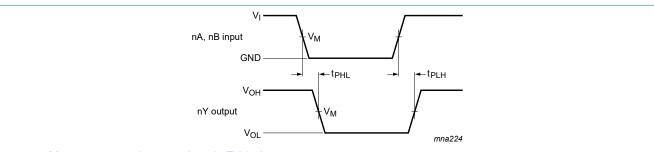
 $f_i$  = input frequency in MHz,  $f_o$  = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching  $\Sigma (C_L \times V_{CC}^{\ 2} \times f_o) = sum \ of \ the \ outputs.$ 

### 10.1. Waveforms and test circuit



Measurement points are given in Table 8.

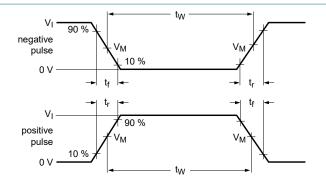
 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

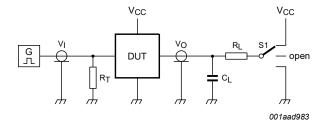
The input (nA, nB) to output (nY) propagation delays

**Table 8. Measurement points** 

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Туре	Input	Output		
	V <sub>M</sub>	V <sub>M</sub>		
74VHC08	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>		
74VHCT08	1.5 V	0.5V <sub>CC</sub>		

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Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>L</sub> = Load resistance.

S1 = Test selection switch.

### Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Туре	Input		Load		S1 position			
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>	
74VHC08	V <sub>CC</sub>	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	
74VHCT08	3.0 V	≤ 3.0 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	

# 11. Package outline

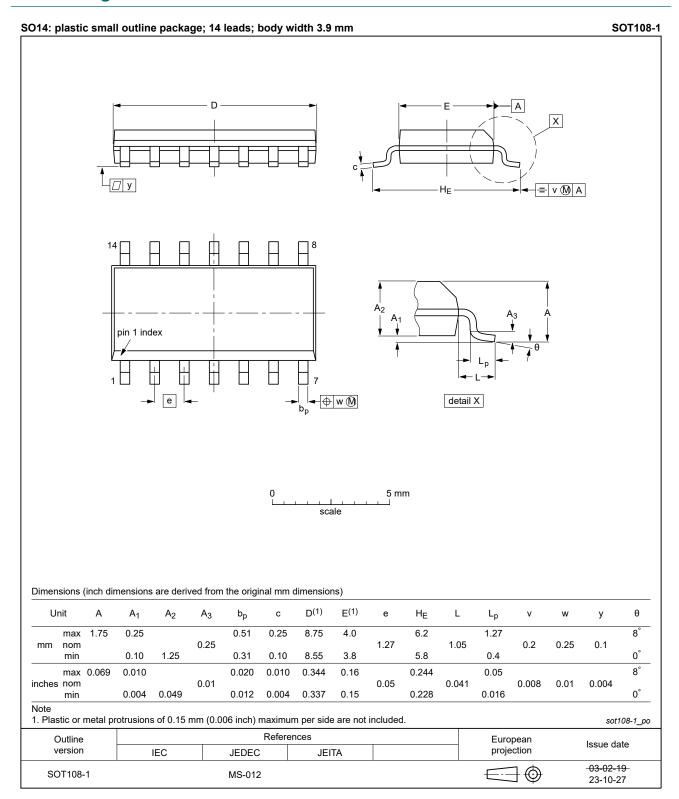


Fig. 6. Package outline SOT108-1 (SO14)

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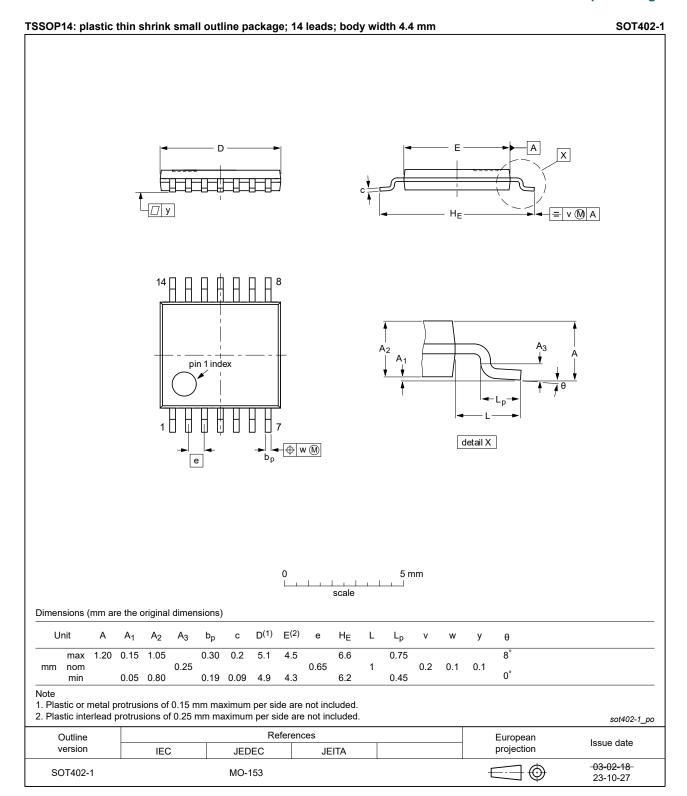


Fig. 7. Package outline SOT402-1 (TSSOP14)

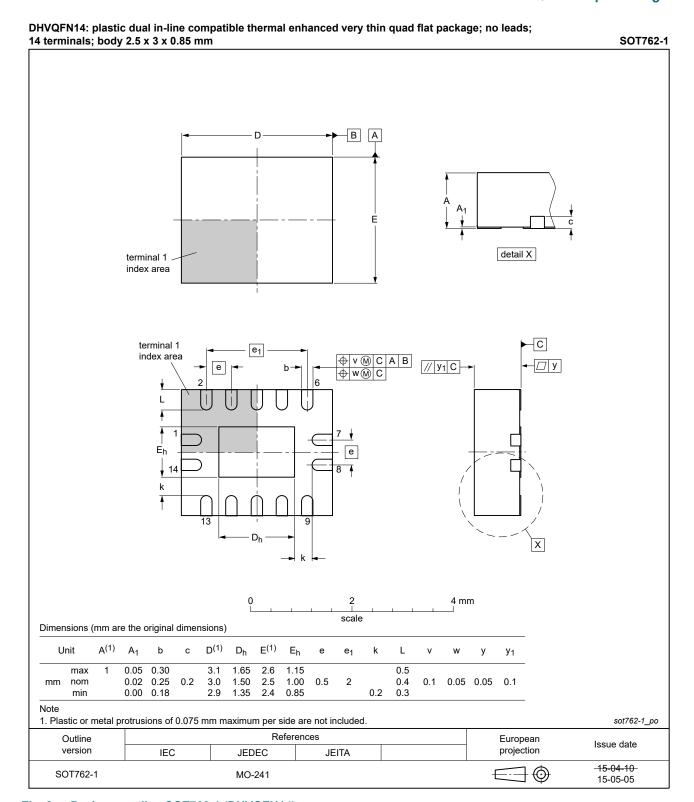


Fig. 8. Package outline SOT762-1 (DHVQFN14)

# 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
TTL	Transistor-Transistor Logic

# 13. Revision history

#### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74VHC_VHCT08 v.2	20240422	Product data sheet	-	74VHC_VHCT08_1	
Modifications:	<ul> <li>Section 2: ESD specification updated according to the latest JEDEC standard.</li> <li>Fig. 6 and Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> </ul>				
74VHC_VHCT08 v.2	20200408	Product data sheet	-	74VHC_VHCT08_1	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Table 4: Derating values for P<sub>tot</sub> total power dissipation updated.</li> <li>Package outline drawing SOT762-1 (DHVQFN14) updated.</li> </ul>				
74VHC_VHCT08_1	20090630	Product data sheet	-	-	

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#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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