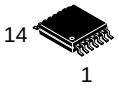
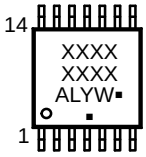
8-Bit Serial-In, Parallel-Out Shift Register

74VHC164



TSSOP−14
DT SUFFIX
CASE 948G

MARKING DIAGRAM



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

General Description

The VHC164 is an advanced high−speed CMOS device fabricated with silicon gate CMOS technology. It achieves the high−speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC164 is a high−speed 8−Bit Serial−In/Parallel−Out Shift Register. Serial data is entered through a 2−input AND gate synchronous with the LOW−to−HIGH transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs LOW independent of the clock. An input protection circuit insures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

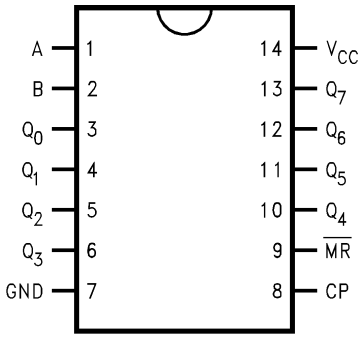
- High Speed: f_{MAX} = 175 MHz at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection Provided on All Inputs
- Low Noise: V_{OLP} = 0.8 V (Max.)
- Pin and Function Compatible with 74HC164
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Functional Description

The VHC164 is an edge−triggered 8−bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active High Enable for data entry through the other input. An unused input must be tied HIGH.

Each LOW−to−HIGH transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs (A · B) that existed before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs LOW.

CONNECTION DIAGRAM



PIN ASSIGNMENT

Pin Names	Description
A, B	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Master Reset Input (Active LOW)
Q_0–Q_7	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

Logic Symbol

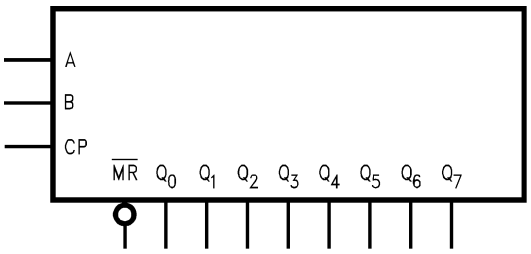


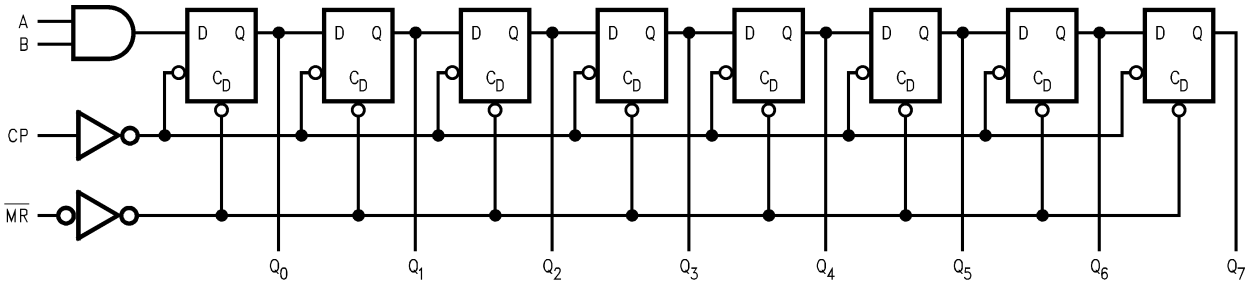
Figure 1. Logic Symbol

FUNCTIONAL TABLE

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	Q_1–Q_7
Reset (Clear)	L	X	X	L	L–L
Shift	H	L	L	L	Q_0–Q_6
	H	L	H	L	Q_0–Q_6
	H	H	L	L	Q_0–Q_6
	H	H	H	H	Q_0–Q_6

H = HIGH Voltage Levels
L = LOW Voltage Levels
X = Immaterial
Q = Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW−to−HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Diode Current, per Pin		±20	mA
I_{OUT}	DC Output Diode Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)		150	°C/W
P_D	Power Dissipation in Still Air at 25°C		833	mW
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 3)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	0	20	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			2.0	1.50	–	–	1.50	–	V
				3.0–5.5	0.7 x V_{CC}	–	–	0.7 x V_{CC}	–	
V_{IL}	LOW Level Input Voltage			2.0	–	–	0.50	–	0.50	V
				3.0–5.5	–	–	0.3 x V_{CC}	–	0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50 μA	2.0	1.9	2.0	–	1.9	–	V
				3.0	2.9	3.0	–	2.9	–	
				4.5	4.4	4.5	–	4.4	–	
			I_{OH} = –4 mA	3.0	2.58	–	–	2.48	–	
			I_{OH} = –8 mA	4.5	3.94	–	–	3.80	–	
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	–	0.0	0.1	–	0.1	V
				3.0	–	0.0	0.1	–	0.1	
				4.5	–	0.0	0.1	–	0.1	
			I_{OL} = 4 mA	3.0	–	–	0.36	–	0.44	
			I_{OL} = 8 mA	4.5	–	–	0.36	–	0.44	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		0–5.5	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		5.5	–	–	4.0	–	40.0	μA

NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C		Unit
				Typ	Limits	
V_{OLP} (Note 4)	Quiet Output Maximum Dynamic V_{OL}	C_L = 50 pF	5.0	0.5	0.8	V
V_{OLV} (Note 4)	Quiet Output Minimum Dynamic V_{OL}	C_L = 50 pF	5.0	–0.5	–0.8	V
V_{IHD} (Note 4)	Minimum HIGH Level Dynamic Input Voltage	C_L = 50 pF	5.0	–	3.5	V
V_{ILD} (Note 4)	Maximum LOW Level Dynamic Input Voltage	C_L = 50 pF	5.0	–	1.5	V

4. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 1 kΩ	3.3 ±0.3	80	125	−	65	−	MHz
		C_L = 50 pF, R_L = 1 kΩ		50	75	−	45	−	
		C_L = 15 pF, R_L = 1 kΩ	5.0 ±0.5	125	175	−	105	−	
		C_L = 50 pF, R_L = 1 kΩ		85	115	−	75	−	
t_{PLH}, t_{PHL}	Propagation Delay Time (CP–Q_n)	C_L = 15 pF, R_L = 1 kΩ	3.3 ±0.3	−	8.4	12.8	1.0	15.0	ns
		C_L = 50 pF, R_L = 1 kΩ		−	10.9	16.3	1.0	18.5	
		C_L = 15 pF, R_L = 1 kΩ	5.0 ±0.5	−	5.8	9.0	1.0	10.5	
		C_L = 50 pF, R_L = 1 kΩ		−	7.3	11.0	1.0	12.5	
t_{PHL}	Propagation Delay Time ($\overline{MR}$–Q_n)	C_L = 15 pF, R_L = 1 kΩ	3.3 ±0.3	−	8.3	12.8	1.0	15.0	ns
		C_L = 50 pF, R_L = 1 kΩ		−	10.8	16.3	1.0	18.5	
		C_L = 15 pF, R_L = 1 kΩ	5.0 ±0.5	−	5.2	8.6	1.0	10.0	
		C_L = 50 pF, R_L = 1 kΩ		−	6.7	10.6	1.0	12.0	
C_{IN}	Input Capacitance	V_{CC} = Open		−	4	10	−	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		−	76	−	−	−	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation:
I_{CC} (opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$.

AC OPERATING REQUIREMENTS

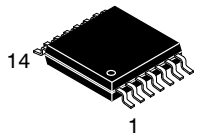
Symbol	Parameter	V_{CC} (V)	T_A = 25°C	T_A = −40°C to +85°C		Unit
			Typ	Guaranteed Minimum		
t_W(L), t_W(H)	Minimum Pulse Width (CP)	3.3	−	5.0	5.0	ns
		5.0	−	5.0	5.0	
t_W(L)	Minimum Pulse Width ($\overline{MR}$)	3.3	−	5.0	5.0	ns
		5.0	−	5.0	5.0	
t_S	Minimum Setup Time	3.3	−	5.0	6.0	ns
		5.0	−	4.5	4.5	
t_H	Minimum Hold Time	3.3	−	0.0	0.0	ns
		5.0	−	1.0	1.0	
t_{REC}	Minimum Removal Time ($\overline{MR}$)	3.3	−	2.5	2.5	ns
		5.0		2.5	2.5	

6. V_{CC} is 3.3 ±0.3 V or 5.0 ±0.5 V

ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC164MTCX	VHC 164	TSSOP−14 (Pb−Free, Halide Free)	2500 Units / Tape & Reel

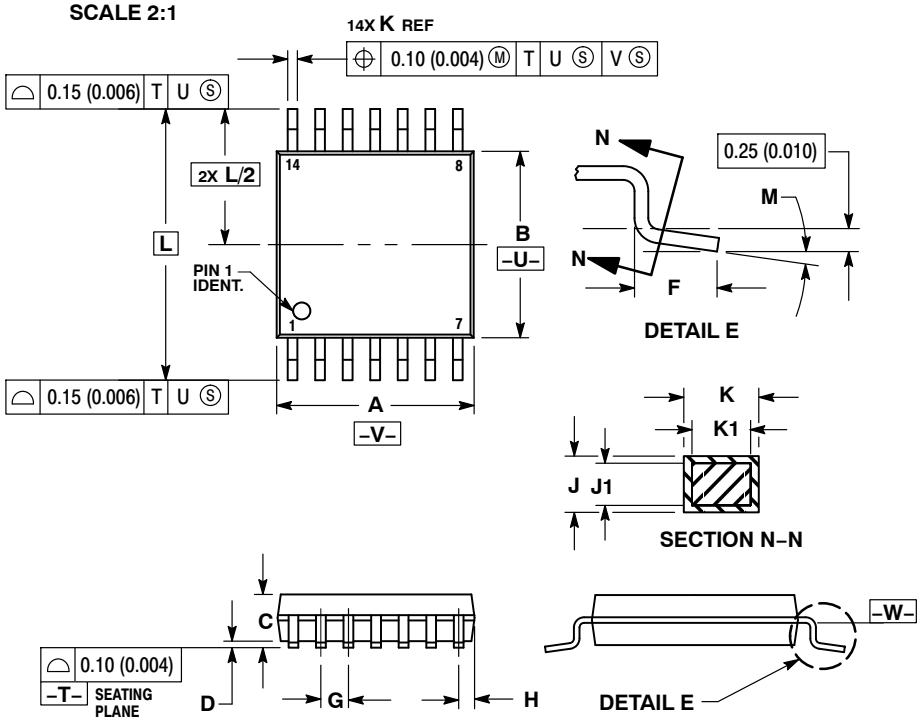
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

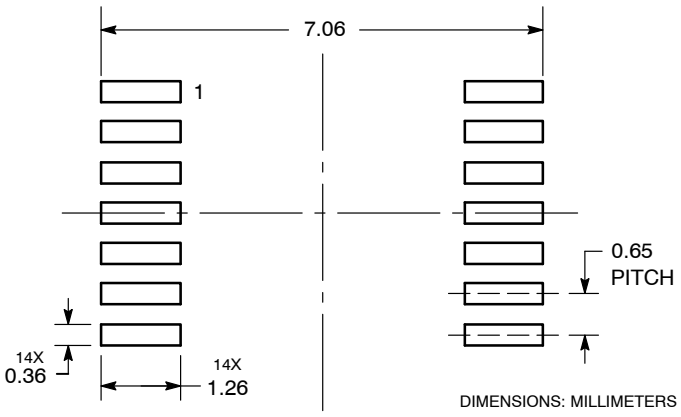
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

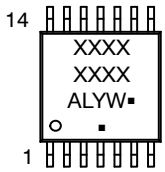
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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