BUCK-BOOST, BOOST, BUCK AND SEPIC LED CONTROLLER

Description

The AL8866Q is a Buck-Boost, Boost, Buck and SEPIC (single-ended primary-inductance converter) DC-Switching controller designed to drive an external MOSFET for high power automotive LED applications such as automotive front lighting. The AL8866Q operates within a wide input power supply range from 4.7V to 85V.

The AL8866Q bases on a fixed-frequency, peak current-mode control architecture to incorporate spread spectrum frequency modulation technique and achieve Low EMI performance.

The AL8866Q modulates LED current with analog or PWM dimming techniques. Analog dimming response with over 100:1 Linear range is obtained by varying the voltage at the DIM pin. PWM dimming is achieved by directly modulating the same DIM pin with the desired duty cycle.

The AL8866Q integrates soft-start function which limits the current through the inductor and external power switch during initialization start up. It gradually increases the inductor and switch current to minimize potential overvoltage and overcurrent at the output.

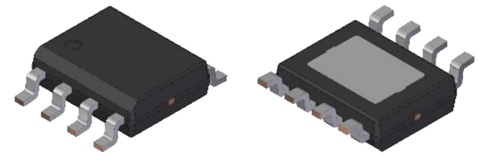
The AL8866Q with an open drain fault output indicates protection conditions triggered like LED output overvoltage, LED output open/short, cycle by cycle overcurrent protection, sense resistor and inductor/diode shorted, diode open and thermal shutdown.

The AL8866Q is available in the enhanced thermal SO-8EP and U-DFN3030-10 packages.

Features

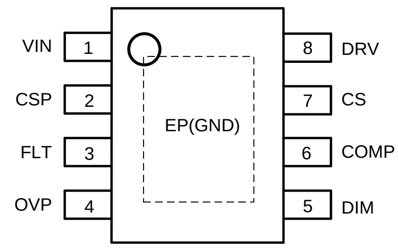
- AEC-Q100 (Grade 1)
- Wide Input Voltage Range from 4.7V to 85V
- Pre-Fixed 400kHz Switching Frequency (Factory Set)
- Spread Spectrum Frequency Modulation for Low EMI
- Analog Dimming Range: 1% to 100%
  - 100% Dimming Level ±3% Current Accuracy
  - 20% Dimming Level ±12% Current Accuracy
- PWM Dimming Ratio 100:1 at 200Hz PWM Frequency
- Programmable Soft Start
- Fault Status Indicator for Protections
- Output Overvoltage and LED Open Circuit Protection
- Output Undervoltage and LED Short Circuit Protection
- Cycle-by-Cycle Overcurrent Limitation Protection
- Sense Resistor Shorted Circuit Protection
- Diode/Inductor Shorted Circuit Protection
- Diode Open Circuit Protection
- Thermal Shutdown
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. “Green” Device (Note 3)**
- **The AL8866Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.** https://www.diodes.com/quality/product-definitions/

Pin Assignments



Top View Bottom View

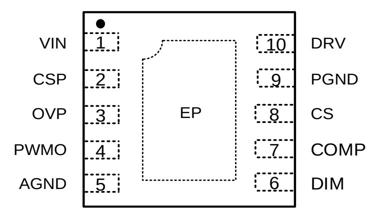
(Top View)



SO-8EP

Top View Bottom View

(Top View)



U-DFN3030-10

Applications

- Automotive front lightings
- Automotive high beams, low beams
- Automotive daytime running lights
- Automotive fog lights, turn lights and position lights
- Other automotive LED lightings

Notes: 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

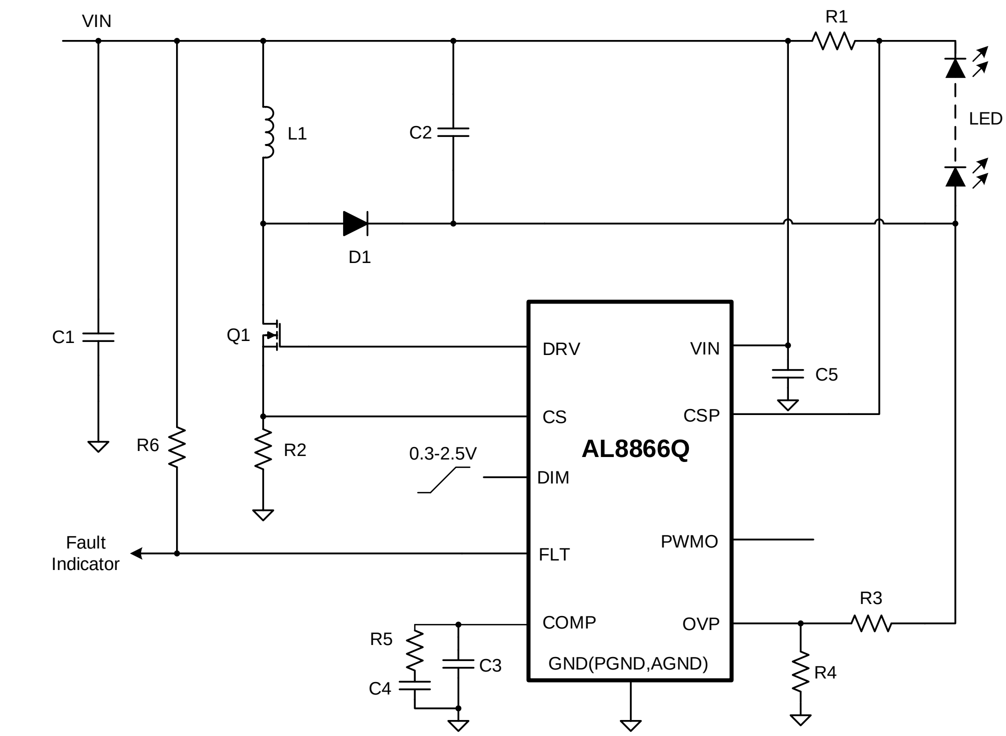


Figure 1 Typical Buck-Boost LED Driver Application

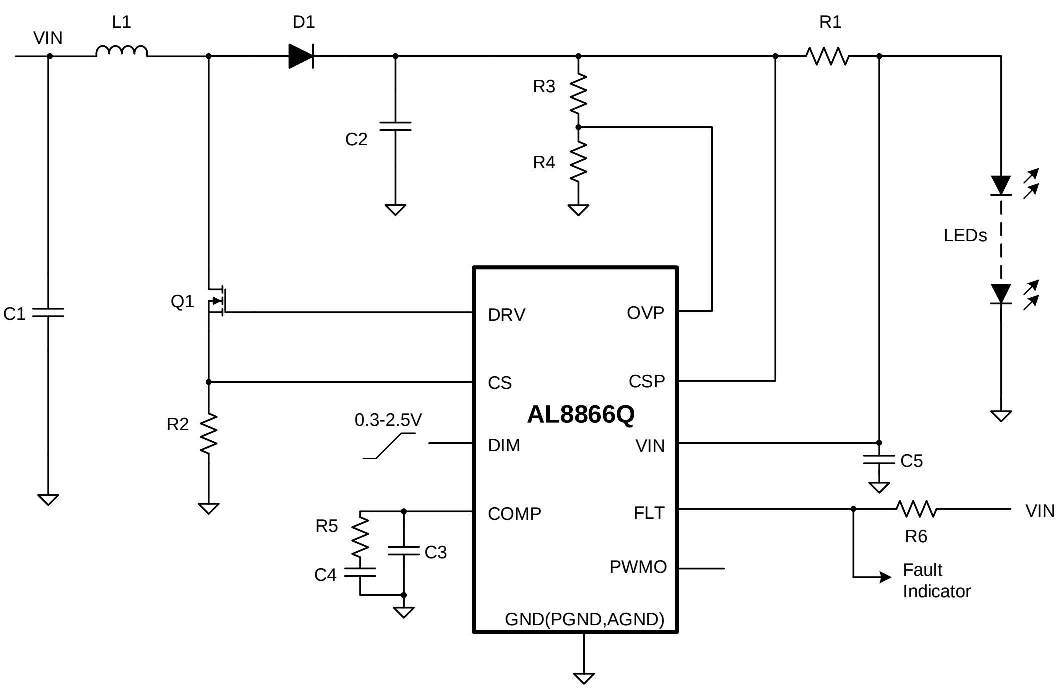


Figure 2 Typical Boost LED Driver Application

Typical Applications Circuit (continued)

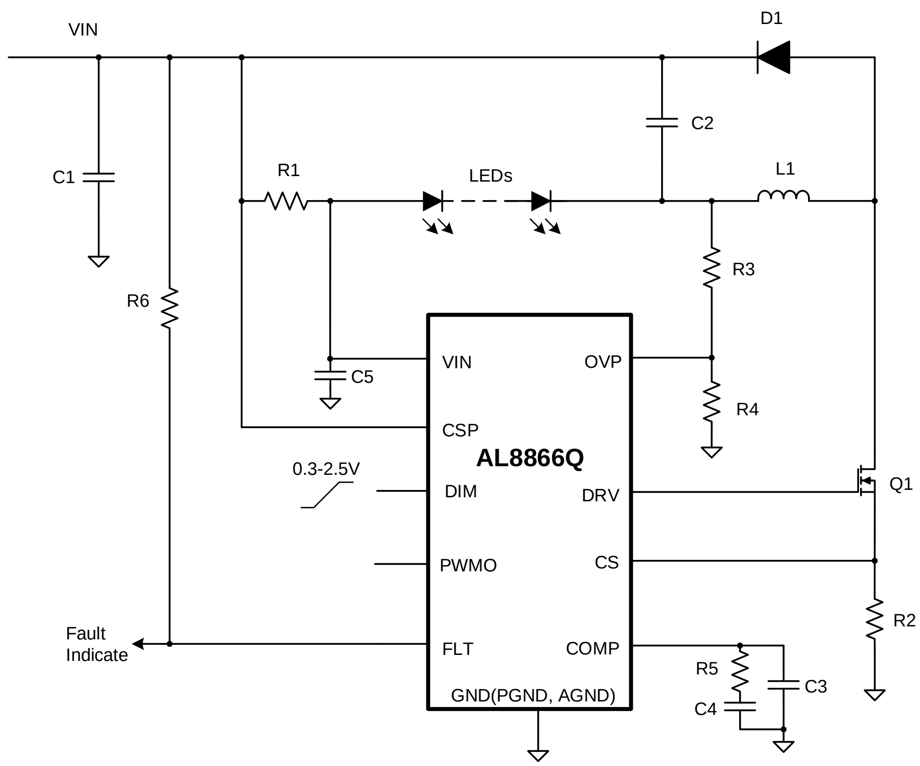


Figure 3 Typical Buck LED Driver Application

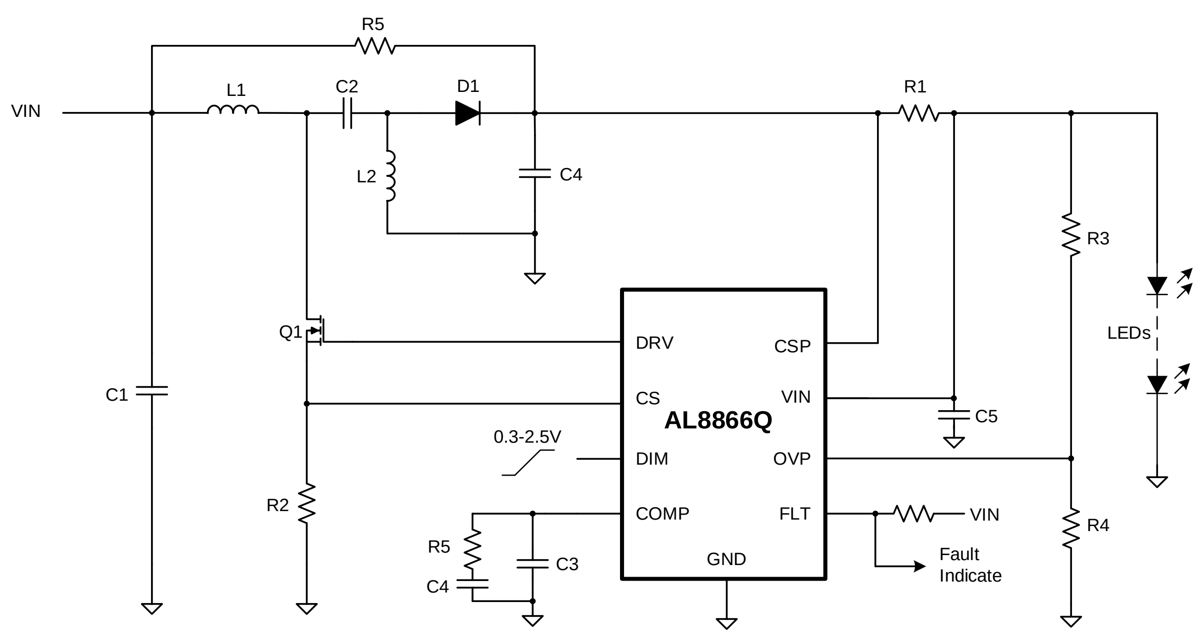


Figure 4 Typical SEPIC LED Driver Application

Pin Descriptions

Pin Number		Pin Name	Function
SO-8EP	U-DFN3030-10	—	
1	1	VIN	Input voltage. Decouple to ground with 1µF or higher X7R ceramic capacitor close to device.
2	2	CSP	Current sense amplifier positive input. Connect current sense resistor from CSP to VIN for current sense control.
3	—	FLT	Fault report pin. Asserted low to report faulty conditions. Needs an external pull-up resistor.
4	3	OVP	Input pin for Output Overvoltage and Output Under Voltage protection. Connected to resistive voltage divider or LED voltage sense circuits to set the over voltage threshold and output under voltage threshold.
5	6	DIM	Multi-function On/Off and brightness control pin: • Leave floating for normal operation. • Drive to voltage below 0.2V to stop the device switching. • Drive to voltage below 0.2V for longer than 30ms to shut down the device. • Drive with DC voltage (0.3V < VSET < 2.5V) to adjust output current from 0% to 100% of IOUT_NOM. • A PWM signal (low level < 0.2V, high level > 2.6V, transition times less than 1µs) allows the output current to be adjusted over a wide range up to 100%. • Connect a capacitor from this pin to ground to increase soft-start time.
6	7	COMP	Compensation output. Connect compensation network to achieve desired closed-loop response.
7	8	CS	Switch current sense input. Connect to the switch sense resistor to set the switch current limit threshold based on the internal reference voltage. Add a resistor from CS to the switching-MOSFET current-sense resistor terminal for programming the slope compensation.
8	10	DRV	N-channel MOSFET gate driver output. Connect to gate of external main switching N-channel MOSFET.
—	4	PWMO	The output pin for PMOS gate driving in PWM dimming operation.
NA	5	AGND	Analog ground.
NA	9	PGND	Power ground.
EP	EP	GND	Exposed pad must connect to GND for SO-8EP.

Functional Block Diagram

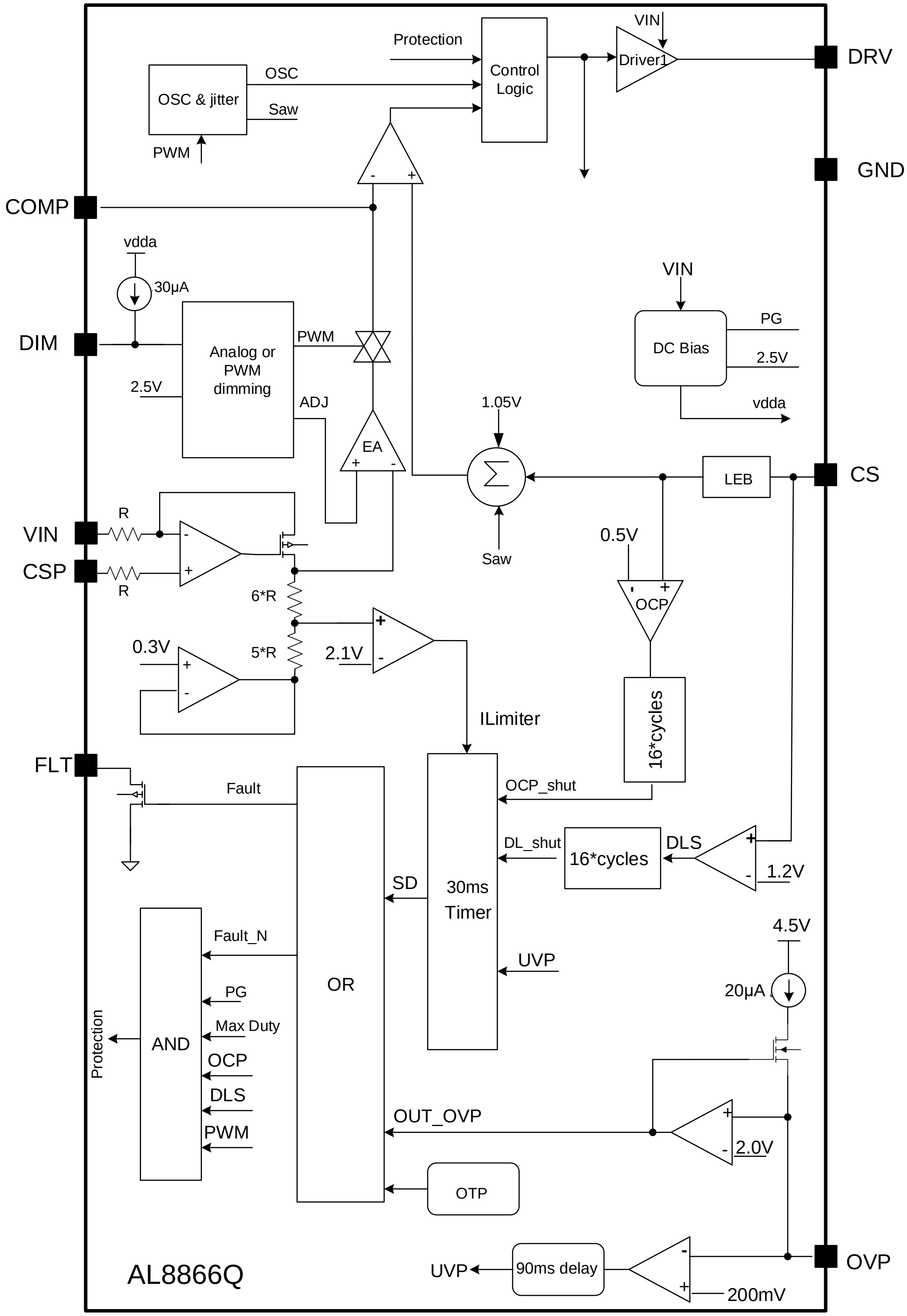


Figure 5 Block Diagram of AL8866QSP-13

Functional Block Diagram

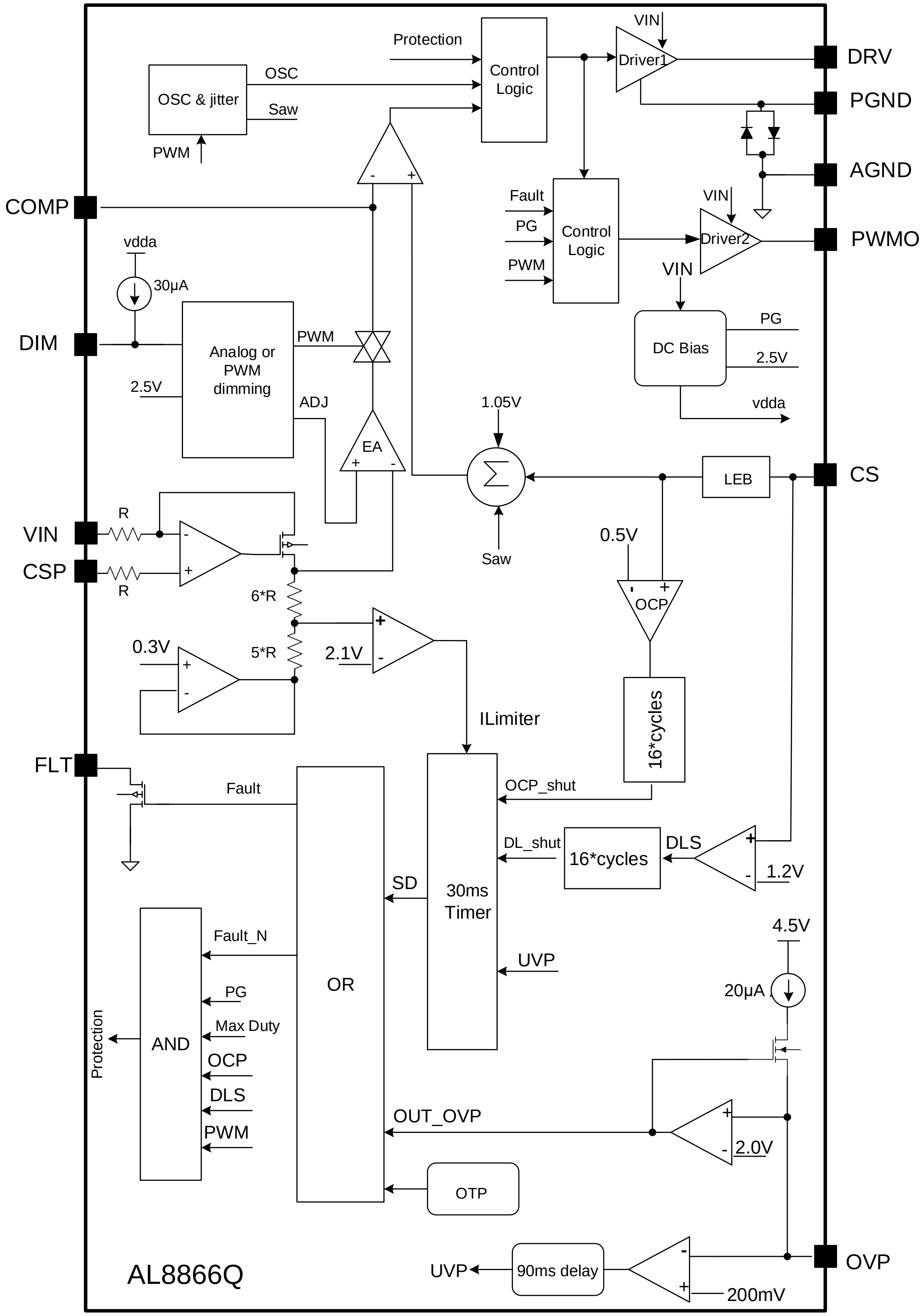


Figure 6 Block Diagram of AL8866QFN-7

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{VIN}, V_{CSP}, V_{FLT}, V_{OVP}, V_{DIM}	Voltage on VIN, CSP, FLT, OVP, DIM Pins	-0.3 to +86	V
V_{DRV}	Voltage on DRV Pin	-0.3 to +20	V
V_{CS}	Voltage on CS Pin	-0.3 to + 45	V
V_{COMP}, V_{PWMO}	Voltage on COMP, PWMO Pin	-0.3 to +6	V
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature Range	-65 to +165	°C

Note: 4. Stresses greater than those listed under *"Absolute Maximum Ratings"* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *"Recommended Operating Conditions"* is not implied. Exposure to *"Absolute Maximum Ratings"* for extended periods can affect device reliability.

ESD Ratings

Symbol	Parameter	Rating	Unit
V_{ESD}	Human-Body Model (HBM), per AEC-Q100-002 (Note 5)	±2000	V
	Charged-Device Model (CDM), per AEC-Q100-011	±1000	

Note: 5. AEC-Q100-002 indicates that HBM stressing shall be accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{IN}	Input Voltage	4.7	—	85	V
F_{PWM}	PWM Dimming Frequency	100	—	1000	Hz
f_{SW}	Operating Frequency	—	400	—	kHz
—	Analog Dimming Range	1	—	100	%
T_A	Operating Ambient Temperature	-40	—	+125	°C

Thermal Information (Note 6)

Package	Symbol	Parameter	Rating	Unit
SO-8EP	$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	63.6	°C/W
	$R_{\theta JC(TOP)}$	Junction-to-Case (Top) Thermal Resistance	75.5	°C/W
	$R_{\theta JC(BOTTOM)}$	Junction-to-Case (Bottom) Thermal Resistance	2.54	°C/W
	$R_{\theta JB}$	Junction-to-Board Thermal Resistance	21.8	°C/W
	Ψjt	Junction-to-Top Characterization Parameter	7.2	°C/W
	Ψjb	Junction-to-Board Characterization Parameter	22.4	°C/W
U-DFN3030-10	$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	51.8	°C/W
	$R_{\theta JC(TOP)}$	Junction-to-Case (Top) Thermal Resistance	49.7	°C/W
	$R_{\theta JC(BOTTOM)}$	Junction-to-Case (Bottom) Thermal Resistance	1.5	°C/W
	$R_{\theta JB}$	Junction-to-Board Thermal Resistance	16.6	°C/W
	Ψjt	Junction-to-Top Characterization Parameter	1.1	°C/W
	Ψjb	Junction-to-Board Characterization Parameter	16.9	°C/W

Note: 6. Device mounted on 2" × 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.

Electrical Characteristics (T_A = -40°C to +125°C, V_{IN} = 12V, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE (VIN)						
VIN_{UVLO}	Under-Voltage Lockout Voltage	VIN Rising Threshold	4.2	4.5	4.7	V
		VIN Falling Threshold	3.8	4.2	4.4	V
		UVLO Hysteresis	145	300	500	mV
I_Q	Quiescent Current	No Switching	0.9	1.8	2.5	mA
		Switching COMP = 3V, C_{DRV} = 1nF	—	6.5	—	mA
I_{SHDN}	Shutdown Supply Current	DIM < 0.2V, Disable Time ≥ 30ms	8	30	60	µA
OSCILLATOR						
f_{SW}	Switching Frequency Range	V_{DIM} = 2V	360	400	440	kHz
D_{MAX}	Maximum Duty Cycle	—	89	95	99	%
f_{DITH}	Frequency Dither	—	±6	±12	±16	%
f_M	Dither Modulation Frequency (Note 7)	—	—	400	—	Hz
LED CURRENT REGULATION (CSP, VIN)						
V_{SNS}	Current Sense Threshold, Voltage between CSP and VIN Pin	V_{DIM} = 2.5V	194	200	206	mV
		V_{DIM} = 0.74V	35	40	45	
I_{CSP}	CSP Pin Input Current	V_{IN} = V_{CSP}+ 0.1V	9	16	30	µA
GATE DRIVER (DRV)						
T_{RISE}	Gate Driver Rising Time	C_{DRV} = 1nF	18	40	70	ns
T_{FALL}	Gate Driver Falling Time	C_{DRV} = 1nF	18	35	70	ns
R_{GH}	Gate Driver High Side Resistance	I_{DRV} = -100mA	2	10	21	Ω
R_{GL}	Gate Driver Low Side Resistance	I_{DRV} = 100mA	0.9	4	10	Ω
V_{DRV_CLAMP}	Clamp Voltage On DRV Output	V_{IN} = 18V	10.0	11.0	12.2	V
INDUCTOR CURRENT SENSE (CS)						
V_{CS_LIMIT1}	Current Limit Threshold Voltage	—	450	500	550	mV
V_{CS_LIMIT2}	CS High Protection Threshold	Diode or Inductor Short	1.1	1.2	1.3	V
I_{SLOPE}	Slope-Compensation Current-Ramp Height	Peak Current Ramp Added to CS Input per Switching Cycle	40	52	80	µA
ANALOG DIMMING (DIM)						
V_{DIM}	Voltage Range On DIM Pin	For Analog Dimming	0.3	—	2.5	V
V_{DIM_CLAMP}	DIM Internal Clamp Voltage	—	3.4	4.0	4.5	V
V_{DIM_ON}	DC Voltage On DIM Pin for Analog Dimming On	V_{DIM} Rising	0.275	0.330	0.385	V
V_{DIM_OFF}	DC Voltage On DIM Pin for Analog Dimming Off	V_{DIM} Falling	0.28	0.30	0.32	V
t_{DIM_DIS}	Disable Time for Entering Standby Mode	DIM = Low	—	30	—	ms
I_{DIM}	DIM Sourcing Current	—	28.5	30	31.5	µA

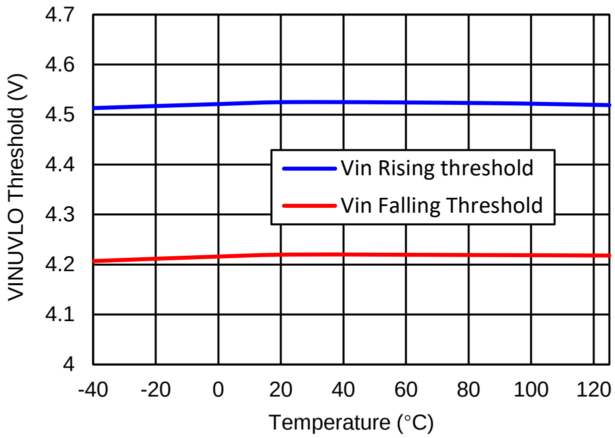
Note: 7. The parameter is guaranteed by design, not 100% tested in production.

Electrical Characteristics (T_A = -40°C to +125°C, V_{IN} = 12V, unless otherwise specified. continued)

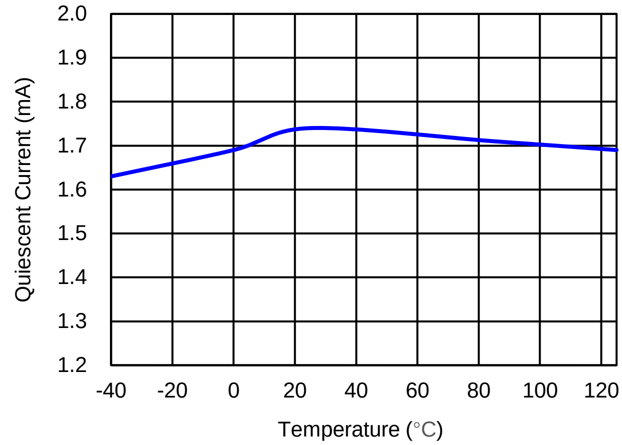
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ERROR AMPLIFIER (COMP)						
g_M	Transconductance of EA	—	80	105	130	µA/V
I_{SOURCE}	COMP Output Source Current	—	120	140	170	µA
I_{SINK}	COMP Output Sink Current	—	120	140	170	µA
OUPUT OVERVOLTAGE PROTECTION AND OUTPUT UNDERVOLTAGE PROTECTION (OVP)						
V_{OVP}	Overvoltage Protection Threshold	—	1.9	2.0	2.1	V
V_{UVP}	Undervoltage Protection Threshold	—	180	200	220	mV
I_{OVP_HYS}	OVP Hysteresis Current	—	12	20	27.5	µA
PWMO OUTPUT						
V_H	PWMO Internal Clamp Voltage	—	3.8	4.6	6	V
R_{PWMO_H}	PWMO Driver High Side Resistance	I_{DRV} = -10mA	—	100	—	Ω
R_{PWMO_L}	PWMO Driver Low Side Resistance	I_{DRV} = 10mA	—	5	—	Ω
FAULT FLAG (FLT)						
V_{FAULT_LOW}	FAULT Output Low Voltage	V_{IN} = 4.75V, V_{OVP} = 2V, I_{FAULT} = 5mA	—	—	200	mV
I_{FAULT_LEAK}	FAULT Leakage Current	V_{FAULT} = 85V	—	—	1	µA
THERMAL SHUTDOWN						
T_{TSD}	Thermal Shutdown Threshold	—	—	+170	—	°C
T_{TSD_HYS}	Thermal Shutdown Hysteresis	—	—	+25	—	°C

Typical Performance Characteristics (TA = -40°C to +125°C, VIN = 12V, unless otherwise specified.)

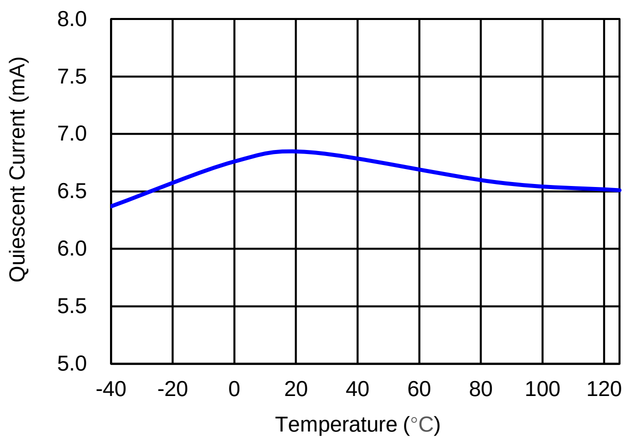
Under Voltage Lockout vs Temperature



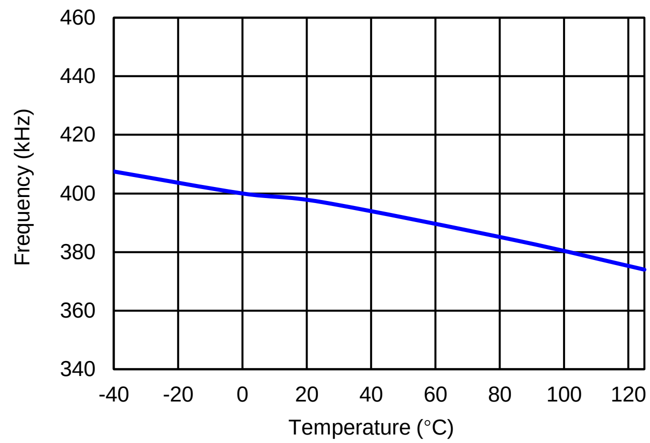
Quiescent Current (No Switching) vs Temperature



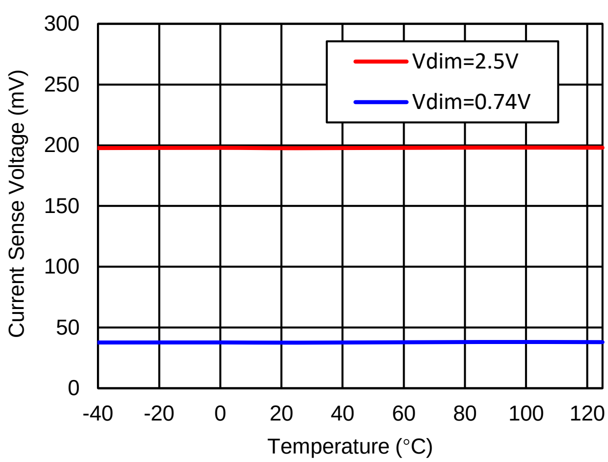
Quiescent Current (Switching) vs Temperature



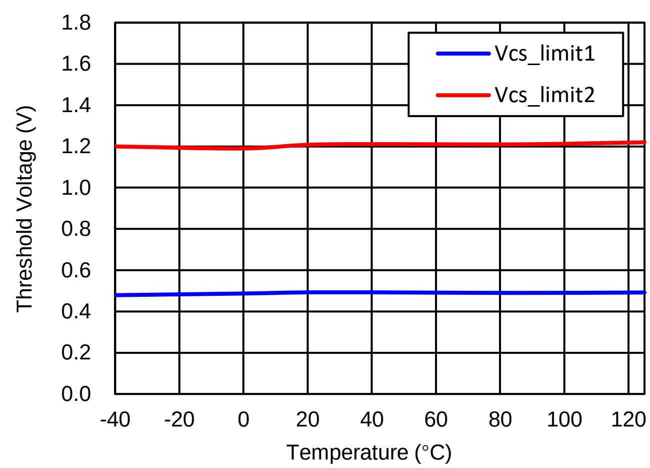
Switch Frequency vs Temperature



Current Sense VSNS vs Temperature

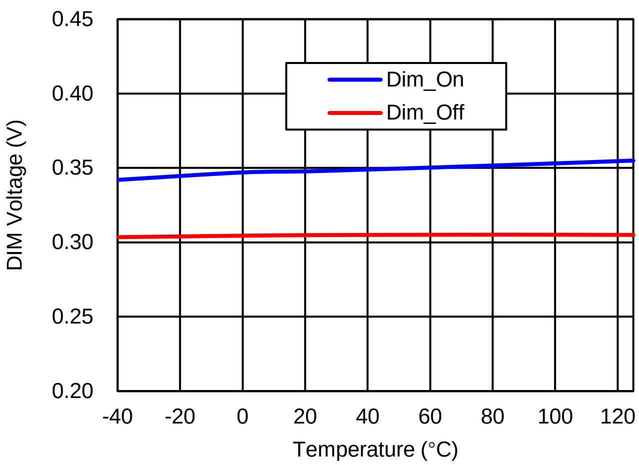


Inductor Currrent Limit Voltage vs Temperature

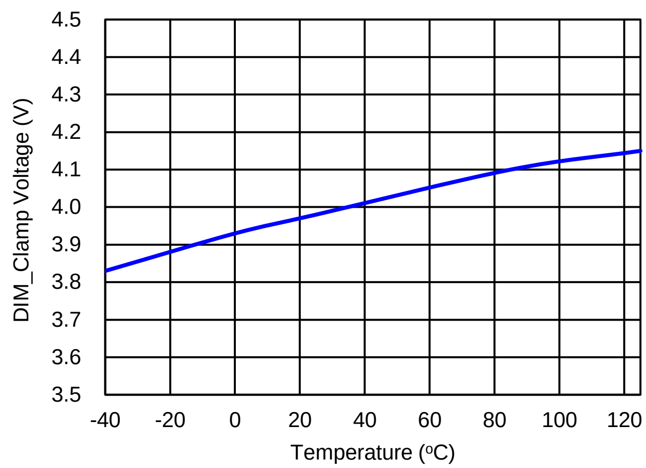


Typical Performance Characteristics (T_A = -40°C to +125°C, V_{IN} = 12V, unless otherwise specified.)

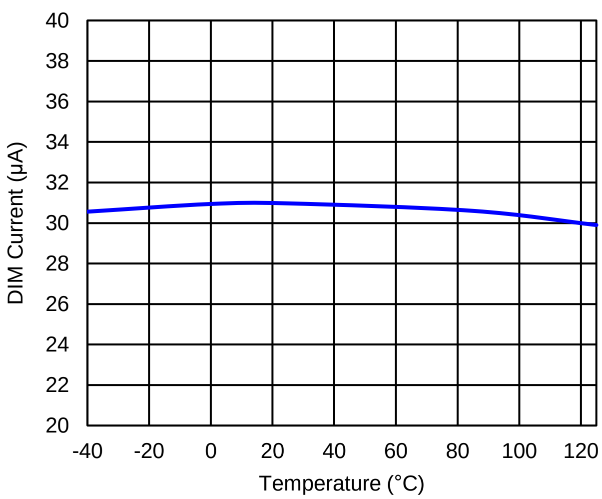
DIM ON/OFF Voltage vs Temperature



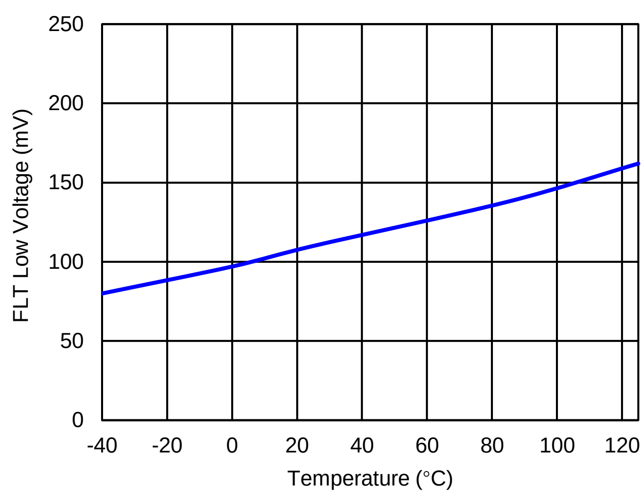
VDIM_Clamp vs Temperature



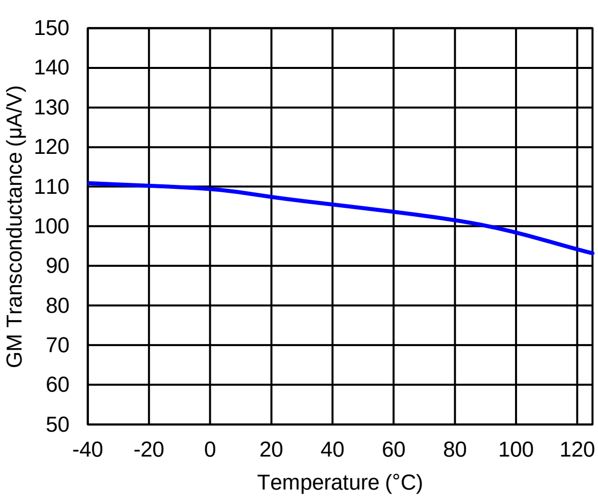
DIM Current vs Temperature



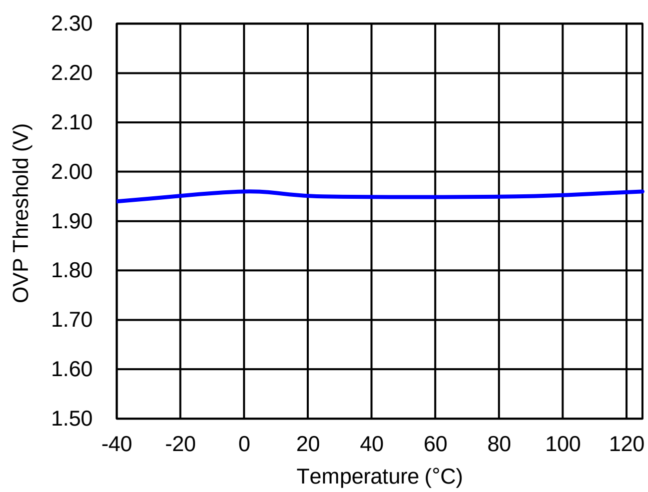
Fault Output Low Voltage vs Temperature



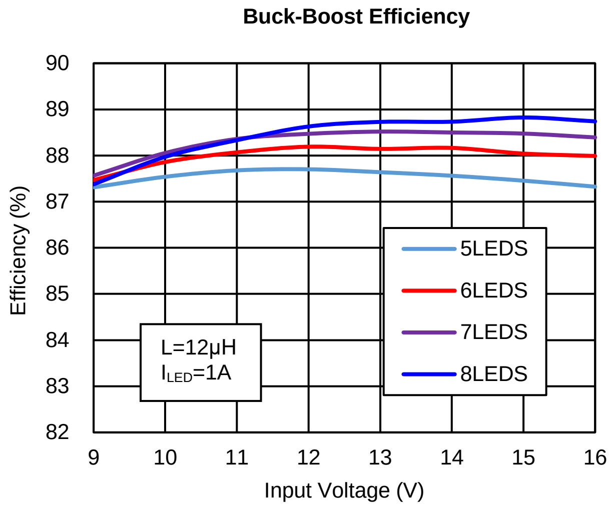
Error Amplifier GM vs Temperature

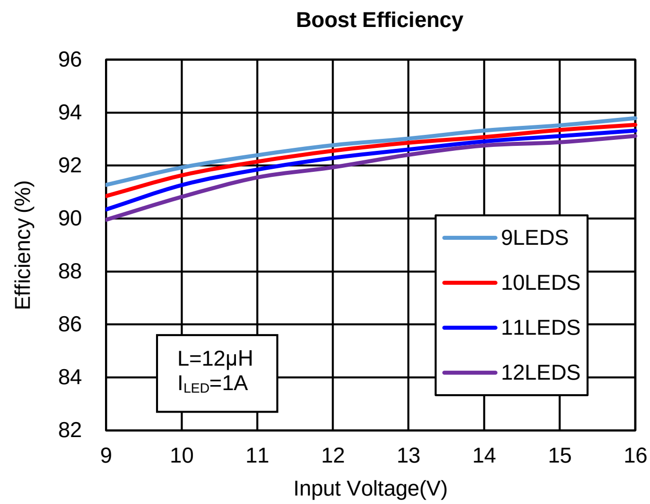


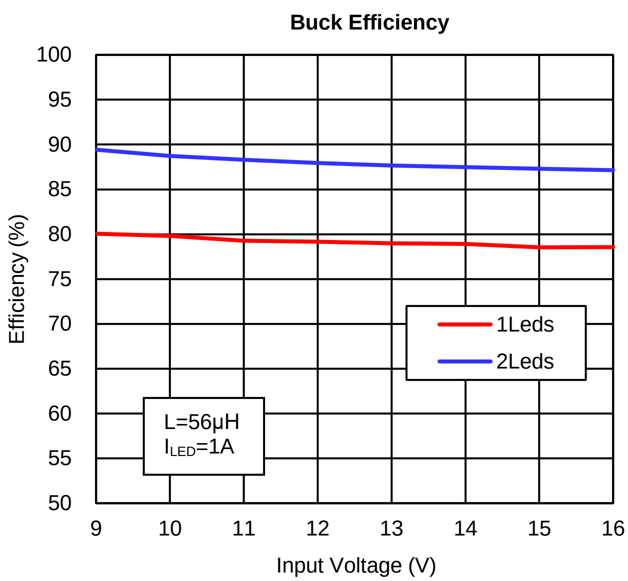
Overvoltage Protection Voltage vs Temperature

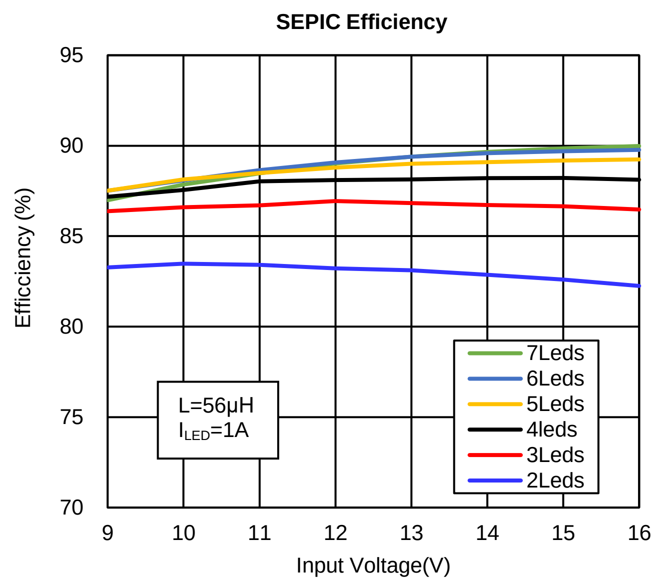


Typical Performance Characteristics (T_A = -40°C to +125°C, V_{IN} = 12V, unless otherwise specified.)









Application Information Overview

The AL8866Q implements a fixed-frequency, peak current-mode control technique to achieve constant output LED current and fast transient response. The integrated high accuracy current sense amplifier provides the flexibility required to power a single string consisting of 1 to 27 series connected LEDs while maintaining better than 3% current accuracy over the operation range. The AL8866Q can be designed to support multiple LED driver topology, such as Buck, Boost, Buck-Boost and SEPIC (single-ended primary-inductance converter).

LED Current Setting

The internal current sense amplifier measures the average LED current based on the differential voltage drop between the CSP and VIN inputs over a common mode range of 4.7V to 85V. The differential voltage, V_{SNS}, is amplified by a voltage-gain factor of 11 and is connected to the negative input of the transconductance error amplifier. The feedback loop will regulate the LED current to the target value set by internal voltage V_{ADJ} at the positive input of the error amplifier. The internal voltage V_{ADJ} is linear regulated by the DC voltage on the DIM pin. If the voltage is higher than 2.5V or PWM signal is applied to DIM pin, the LED current is programmed by the LED sense resistor, R_{SENSE}, between CSP pin and VIN pin, according to:

$$I_{LED} = \frac{V_{SNS}}{R_{SENSE}} = \frac{200\ mV}{R_{SENSE}}$$

Spread Spectrum

The AL8866Q incorporates spread spectrum frequency modulation technique for low EMI performance. The switching frequency is modulated by ±12% of nominal frequency at a rate of 400Hz via a triangular waveform. In one modulation cycle, the switching frequency varies linearly from a minimum to a maximum to a minimum again. The AL8866Q would disable spread spectrum function when the voltage on DIM pin lower than 1V and re-activates this function when the voltage on DIM pin exceeds 1.1V. The average switching frequency of the AL8866Q is 400kHz typically when spread spectrum is active, and 360kHz typically when spread spectrum is disabled.

Slope Compensation

Slope compensation can be added to the MOSFET current-sense signal on CS pin to prevent subharmonic oscillations at duty cycles greater than 50%. During switching, a current source of saw tooth from 0 to 50µA is sourced from the CS input. An external resistor, R_{SLOPE}, connected between the CS pin and the source connection of the MOSFET, is used to program the appropriate amount of slope compensation.

PWM Dimming

The AL8866Q supports directive PWM dimming operation. The LED current can be adjusted digitally by applying a low frequency Pulse-Width-Modulated (PWM) logic signal to the PWM pin to turn the device on and off. This will produce an average output current proportional to the duty cycle of the control signal. To achieve a high resolution, the PWM frequency is recommended to be lower than 1kHz, however high dimming frequencies can be used, at the expense of dimming dynamic range and accuracy. The LED string would flicker at low dimming level in PWM dimming operation, recommend 3% minimum dimming level for 200Hz and 10% minimum dimming level for 1kHz. The dimming curve below shows the typical dimming range for this kind of dimming operation.

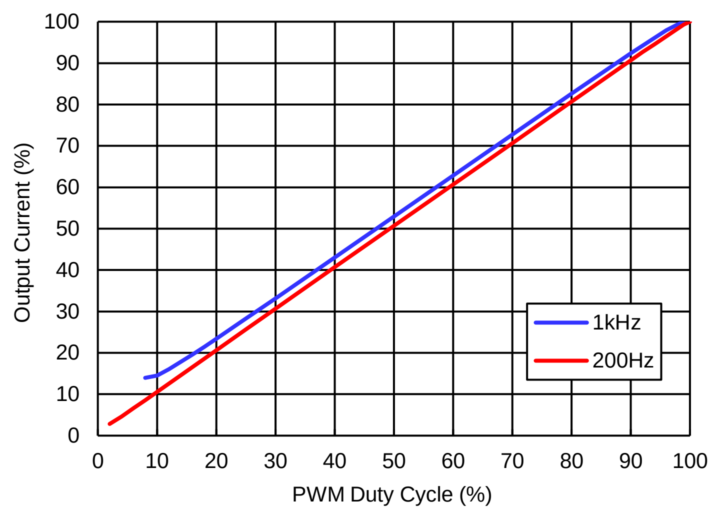


Figure 7 PWM Dimming Curve without PMOS Driving on Output on Buck-Boost

Application Information (continued)

To achieve better linearity of dimming curve in directive PWM dimming mode, the AL8866QFN-7 integrates PWMO output as dimming MOSFET driving. The driving signal is synchronizing with PWM dimming signal on PWM pin in normal status. Once a fault is triggered, the PWMO signal output low to turn off dimming MOSFET to protect LED load.

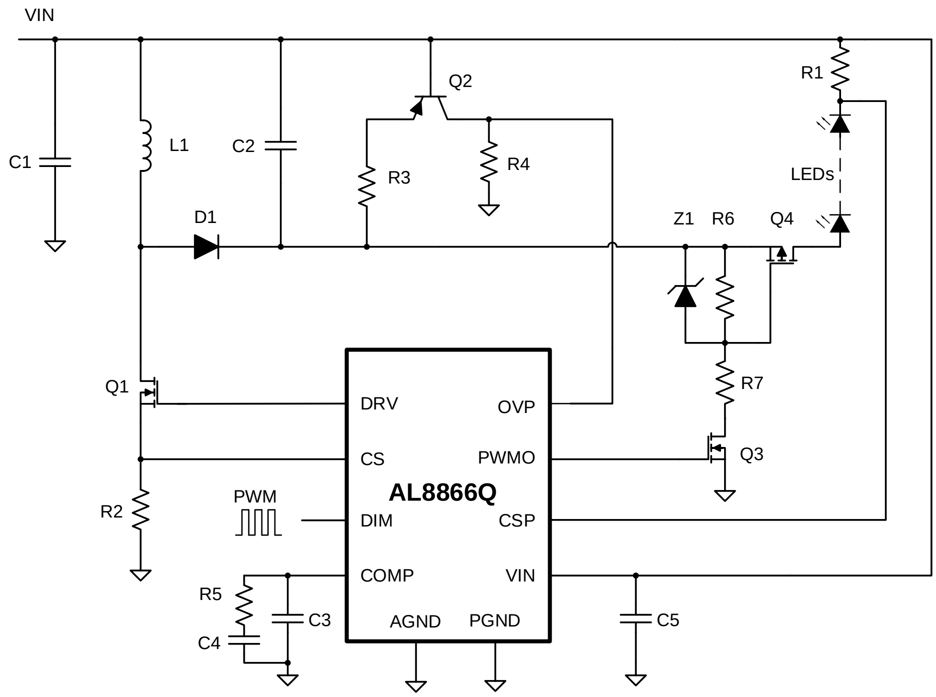


Figure 8 Buck-Boost LED Driver with PWM Dimming Operation

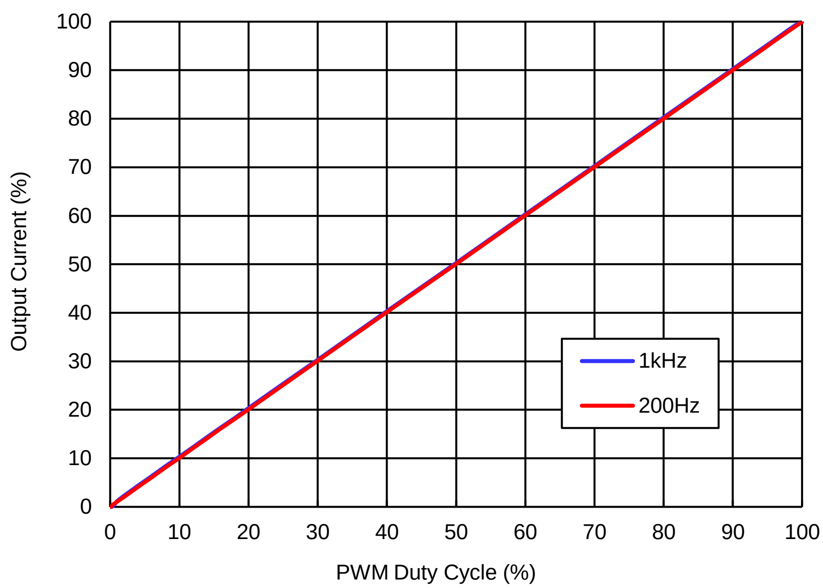


Figure 9 PWM Dimming Curve with PMOS Driving on Output on Buck-Boost

Application Information (continued)

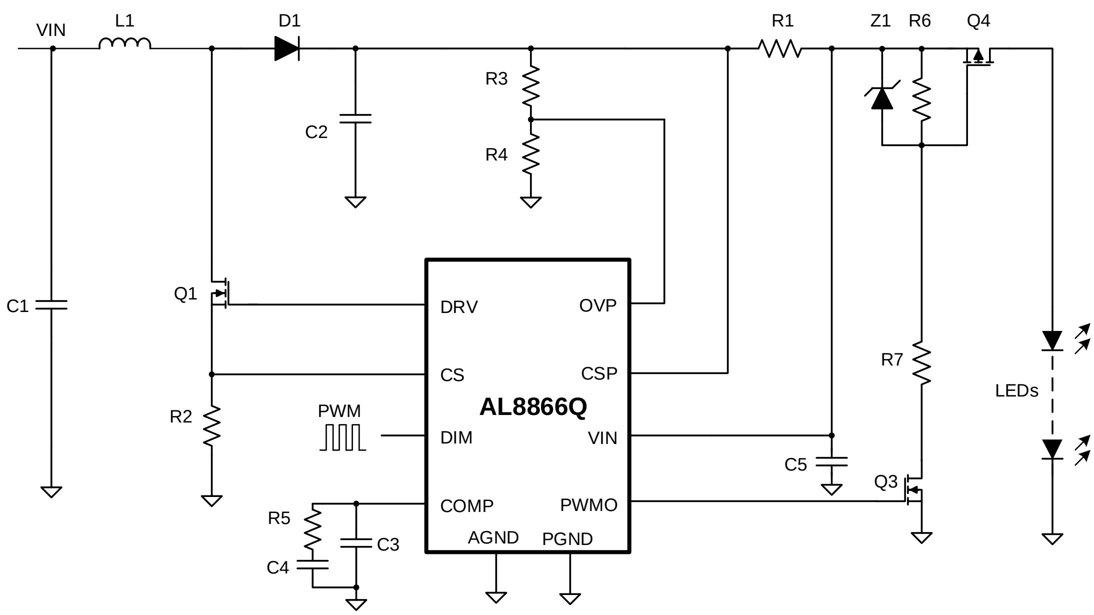


Figure 10 Boost LED Driver with PWM Dimming Operation

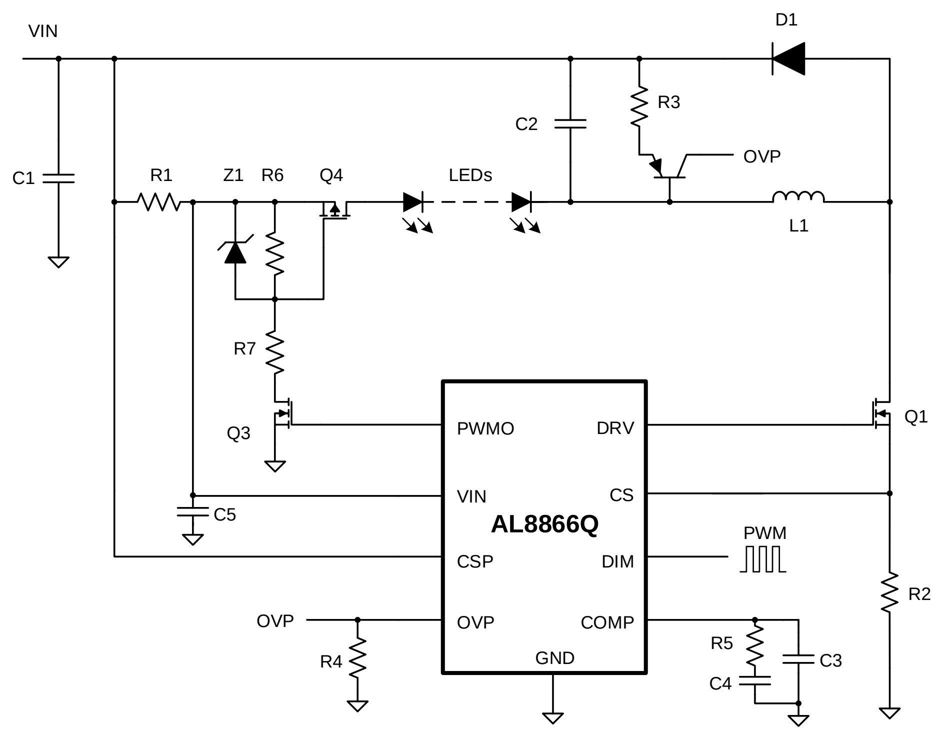


Figure 11 Buck LED Driver with PWM Dimming Operation

Application Information (continued)

Analog Dimming

The LED current can be linearly adjusted from 0 to 100% by varying the voltage at DIM pin from 0.3V to 2.5V.

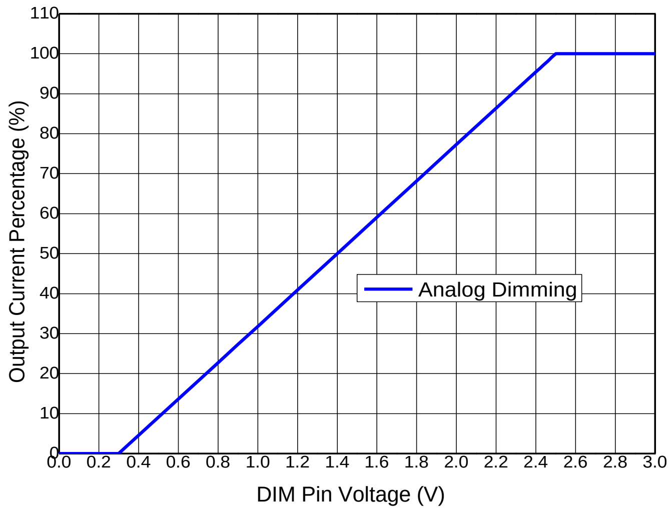


Figure 12 Analog Dimming Curve

Soft-Start

Soft-start can be provided via the analog dimming signal at DIM pin. The soft-start period can be programmed by the selection of appropriate capacitor between DIM pin and GND according to the following formula. The internal 30μA current source gradually increases the voltage on an external soft-start capacitor connected to the DIM pin. The default soft-start time is 11ms if no capacitor connected on DIM pin.

$$C_{soft} = \frac{t_{soft} \times 30 \times 10^{-6}}{2.5}$$

Protections

VIN Undervoltage Lockout (UVLO)

The AL8866Q monitors the voltage on VIN pin to implement UVLO protection. Operation is enabled when V_{VIN} exceeds 4.5V (typ) and is disabled when V_{VIN} drops below 4.2V (typ). The 300mV hysteresis is added on UVLO comparator to avoid chatter during transient. The UVLO threshold is fixed internal and cannot be adjusted. The VIN supply powers the internal circuitry. Place a bypass capacitor across the VIN and GND to ensure proper operation.

Output Overvoltage Protection (OVP) and LED Open-Circuit Protection

To prevent components damaged, the AL8866Q features output overvoltage protection. When LED string is open, the output voltage and V_{OVP} will increase immediately. The AL8866Q would enter hiccup mode once V_{OVP} exceed 2V. For different topology, customers need to select the suitable LED voltage sense circuitry. For Boost/SEPIC topologies, the output LED string cathode end is connected to ground, so designer could use simply resistor divider to sense the output LED voltage, as shown in Figure 2 & Figure 4.

$$V_{OVP} \approx \frac{R_4}{R_3 + R_4} \times (V_{LED} + V_{SNS})$$

For Buck-Boost and Buck application, the LED string cathode end is not connected to ground. Use an additional sensing circuit in Figure 8 and Figure 11 to sense LED string voltage accurately. The voltage on OVP pin in LED open status is calculated by following formula:

$$V_{OVP} \approx \frac{R_4}{R_3} \times (V_{LED} + V_{SNS} - V_{EB})$$

Where V_{EB} is the voltage between the emitter and base of bipolar.

To simplify circuit design, using a resistor divider to sense LED voltage roughly is acceptable if input voltage range is not too large on Buck-Boost topology shown in Figure 1.

$$V_{OVP} \approx \frac{R_4}{R_3 + R_4} \times (V_{IN} + V_{LED} + V_{SNS})$$

For Buck topology shown in Figure 3, use the following formula below to calculate the voltage on OVP pin.

$$V_{OVP} \approx \frac{R_4}{R_3 + R_4} \times (V_{IN} - V_{LED} - V_{SNS})$$

Application Information (continued)

Output Overvoltage Protection (OVP) and LED Open-Circuit Protection (continued)

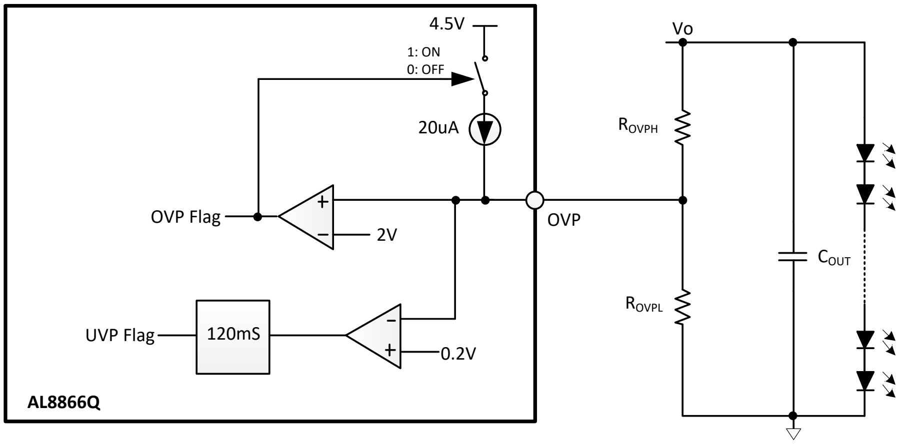


Figure 13 Output Overvoltage Detection Circuit

If V_{OVP} is higher than 2V, output overvoltage fault is detected and device enters Overvoltage Protection (OVP). The device is shutting down and the COMP capacitor is discharged, the FLT pin voltage is pulled to low level. When OVP is triggered, a 20µA current source goes through the resistor R_{OVPL} between OVP pin and GND, then V_{OVP} equals to 2V plus the hysteresis V_{HYS_OVP}.

$$V_{HYS\_OVP} = 20\mu A \times R_{OVPL}$$

If error is removed and V_{OVP} is lower than 2V, the internal comparator output turns to low, and the OVP flag is released, meanwhile a soft-start sequence is initiated to restart the device.

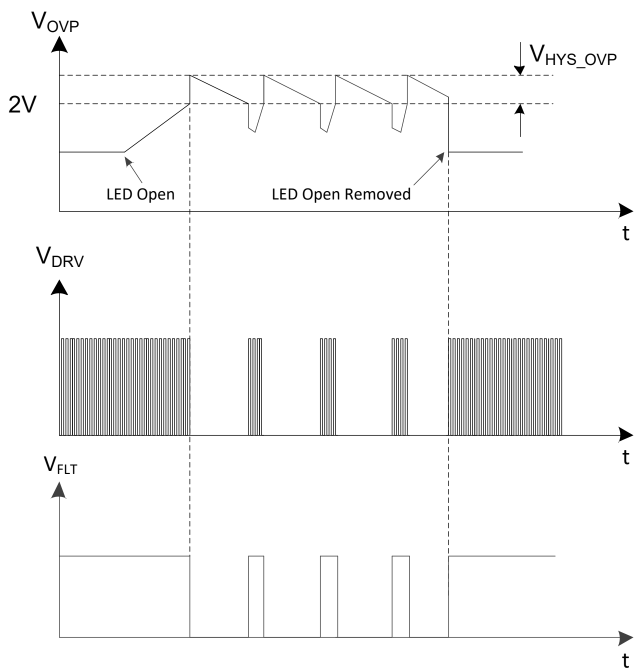


Figure 14 Output Overvoltage Protection

Application Information (continued)

Output Undervoltage Protection (UVP) and LED String Short-Circuit Protection

The AL8866Q features output LED short-circuit protection. When LED string (LED+ to LED-) is shorted, the voltage on output capacitor decreases rapidly. Meanwhile V_{OVP} decreases correspondingly. The voltage drop on output current sense resistor R_{LED} exceeds 0.36V, the output short condition is detected.

Once output short-circuit is detected, switching driver is shut-down; the device enters in hiccup mode. After 30ms, the device restarts to check if the short condition is removed. If the short condition still exists, V_{LED} should be very low. If V_{OVP} is lower than 0.2V for 60ms, the output Undervoltage Protection (UVP) is detected, and the device stops switching.

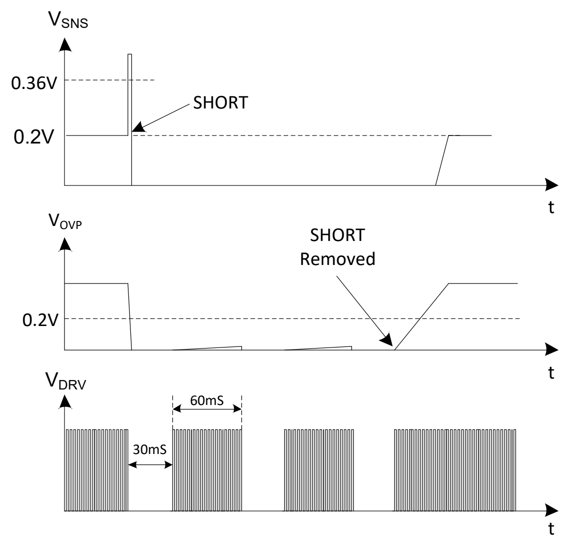


Figure 15 Output Short-Circuit Protection

Switching Current Limitation

The AL8866Q supports cycle-by-cycle current limit to prevent power switch from damage. The CS pin monitors the current going through power switch. Cycle-by-cycle current limit is accomplished by two internal comparators. After 100ns (typical) Leading Edge Blanking (LEB) time, if V_{CS} exceeds 0.5V in 16 switching cycles continuously, the switching overcurrent is detected. Another current limit comparator has 1.2V typical threshold. In any switching cycle, once V_{CS} exceeds 1.2V, the device terminates the switching to end this cycle immediately. If 1.2V-Current Limit is triggered for 16 switching cycle, the switching overcurrent is detected.

When a switching overcurrent fault is detected, the device turns off switching output, and the V_{FLT} is pulled down to low. System enters in hiccup mode. After 30ms turn off time, the system restarts to operate with soft-start sequence.

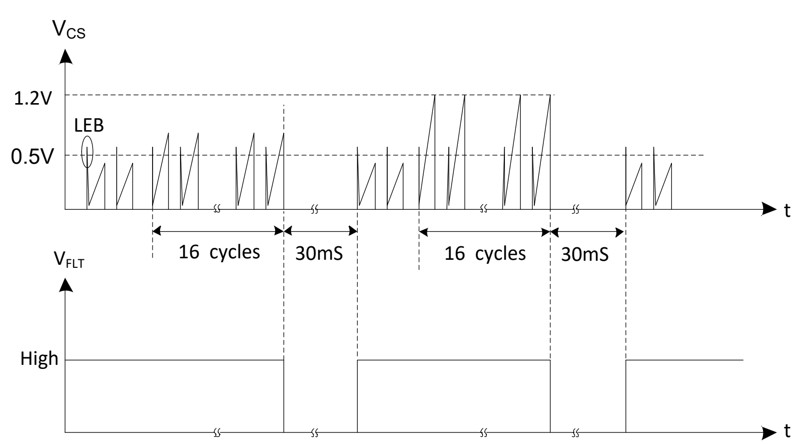


Figure 16 Switching Current Limit

Application Information (continued)

Sense Resistor Short-Circuit Protection

In single fault test, the sense resistor would be short. In this fault condition, the output current is set to a very large value. The current through inductor also increases significantly. When V_{CS} exceeds 0.5V for 16 cycles, the switching over current fault is detected, the device turns off switching to enter in hiccup mode.

Diode/Inductor Short-Circuit Protection

Once the main diode or inductor is short, the V_{CS} increases quickly to exceed 1.2V, and this situation V_{CS} pulse lasts for 16 switching cycle, the OCP protection is triggered. System enters hiccup mode to protect the device and power components.

Diode Open-Circuit Protection

The output capacitor discharges and the output voltage decreases while the diode is open. Once the V_{OVP} is lower than 0.2V, the output under voltage protection is triggered. System enters hiccup mode to protect the device and power components.

Thermal Shutdown Protection

Internal thermal shutdown circuitry is implemented to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at +170°C, the controller is forced into a shutdown mode, disabling the internal regulator. Once the device temperature is down to +145°C (typ +25°C hysteresis), the fault is cleared and restarts to switching. This feature is designed to prevent overheating and damage to the device.

Fault Indicator

The AL8866Q includes an open-drain output to indicate fault conditions. Designer could directly tie FLT to GPIO of micro controller or connects to input DC source via a resistor.

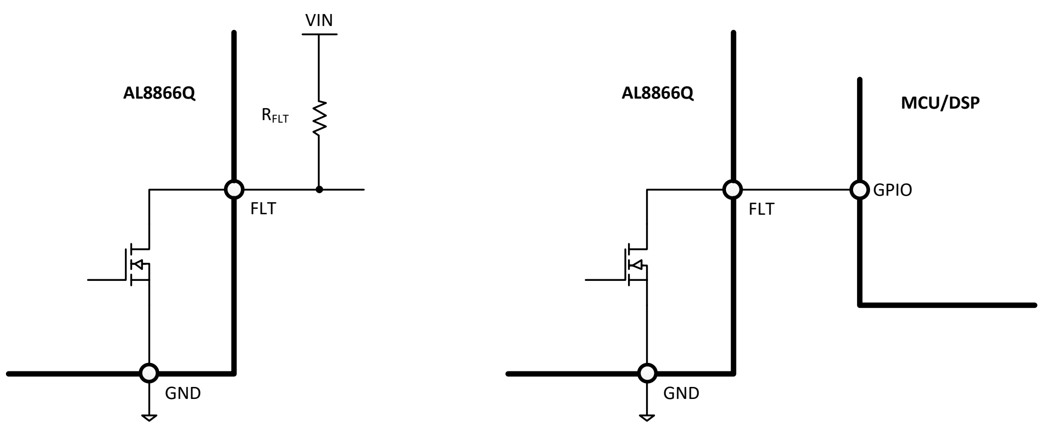


Figure 17 FLT Pin Interface Connection

Application Information (continued)

The FLT pin goes low under the following conditions:

- Output overvoltage protection / LED open-circuit protection
- Output undervoltage protection/ LED short-circuit protection
- Cycle-by-cycle current limitation
- Sense resistor short-circuit protection
- Diode/inductor short-circuit protection
- Diode open-circuit protection
- Thermal shutdown protection

Protection	Detection	FLT Status	Action
Input Undervoltage (UVLO)	V_{VIN} < 4V	High	VIN UVLO rising 4V with 0.4V hysteresis. FLT pin remains in high impedance state.
Cycle by Cycle Current Limit	V_{CS} > 500mV	Low	When fault occurs, cycle-by-cycle current limit operates. If fault > 16 switching cycles, the device is shutdown, the FLT pin is forced to low level, and enter hiccup period, then auto-restart.
Thermal Protection	T_J > +170°C	Low	The device is forced into a shutdown mode, and the FLT pin is forced to low level. A startup sequence is initiated when the junction temperature falls below +145°C.
Output Overvoltage Protection/ LED Open-Circuit Protection	V_{OVP} > 2V	Low	If the voltage at OVP pin is higher than 2V, the device is shut down and the COMP capacitor is discharged. The FLT pin is forced to low level. Meanwhile a 20µA current source on OVP pin is activated and go through external resistor on OVP pin. At this time the voltage on OVP pin equals to sum of 2V and voltage drop on external resistor on OVP pin. Soft-start sequence is initiated once the voltage on OVP pin drops below 2V.
Output Undervoltage Protection/ LED Short-Circuit Protection/ Diode Open-Circuit Protection	V_{CSP}- V_{VIN} > 360mV V_{OVP} < 200mV	Low	When the voltage gap between CSP and VIN pin exceeds 360mV, the output over current protection will be triggered. When OV pin voltage drops below 200mV, the device is shut down; the FLT pin is forced to low level, and enter hiccup period, then auto-restart.
Sense Resistor Short-Circuit Protection	V_{CS} > 500mV after LEB accumulated 16 switching cycles	Low	When the chip gate drive signal changes from low to high level, an internal comparator starts detecting the CS signal after leading edge blanking (LEB) time. When CS voltage exceeds 0.5V, the chip will immediately end the current gate drive and increment a counter. When the accumulates time in the counter reaches 16, this protection is triggered. The FLT pin is forced to low level, and enter hiccup period, then auto-restart.
Diode/Inductor Short-Circuit Protection	V_{CS} > 1.2V accumulated 16 switching cycles	Low	When the chip gate drive signal changes from low to high level, an internal comparator starts detecting the CS signal. When CS voltage exceeds 1.2V, the chip will immediately end the current gate drive and increment a counter. When the accumulates time in the counter reaches 16, this protection is triggered. The FLT pin is forced to low level, and enter hiccup period, then auto-restart.

Application Information (continued)

Duty Cycle Considerations

The switch duty cycle, D, defines the converter operation and is a function of the input and output voltages. In steady state, the duty cycle is derived using expression:

- Boost:

$$D = \frac{V_O - V_{IN}}{V_O}$$

- Buck-Boost:

$$D = \frac{V_O}{V_O + V_{IN}}$$

- Buck:

$$D = \frac{V_O}{V_{IN}}$$

The minimum duty cycle, D_{MIN}, and maximum duty cycle, D_{MAX}, are calculated by substituting maximum input voltage, $VIN_{(MAX)}$, and the minimum input voltage, $VIN_{(MIN)}$, respectively in the previous expressions. The minimum duty cycle achievable by the device is determined by the leading edge blanking period and the switching frequency. The maximum duty cycle is limited by the internal oscillator to 95% (typ) to allow for minimum off-time. It is necessary for the operating duty cycle to be within the operating limits.

Inductor Selection

The choice of inductor sets the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) boundary condition. Therefore, one approach of selecting the inductor value is by deriving the relationship between the output power corresponding to CCM-DCM boundary condition, $P_{O(BDRY)}$ and inductance, L. This approach ensures CCM operation in battery-powered LED driver applications that are required to support different LED string configurations with a wide range of programmable LED current set points. The CCM-DCM boundary condition can be estimated either based on the lowest LED current and the lowest output voltage requirements for a given application or as a fraction of maximum output power, $P_{O(MAX)}$.

$$P_{O(BDRY)} < I_{LED(MIN)}\ x\ V_{O(MIN)}$$

$$\frac{P_{O(MAX)}}{4} \le P_{O(BDRY)} \le \frac{P_{O(MAX)}}{2}$$

- Boost:

$$L = \frac{V_{IN(MAX)}^2}{2 \times P_{O(BDRY)} \times f_{sw}} \times (1 - \frac{V_{IN(MAX)}}{V_{O(MAX)}})$$

- Buck-Boost:

$$L = \frac{1}{2 \times P_{O(BDRY)} \times f_{sw} \times (\frac{1}{V_{O(MAX)}} + \frac{1}{V_{IN(MAX)}})^2}$$

- Buck:

$$L = \frac{(V_{IN(MAX)} - V_{O(MAX)})^2}{2 \times P_{O(BDRY)} \times f_{sw}} \times (\frac{V_{O(MAX)}}{V_{IN(MAX)}})^2$$

Select inductor with saturation current rating greater than the peak inductor current, I_{PK}, at the maximum operating temperature.

- Boost:

$$I_{PK} = \frac{P_{O(MAX)}}{V_{IN(MIN)}} + \frac{V_{IN(MIN)}}{2 \times L \times f_{sw} \times V_{O(MAX)}} \times (1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}})$$

- Buck-Boost:

$$I_{PK} = P_{O(MAX)} \times \left(\frac{1}{V_{O(MIN)}} + \frac{1}{V_{IN(MIN)}}\right) + \frac{V_{O(MIN)} \times V_{IN(MIN)}}{2 \times L \times f_{sw} \times (V_{O(MIN)} + V_{IN(MIN)})}$$

Application Information (continued)

Inductor Selection (continued)

- Buck:

$$I_{PK} = I_{O(MAX)} \times \frac{V_{IN(MIN)}}{V_{IN(MIN)} - V_{O(MAX)}} + \frac{(V_{IN(MIN)} - V_{O(MAX)}) \times V_{O(MAX)}}{2 \times L \times f_{sw} \times V_{IN(MIN)}}$$

Output Capacitor Selection

The output capacitors are required to attenuate the discontinuous or large ripple current generated by switching and achieve the desired peak-to-peak LED current ripple, $\Delta i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, r_D and the switching frequency, f_{SW}. The capacitance required for the target LED ripple current can be calculated based on following equations.

- Boost and Buck:

$$C_{OUT} = \frac{P_{O(MAX)}}{\Delta i_{LED(PP)} \times r_{D(MIN)} \times f_{sw} \times V_{O(MAX)}} \times (1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}})$$

- Buck-Boost:

$$C_{OUT} = \frac{P_{O(MAX)}}{\Delta i_{LED(PP)} \times r_{D(MIN)} \times f_{sw} \times (V_{O(MIN)} + V_{IN(MIN)})}$$

When choosing the output capacitors, it is important to consider the ESR and the ESL characteristics as they directly impact the LED current ripple. Ceramic capacitors are the best choice due to their low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions. DIODES recommends an X7R dielectric with voltage rating greater than maximum LED stack voltage. An aluminum electrolytic capacitor can be used in parallel with ceramic capacitors to provide bulk energy storage. The aluminum capacitors must have necessary RMS current and temperature ratings to ensure prolonged operating lifetime. The minimum allowable RMS output capacitor current rating, $I_{COUT(RMS)}$, can be approximated:

- Boost and Buck-Boost:

$$I_{COUT(RMS)} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

- Buck:

$$I_{COUT(RMS)} = \frac{V_{IN(MIN)} - V_{O(MAX)}}{\sqrt{12} \times L \times f_{sw}} \times D_{MAX}$$

Input Capacitor Selection

The input capacitors, C_{IN}, smooth the input voltage ripple and store energy to supply input current during input voltage or PWM dimming transients. The series inductor in the Boost and SEPIC topologies provides continuous input current and requires a smaller input capacitor to achieve desired input ripple voltage, $\Delta V_{IN(PP)}$. The Buck- Boost topology has discontinuous input current and require a larger capacitor to achieve the same input voltage ripple. Based on the switching frequency, f_{SW}, and the maximum duty cycle, D_{MAX}, the input capacitor value can be calculated as follows:

- Boost:

$$C_{IN} = \frac{V_{IN(MIN)}}{8 \times L \times f_{sw}^2 \times \Delta V_{IN(PP)}} \times (1 - \frac{V_{IN(MIN)}}{V_{O(MAX)}})$$

- Buck-Boost:

$$C_{IN} = \frac{P_{O(MAX)}}{f_{sw} \times \Delta V_{IN(PP)} \times (V_{O(MAX)} + V_{IN(MIN)})}$$

- Buck:

$$C_{OUT} = \frac{P_{O(MAX)}}{f_{sw} \times \Delta V_{IN(PP)} \times (V_{O(MAX)} + V_{IN(MIN)})} \times (1 - \frac{V_{O(MAX)}}{V_{IN(MIN)}})$$

X7R dielectric-based ceramic capacitors are the best choice due to their low ESR, high ripple current rating, and good temperature performance. For applications using PWM dimming, recommends an aluminum electrolytic capacitor in addition to ceramic capacitors to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

Application Information (continued)

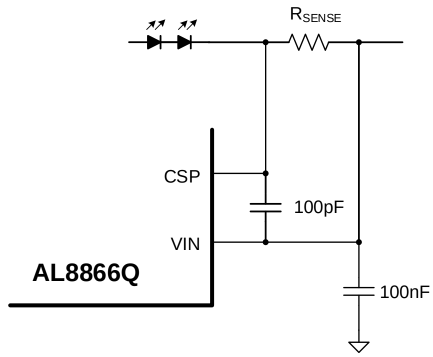


Figure 18 VIN and CSP Input Filter

Decouple VIN pin with a 0.1μF ceramic capacitor, placed as close as possible to the device and a series 10Ω resistor to create a 150kHz low-pass filter.

Main Power MOSFET Selection

The power MOSFET is required to sustain the maximum switch node voltage, V_{SW}, and switch RMS current derived based on the converter topology. TI recommends a drain voltage V_{DS} rating of at least 10% greater than the maximum switch node voltage to ensure safe operation. The MOSFET drain-to-source breakdown voltage, V_{DS}, is calculated using the following expressions.

- Boost:

$$V_{DS} = 1.1 \times V_{O(OV)}$$

- Buck-Boost:

$$V_{DS} = 1.1 \times (V_{O(OV)} + V_{IN(MAX)})$$

- Buck:

$$V_{DS} = 1.1 \times V_{IN(MAX)}$$

The voltage, $V_{O(OV)}$, is the overvoltage protection threshold and the worst-case output voltage under fault conditions. The worst case MOSFET RMS current for Boost and Buck-Boost topology is dependent on maximum output power, $P_{O(MAX)}$, and is calculated as follows:

- Boost & Buck-Boost:

$$I_{Q(RMS)} = \frac{P_{O(MAX)}}{V_{IN(MIN)})} \times \sqrt{1 + \frac{V_{IN(MIN)}}{V_{O(MIN)}}}$$

- Buck:

$$I_{Q(RMS)} = \frac{P_{O(MAX)}}{V_{IN(MIN)})} \times \sqrt{1 + \frac{V_{IN(MIN)}}{V_{O(MIN)}}} \times (1 - \frac{V_{O(MIN)}}{V_{IN(MIN)}})$$

Select a MOSFET with low total gate charge, Qg, to minimize gate drive and switching losses. The MOSFET $R_{DS(ON)}$ resistance is usually a less critical parameter because the switch conduction losses are not a significant part of the total converter losses at high operating frequencies. The switching and conduction losses are calculated as follows:

$$P_{Cond} = R_{DSON} \times I_{Q(RMS)}^2$$

$$P_{SW} = \frac{I_L \times V_{SW}^2 \times C_{rss} \times f_{sw}}{I_{GATE}}$$

$$P_{MOS\_TOTAL} = P_{Cond} + P_{SW}$$

C_{RSS} is the MOSFET reverse transfer capacitance. I_L is the average inductor current. I_{GATE} is gate drive output current, typically 500mA. The MOSFET power rating and package is selected based on the total calculated loss, the ambient operating temperature, and maximum allowable temperature rise.

Application Information (continued)

Switch Current Sense Resistor

The switch current sense resistor, R_{CS}, is used to implement peak current mode control and to set the peak switch current limit. The value of R_{CS} is selected to protect the main switching MOSFET under fault conditions. The R_{CS} can be calculated based on peak inductor current, $i_{L(PK)}$, and switch current limit threshold, V_{CS_LIMIT1} which is 0.5V typical.

$$R_{CS} = \frac{V_{CS\_LIMIT1}}{i_{L\_PK}}$$

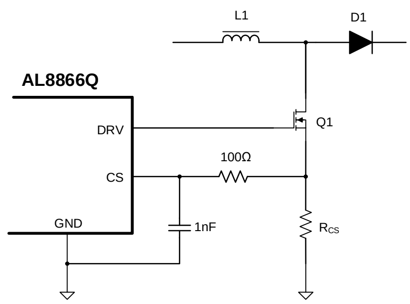


Figure 19 MOSFET Current Sense Input Filter

Feedback Compensation

The open-loop response is the product of the modulator transfer function and the feedback transfer function. Using a first-order approximation, the modulator transfer function can be modeled as a single pole created by the output capacitor, and in the boost and buck-boost topologies, a right half-plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance, r_D. The ESR of the output capacitor is neglected in the analysis. The small-signal modulator model also includes a DC gain factor that is dependent on the duty cycle, output voltage, and LED current.

- Boost & Buck-Boost:

$$\frac{\hat{\mathrm{i}}_{\mathrm{LED}}}{\hat{\mathrm{v}}_{\mathrm{COMP}}} = G_0 \times \frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{\omega_P}}$$

- Buck:

$$\frac{\hat{\mathrm{i}}_{\mathrm{LED}}}{\hat{\mathrm{v}}_{\mathrm{COMP}}} = G_0 \times \frac{1}{1 + \frac{s}{\omega_P}}$$

The Table listed below summarizes the expression for the small-signal model parameters.

Small-Signal Model Parameters

Topology	DC Gain (G_0)	Pole Frequency (ω_P)	Zero Frequency (ω_z)
Boost	$\frac{(1-D) \times V_O}{R_{CS} \times (V_O + r_D \times I_{LED})}$	$\frac{V_O + r_D \times I_{LED}}{V_O \times r_D \times C_{OUT}}$	$\frac{V_O \times (1-D)^2}{L \times I_{LED}}$
Buck-Boost	$\frac{(1-D) \times V_O}{R_{CS} \times (V_O + D \times r_D \times I_{LED})}$	$\frac{V_O + D \times r_D \times I_{LED}}{V_O \times r_D \times C_{OUT}}$	$\frac{V_O \times (1-D)^2}{D \times L \times I_{LED}}$
Buck	$\frac{V_O}{R_{CS} \times r_D \times I_{LED}}$	$\frac{1}{r_D \times C_{OUT}}$	—

The feedback transfer function includes the current sense resistor and the loop compensation of the transconductance amplifier. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. A simple capacitor, C_{COMP}, from COMP to GND (as shown in Figure 20) provides integral compensation and creates a pole at the origin. Alternatively, a network of R_{COMP}, C_{COMP}, and C_{HF}, shown in Figure 21, can be used to implement proportional and integral (PI) compensation to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

Application Information (continued)

The feedback transfer function is defined as follows.

Feedback transfer function with integral compensation:

$$-\frac{\hat{\mathrm{v}}_{\mathrm{COMP}}}{\hat{\mathrm{i}}_{\mathrm{LED}}}=\frac{11\times g_M\times R_{SENSE}}{\mathrm{s}\times C_{COMP}}$$

Feedback transfer function with proportional integral compensation:

$$-\frac{\hat{\mathrm{v}}_{\mathrm{COMP}}}{\hat{\mathrm{i}}_{\mathrm{LED}}}=\frac{11\times g_M\times R_{SENSE}}{\mathrm{s}\times(C_{COMP}+C_{HF})}\times\frac{1+\mathrm{s}\times R_{COMP}\times C_{COMP}}{1+\mathrm{s}\times R_{COMP}\times\frac{C_{COMP}\times C_{HF}}{C_{COMP}+C_{HF}}}$$

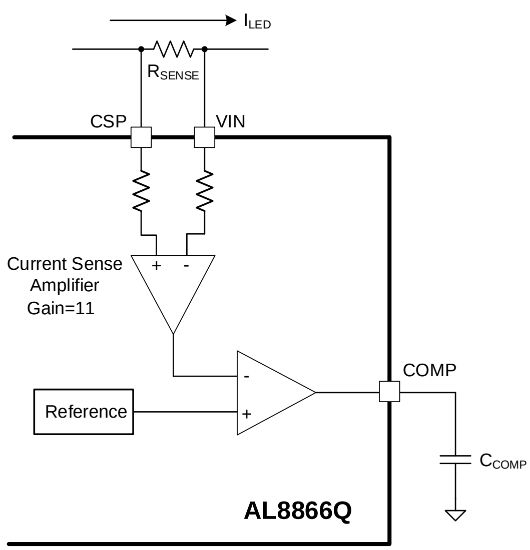


Figure 20 Integral Compensator

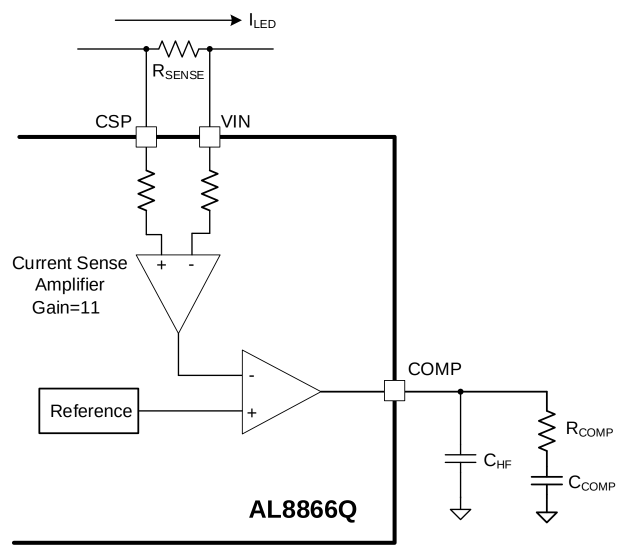


Figure 21 Proportional Integral Compensator

Boost and Buck-Boost with integral compensator:

$$C_{COMP}=\frac{8.75\times10^{-3}\times R_{SENSE}}{\omega_P}$$

Boost and Buck-Boost with proportional integral compensator:

$$C_{COMP}=8.75\times10^{-3}\times\frac{R_{SENSE}\times G_0}{\omega_Z}$$

$$C_{HF}=\frac{C_{COMP}}{100}$$

$$R_{COMP}=\frac{1}{\omega_P\times C_{COMP}}$$

The loop response is verified by applying step input voltage transients. The goal is to minimize LED current overshoot and undershoot with a damped response. Additional tuning of the compensation network may be necessary to optimize PWM dimming performance.

Layout

PCB Layout

1. The AL8866Q is a high switching frequency converter. Hence, attention must be paid to the switching currents interference in the layout. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. If the AL8866Q works at high power output condition, remarkable heat dissipation is a major concern in the layout of the PCB. 2oz copper for both the top and bottom layers is recommended. Four layers PCB is recommended to minimize ground noise.
2. Place the decoupling capacitor as closely across VIN and GND as possible.
3. Place the inductor as close to MOSFET drain node as possible.
4. Place the output capacitors as close to VIN/GND as possible for Buck-Boost/Boost.
5. The copper trace between the LED current sense resistor and the VIN & CSP pins should be kept parallel and the enclosed area should be minimized as much as possible.
6. Add as many vias as possible around both the GND pin and under the GND plane for heat dissipation to all the GND layers.
7. See Figure 22 for more details.

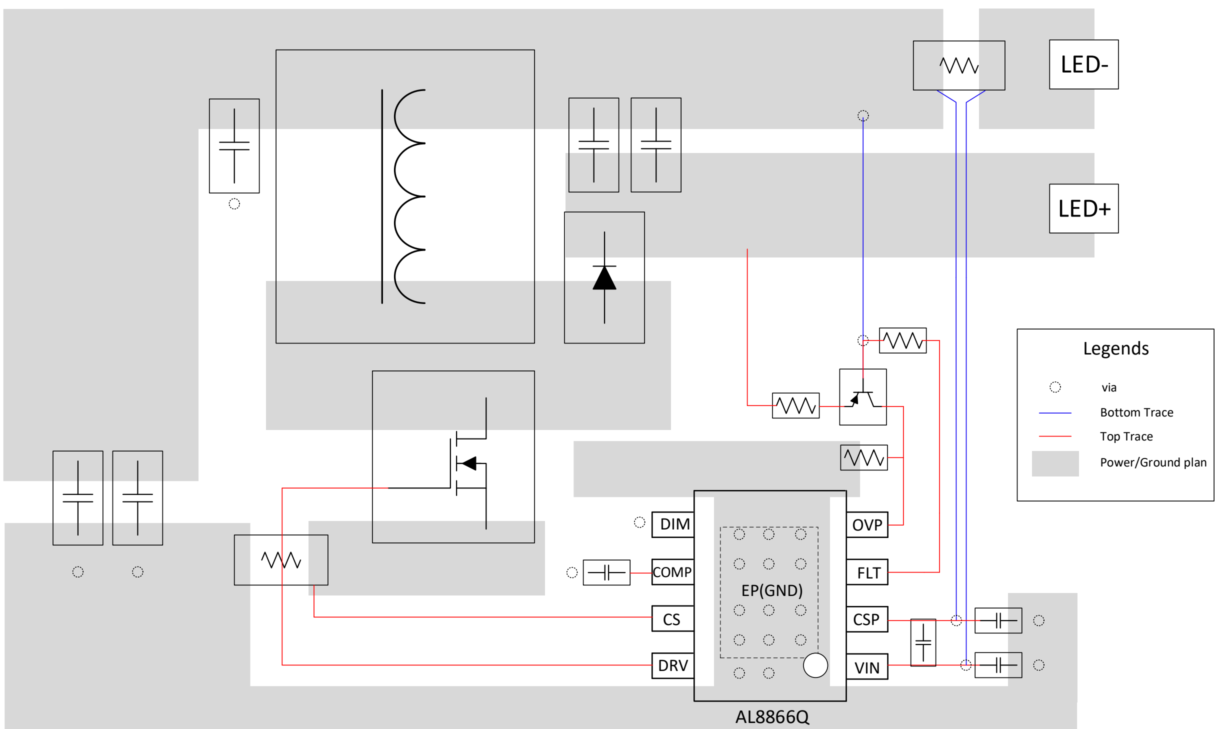


Figure 22 Recommend PCB Layout

Design Tools (Note 8)

- AL8866Q Demo Boards
- AL8866Q Calculator
- Demo Board Gerber File for PCB Layout Reference

Note: 8. Diodes Incorporated’s design tools can be found on our website at https://www.diodes.com/design/tools/.

Ordering Information

AL8866Q XX–XX

Product Name

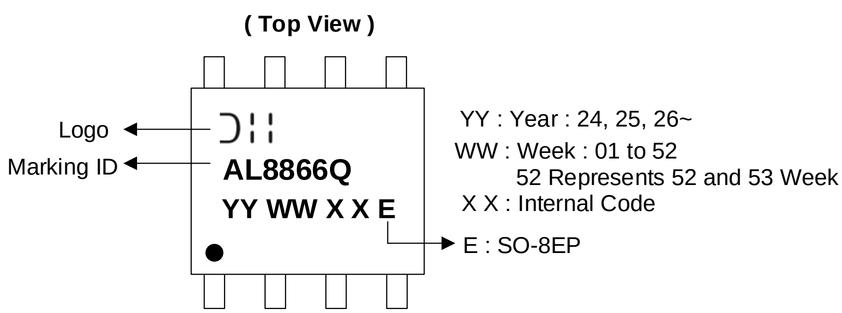
Package
SP: SO-8EP
FN: U-DFN3030-10

Packing
13: 13" Tape and Reel
7: 7" Tape and Reel

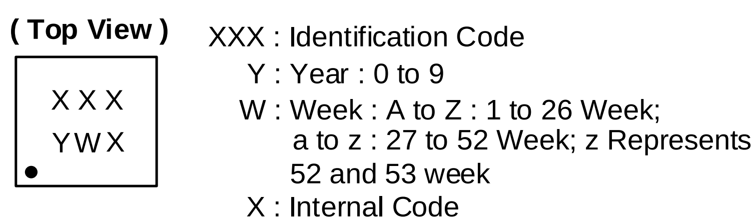
Orderable Part Number	Package Code	Package	Packing	
			Qty.	Carrier
AL8866QSP-13	SP	SO-8EP	2500	13” Tape & Reel
AL8866QFN-7	FN	U-DFN3030-10	1500	7” Tape & Reel

Marking Information

SO-8EP



U-DFN3030-10

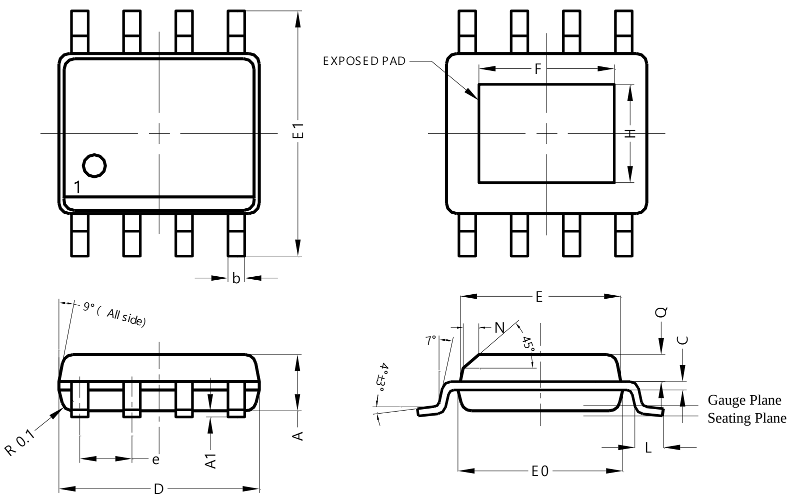


Orderable Part Number	Package	Identification Code
AL8866QFN-7	**U-DFN3030-10**	**PPQ**

Package Outline Dimensions (Note 9)

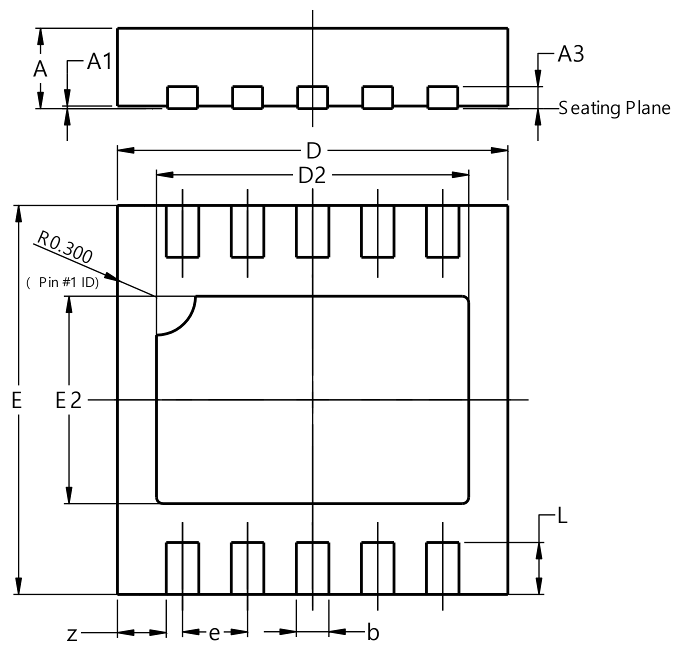
Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP



SO-8EP			
Dim	**Min**	**Max**	**Typ**
A	1.40	1.50	1.45
A1	0.00	0.13	-
b	0.30	0.50	0.40
C	0.15	0.25	0.20
D	4.85	4.95	4.90
E	3.80	3.90	3.85
E0	3.85	3.95	3.90
E1	5.90	6.10	6.00
e	-	-	1.27
F	2.75	3.35	3.05
H	2.11	2.71	2.41
L	0.62	0.82	0.72
N	-	-	0.35
Q	0.60	0.70	0.65
All Dimensions in mm			

U-DFN3030-10



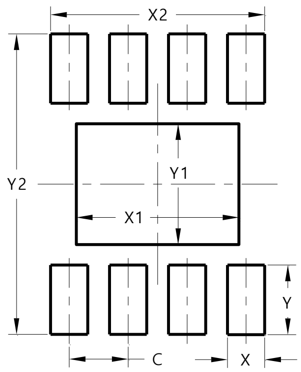
U-DFN3030-10			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0.00	0.05	0.02
A3	—	—	0.15
b	0.20	0.30	0.25
D	2.90	3.10	3.00
D2	2.30	2.50	2.40
E	2.90	3.10	3.00
E2	1.50	1.70	1.60
e	--	--	0.50
L	0.25	0.55	0.40
z	—	—	0.375
All Dimensions in mm			

Note: 9. Please see https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf for tape and reel information.

Suggested Pad Layout

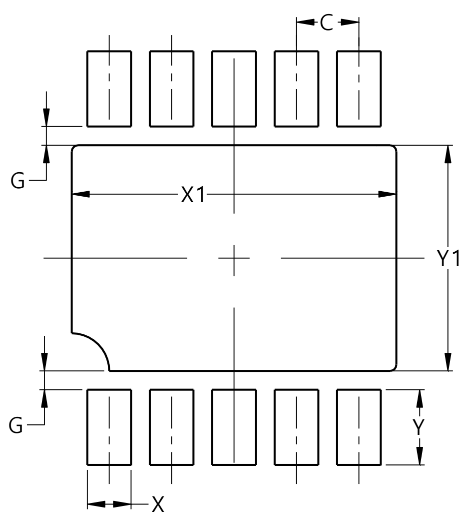
Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8EP



Dimensions	Value (in mm)
C	1.270
X	0.802
X1	3.502
X2	4.612
Y	1.505
Y1	2.613
Y2	6.500

U-DFN3030-10



Dimensions	Value (in mm)
C	0.50
G	0.15
X	0.35
X1	2.60
Y	0.60
Y1	1.80

Mechanical Data

SO-8EP:

- Moisture Sensitivity: MSL Level 1 per JESD22-A113
- Terminals: Finish - Matte Tin Plated Leads, Solderable per M2003 JESD22-B102 e3
- Weight: 0.077 grams (Approximate)

U-DFN3030-10:

- Moisture Sensitivity: MSL Level 1 per JESD22-A113
- Terminals: Finish - Matte NiPdAu Plated Leads, Solderable per M2003 JESD22-B102 e3
- Weight: 0.017 grams (Approximate)

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