This is a summary document. A complete document is available under NDA. For more information, please contact your local Microchip sales office.

CryptoAuthentication™ ATECC608C Summary Data Sheet

ATECC608C

Features

- Cryptographic Co-Processor with Secure Hardware-Based Key Storage:
  - Protected storage for up to 16 keys, certificates or data
- Hardware Support for Asymmetric Sign, Verify, Key Agreement:
  - ECDSA: FIPS186-3 Elliptic Curve Digital Signature
  - ECDH: FIPS SP800-56A Elliptic Curve Diffie-Hellman
  - NIST Standard P256 (ECC secp256r1) Elliptic Curve Support
- Hardware Support for Symmetric Algorithms:
  - SHA-256 & HMAC Hash including off-chip context save/restore
  - AES-128: Encrypt/Decrypt, Galois Field Multiply for GCM
- Networking Key Management Support:
  - Turnkey PRF/HKDF calculation for TLS 1.2 & 1.3
  - Ephemeral key generation and key agreement in SRAM
  - Small message encryption with keys entirely protected
- Secure Boot Support:
  - Full ECDSA code signature validation, optional stored digest/signature
  - Optional communication key disablement prior to secure boot
  - Encryption/Authentication for messages to prevent on-board attacks
- JIL High Rating – Validated to JIL Application of Attack Potential to Smartcards and Similar Devices, Version 3.1
- Internal High-Quality NIST SP 800-90A/B/C True Random Number Generator (TRNG), NIST CMVP ESV Certified
- Two High-Endurance Monotonic Counters
- Unique 72-Bit Serial Number
- Two Interface Options Available:
  - High-Speed Single Wire Interface with One GPIO Pin
  - 1 MHz Standard I^{2}C Interface
- 1.8V to 5.5V IO Levels, 2.0V to 5.5V Supply Voltage
- Two Temperature Ranges Available:
  - Standard Industrial Temperature Range: -40℃ to +85℃
  - Extended Industrial Temperature Range: -40℃ to +100℃
- <150 nA Sleep Current
- Packaging Options
  - 8-pad UDFN, 8-Lead SOIC and 3-Lead Contact Package Options
  - Die-on-Tape and Reel and WLCSP for Qualified Customers (Contact Microchip Sales)

Applications

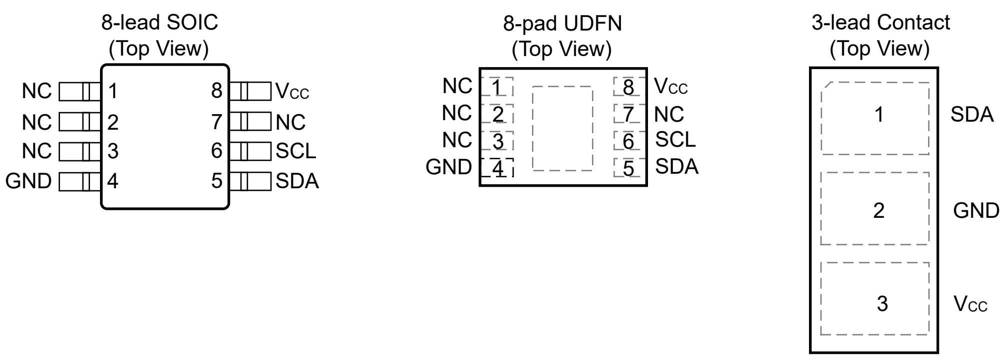
- IoT network endpoint key management & exchange
- Encryption for small messages and PII data
- Secure Boot and Protected Download
- Ecosystem Control, Anti-cloning

Pin Configuration and Pinouts

Table 1. Pin Configuration

Pin	Function I²C Interface	Function SWI Interface
NC	No Connect	No Connect
GND	Ground	Ground
SDA	Serial Data	Serial Data
SCL	Serial Clock Input	GPIO
V_{CC}	Power Supply	Power Supply

Figure 1. Package Types



Note: The UDFN backside paddle is recommended to be connected to GND.

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1. Introduction

The ATECC608C is a member of the Microchip CryptoAuthentication™ family of high-security cryptographic devices, which combine world-class, hardware-based key storage with hardware cryptographic accelerators to implement various authentication and encryption protocols.

The ATECC608C provides security enhancements over that of the ATECC608B, while providing backwards compatibility. All configuration settings, commands, packages and functionality of the ATECC608B are still available in the ATECC608C, making migration from the ATECC608B a simple process. For new designs, it is recommended that customers start directly with the ATECC608C device. For designs that are being upgraded and currently use the ATECC508A, ATECC608A or ATECC608B, it is recommended that they move to the ATECC608C. For designs not planned to be upgraded, it is recommended that customers review their designs to see if they would benefit from the enhanced security of the ATECC608C. For assistance with migrating a design to the ATECC608C, see the Migrations References section.

For more information on compatibility with other Microchip CryptoAuthentication products, please see 5. Compatibility.

Migration References:

1. AN3539: Provides guidance on migrating from the ATECC508A to the ATECC608B
2. AN2237: Provides guidance on migrating from the ATECC608A to the ATECC608B
3. AN5078: Provides guidance on migrating from the ATECC608B to the ATECC608C

1.1 Applications

The ATECC608C has a flexible command set that allows use in many applications, including the following:

- **Network/IoT Node Endpoint Security**
  Manages node identity authentication and session key creation and management. Supports the entire ephemeral session key-generation flow for multiple protocols, including TLS 1.2 (and earlier) and TLS 1.3.
- **Secure Boot**
  Supports the MCU host by validating code digests and optionally enabling communication keys on success. Various configurations to offer enhanced performance are available.
- **Small Message Encryption**
  Contains a hardware AES engine to encrypt and/or decrypt small messages or data such as PII information. Supports the AES-ECB mode directly. Other modes can be implemented with the help of the host microcontroller. There is an additional GFM calculation function to support AES-GCM.
- **Key Generation for Software Download**
  Supports local protected key generation for downloaded images. Both broadcast of one image to many systems, each with the same decryption key, or point-to-point download of unique images per system are supported.
- **Ecosystem Control and Anti-Counterfeiting**
  Validates that a system or component is authentic and came from the OEM shown on the nameplate.

1.2 Device Features

The ATECC608C includes an EEPROM array which can be used for storage of up to 16 keys, certificates, miscellaneous read/write, read-only or secret data, consumption logging and security configurations. Access to the various sections of memory can be restricted in a variety of ways and then the configuration can be locked to prevent changes.

Access to the device is made through a standard I^2C Interface at speeds of up to 1 Mbps. The interface is compatible with standard Serial EEPROM I^2C interface specifications. The device also supports a Single-Wire Interface (SWI), which can reduce the number of GPIOs required on the system processor, and/or reduce the number of pins on connectors. If the Single-Wire Interface is enabled, the remaining pin is available for use as a GPIO, an authenticated output or tamper input.

Each ATECC608C ships with an ensured unique 72-bit serial number. Using the cryptographic protocols supported by the device, a host system or remote server can verify a signature of the serial number to prove that the serial number is authentic and not a copy. Serial numbers are often stored in a standard Serial EEPROM; however, these can be easily copied with no way for the host to know if the serial number is authentic or if it is a clone.

The ATECC608C features a wide array of defense mechanisms specifically designed to prevent physical attacks on the device itself, or logical attacks on the data transmitted between the device and the system. Hardware restrictions on the ways in which keys are used or generated provide further defense against certain styles of attack.

1.3 Cryptographic Operation

The ATECC608C implements a complete asymmetric (public/private) key cryptographic signature solution based upon Elliptic Curve Cryptography and the ECDSA signature protocol. The device features hardware acceleration for the NIST standard P256 prime curve and supports the complete key life cycle from high quality private key generation, to ECDSA signature generation, ECDH key agreement and ECDSA public key signature verification.

The hardware accelerator can implement such asymmetric cryptographic operations from ten to one-thousand times faster than software running on standard microprocessors, without the usual high risk of key exposure that is endemic to standard microprocessors.

The ATECC608C also implements AES-128, SHA256 and multiple SHA derivatives such as HMAC(SHA), PRF (the key derivation function in TLS) and HKDF in hardware. Support is included for the Galois Field Multiply (aka Ghash) to facilitate GCM encryption/decryption/authentication.

The device is designed to securely store multiple private keys along with their associated public keys and certificates. The signature verification command can use any stored or an external ECC public key. Public keys stored within the device can be configured to require validation via a certificate chain to speed up subsequent device authentications.

Random private key generation is supported internally within the device to ensure that the private key can never be known outside of the device. The public key corresponding to a stored private key is always returned when the key is generated and it may optionally be computed at a later time.

The ATECC608C can generate high-quality random numbers using its internal random number generator. This sophisticated function includes runtime health testing designed to ensure that the values generated from the internal noise source contain sufficient entropy at the time of use. The random number generator is designed to meet the requirements documented in the NIST SP800-90A, SP800-90B and SP800-90C documents. The SP800-90B NRBG is FIPS140-3 ESV certified.

These random numbers can be employed for any purpose, including as part of the device's cryptographic protocols. Because each random number is ensured to be essentially unique from all numbers ever generated on this or any other device, their inclusion in the protocol calculation ensures that replay attacks (i.e., re-transmitting a previously successful transaction) will always fail.

The ATECC608C also supports a standard hash-based challenge-response protocol to allow its use across a wide variety of additional applications. In its most basic instantiation, the system sends a challenge to the device, which combines that challenge with a secret key via the MAC command and then sends the response back to the system. The device uses a SHA-256 cryptographic hash algorithm to make that combination so that an observer on the bus cannot derive the value of the secret key. At the same time, the recipient can verify that the response is correct by performing the same calculation with a stored copy of the secret on the recipient’s system. There are a wide variety of variations possible on this symmetric challenge/response theme.

2. Security Information

2.1 Cryptographic Standards

The ATECC608C follows various industry standards for the computation of cryptographic results. These reference documents are described in the following sections.

2.1.1 SHA-256

The ATECC608C computes the SHA-256 digest based upon the algorithm documented in the following site:

nvlpubs.nist.gov/nistpubs/FIPS/NIST.FIPS.180-4.pdf

2.1.2 HMAC/SHA-256

The ATECC608C can compute an HMAC digest based upon SHA-256 using a key stored in the EEPROM as documented below:

http://csrc.nist.gov/publications/fips/fips198-1/FIPS-198-1_final.pdf

2.1.3 TLS V1.2 Pseudo Random Function (PRF)

The ATECC608C KDF(PRF) command calculates the key derivation function (KDF) specified for TLSV1.2 (and earlier) at:

tools.ietf.org/html/rfc5246

2.1.4 HMAC-based Extract-and-Expand KDF (HKDF)

The ATECC608C KDF(HKDF) command calculates the HKDF key derivation function (KDF). This is the KDF that is used in the TLS1.3 specification. It is specified at:

tools.ietf.org/html/rfc5869

2.1.5 Elliptic Curve Digital Signature Algorithm (ECDSA)

The ATECC608C computes and verifies the Elliptic Curve signatures according to the algorithm documented in:

- ANSI X9.62-2005 www.ansi.org/
- FIPS 186-5 specification nvlpubs.nist.gov/nistpubs/FIPS/NIST.FIPS.186-5.pdf

2.1.6 Elliptic Curve Diffie-Hellman (ECDH)

The ATECC608C executes the ECDH key agreement according to NIST Special Publication 800-56A recommendations:

nvlpubs.nist.gov/nistpubs/SpecialPublications/NIST.SP.800-56Ar2.pdf

2.1.7 Advanced Encryption Standard (AES)

Symmetric encryption & decryption, if enabled, is implemented via the AES command using only AES-128 per:

nvlpubs.nist.gov/nistpubs/FIPS/NIST.FIPS.197.pdf

2.2 Certifications

As part of the overall development effort of the ATECC608C, Microchip Technology worked in concert with certified industry laboratories to perform extensive certification and validation procedures. The following subsections provide more information on the certification and validation testing performed.

2.2.1 NIST CAVP Algorithm Certifications

The ATECC608C algorithms were certified through the NIST Cryptographic Algorithm Validation Program (CAVP) working in conjunction with a NIST certified laboratory. Microchip Technology was issued the following CAVP certificate numbers, attesting that the following algorithms are in compliance to NIST standards.

- A4280: All algorithms other than AES-GCM
- A4285: AES-GCM

Table 2-1. ATECC608C Certified CAVP algorithms

• AES-ECB	• SHA2-256	• ECDSA KeyGen (FIPS186-5)
• AES-GCM	• Counter DRBG	• ECDSA SigVer (FIPS186-5)
• ECDSA KeyVer (FIPS186-5)	• ECDSA SigGen (FIPS186-5)	• KDF TLS
• HMAC-SHA-256	• KAS-ECC-SSC SP800-56Ar3	

2.2.2 Vulnerability Analysis

The ATECC608C device was evaluated by a third Party SOGIS certified laboratory on its overall vulnerability resistance to attack in accordance with the Joint Interpretation Laboratory (JIL) methodologies and standards. The device achieved the highest possible rating of JIL HIGH when measured against the JIL rating score defined in the JIL standard: Application of Attack Potential to Smartcards and Similar Devices version 3.1.

2.2.3 RNG Certifications

The ATECC608C True Random Number Generator (TRNG) was developed in accordance with the NIST SP800-90A/B/C specifications. The DRBG and NRBG elements of the design were evaluated using a NIST certified laboratory to the procedures they have specified.

- **DRBG Certification:** The Deterministic Random Bit Generator (DRBG) was evaluated as part of the ATECC608C CAVP certification activity resulting in certificate number A4280. NIST validated and attests that the DRBG, implemented as a Counter DRBG algorithm, complies with the SP800-90A specification.
- **NRBG Certification:**The ATECC608C NRBG Entropy Source module was certified through the NIST Cryptographic Module Validation (CMVP) Entropy Source Validation (ESV) program working in conjunction with a NIST certified laboratory. Microchip Technology was issued Entropy Certificate #E46 by NIST. NIST validated and attests that the "ECC608 NRBG Entropy Source" module complies to the SP800-90B standard with a ring oscillator-based architecture for a physical non-deterministic random bit generator module that can be reused in product revisions of the ATECC608. This attestation is being extended to the ATECC608C revision of the product. The E46 certificate will be updated on the NIST validation site when the NIST extension review is complete.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Operating Temperature	-40°C to +100°C
Storage Temperature	-65°C to +150°C
Maximum Operating Voltage	6.0V
DC Output Current	5.0 mA
Voltage on any pin -0.5V to (V_{CC} + 0.5V)	-0.5V to (V_{CC} + 0.5V)
ESD Ratings:	
Human Body Model(HBM) ESD	>4 kV
Charge Device Model(CDM) ESD	>1 kV

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Reliability

The ATECC608C is fabricated with Microchip's high reliability CMOS EEPROM manufacturing technology.

Table 3-1. EEPROM Reliability

Parameter	Min.	Typ.	Max.	Units
Write Endurance at +85°C (Each Byte)	400,000	—	—	Write Cycles
Data Retention at +70°C	15	—	—	Years
Data Retention at +55°C	45	—	—	Years
Read Endurance	Unlimited			Read Cycles

3.3 AC Parameters: All I/O Interfaces

Figure 3-1. Wake Timing: All Interfaces

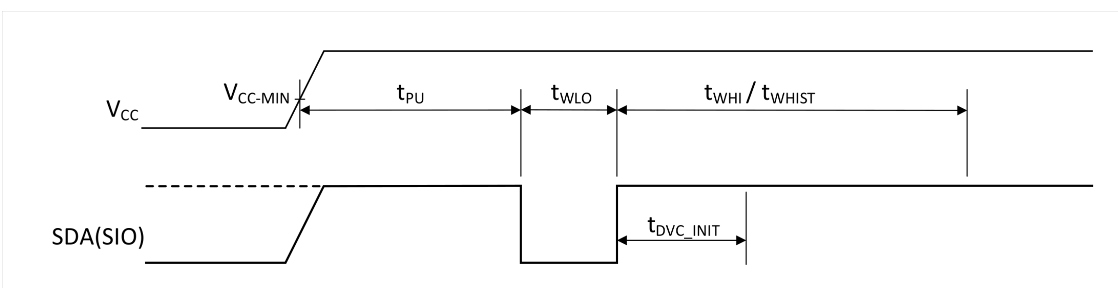


Figure 3-2. Input Noise Suppression: All Interfaces

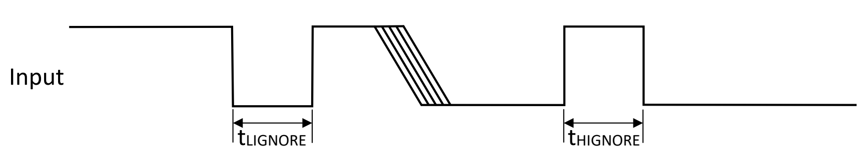


Table 3-2. AC Parameters: All I/O Interfaces

Parameter	Sym.	Direction	Min.	Typ.	Max.	Units	Conditions
Power-Up Delay	t_{PU}	To Crypto Device	100	—	—	µs	Minimum time between V_{CC} > V_{CC} min prior to start of t_{WLO}.
Wake Low Duration	t_{WLO}	To Crypto Device	60	—	—	µs	—
Initialization Time[1]	t_{DVC_INIT}	Internal	—	—	400	µs	Maximum time from rising edge of wake pulse until device is initialized.[2]
Wake High Delay to Data Comm	t_{WHI}	To Crypto Device	1500	—	—	µs	SDA is recommended to be stable high for this entire duration unless polling is implemented. SelfTest is not enabled at power-up.
Wake High Delay when SelfTest is Enabled	t_{WHIST}	To Crypto Device	20	—	—	ms	SDA is recommended to be stable high for this entire duration unless polling is implemented.
High-Side Glitch Filter at Active[1]	$t_{HIGNORE\_A}$	To Crypto Device	45	—	—	ns	Pulses shorter than this in width will be ignored by the device, regardless of its state when active.
Low-Side Glitch Filter at Active[1]	$t_{LIGNORE\_A}$	To Crypto Device	45	—	—	ns	Pulses shorter than this in width will be ignored by the device, regardless of its state when active.
Low-Side Glitch Filter at Sleep[1]	$t_{LIGNORE\_S}$	To Crypto Device	15	—	—	µs	Pulses shorter than this in width will be ignored by the device when in Sleep mode.
Watchdog Time-out	$t_{WATCHDOG}$	To Crypto Device	0.7	1.3	1.7	s	Time from wake until device is forced into Sleep mode if Config.ChipMode[2] is 0.

Notes:

1. These parameters are characterized, but not production tested.
2. No communications, other than the wake pulse, on the I^2C bus is recommended until after t_{DVC_INIT} time has passed.

3.3.1 AC Parameters: Single-Wire Interface

Figure 3-3. AC Timing Diagram: Single-Wire Interface

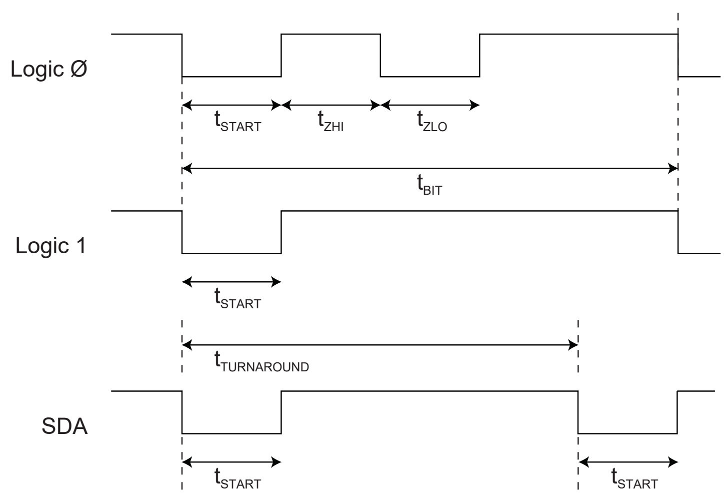


Table 3-3. AC Parameters: Single-Wire Interface
Unless otherwise specified, applicable from T_A = -40°C to +100°C, V_{CC} = +2.0V to +5.5V, C_L = 100 pF.

Parameter	Symbol	Direction	Min.	Typ.	Max.	Unit	Conditions
Start Pulse Duration	t_{START}	To Crypto Device	4.10	4.34	4.56	μs	—
		From Crypto Device	4.60	6	8.60	μs	—
Zero Transmission High Pulse	t_{ZHI}	To Crypto Device	4.10	4.34	4.56	μs	—
		From Crypto Device	4.60	6	8.60	μs	—
Zero Transmission Low Pulse	t_{ZLO}	To Crypto Device	4.10	4.34	4.56	μs	—
		From Crypto Device	4.60	6	8.60	μs	—
Bit Time[(1)]	t_{BIT}	To Crypto Device	37	39	—	μs	If the bit time exceeds $t_{TIMEOUT\text{-}SWI}$, ATECC608C may enter Sleep mode.
		From Crypto Device	41	54	78	μs	—
Turn Around Delay	$t_{TURNAROUND}$	From Crypto Device	64	96	131	μs	ATECC608C will initiate the first low going transition after this time interval following the initial falling edge of the start pulse of the last bit of the transmit flag.
		To Crypto Device	93	—	—	μs	After ATECC608C transmits the last bit of a group, the system must wait this interval before sending the first bit of a flag. It is measured from the falling edge of the start pulse of the last bit transmitted by ATECC608C.
IO Timeout	$t_{TIMEOUT\text{-}SWI}$	To Crypto Device	45	65	85	ms	ATECC608C may transition to the Sleep mode if the bus is inactive longer than this duration.

Note:

1. t_{START}, t_{ZLO}, t_{ZHI} and t_{BIT} are designed to be compatible with a standard UART running at 230.4 kBaud for both transmit and receive. The UART must be set to seven data bits, no parity and one Stop bit.

3.3.2 AC Parameters: I²C Interface

Figure 3-4. I²C Synchronous Data Timing

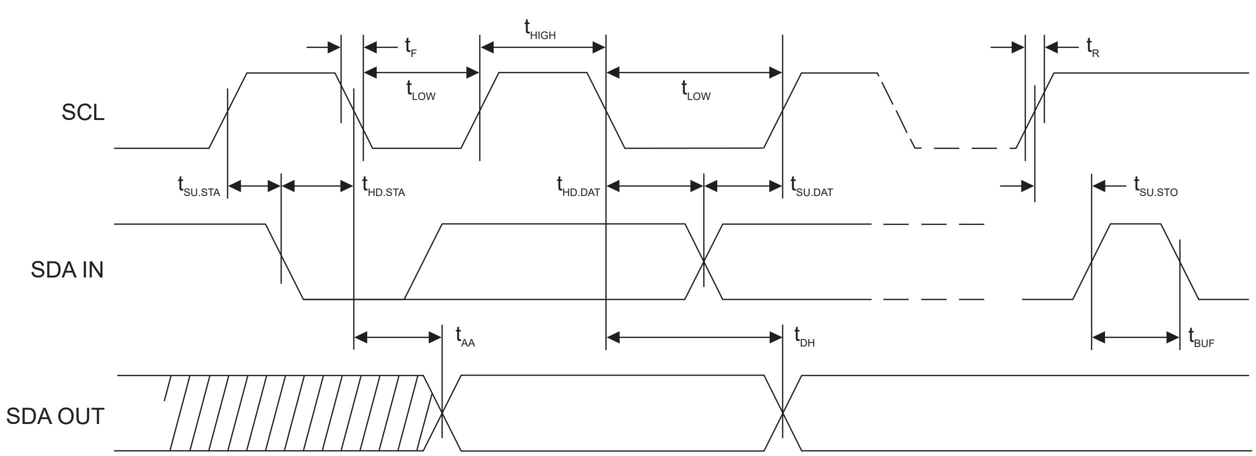


Table 3-4. AC Characteristics of I^2C Interface[2]
Unless otherwise specified, applicable over recommended operating range from T_A = -40°C to +100°C, V_{CC} = +2.0V to +5.5V, C_L = 1 TTL Gate and 100 pF.

Parameter	Sym.	Min.	Max.	Units
SCL Clock Frequency	f_{SCL}	0	1	MHz
SCL High Time	t_{HIGH}	400	—	ns
SCL Low Time	t_{LOW}	400	—	ns
Start Setup Time	$t_{SU.STA}$	250	—	ns
Start Hold Time	$t_{HD.STA}$	250	—	ns
Stop Setup Time	$t_{SU.STO}$	250	—	ns
Data In Setup Time	$t_{SU.DAT}$	100	—	ns
Data In Hold Time	$t_{HD.DAT}$	0	—	ns
Input Rise Time[1]	t_R	—	300	ns
Input Fall Time[1]	t_F	—	100	ns
Clock Low to Data Out Valid	t_{AA}	50	550	ns
Data Out Hold Time	t_{DH}	50	—	ns
SMBus Time-Out Delay	$t_{TIMEOUT}$	25	35	ms
Time bus must be free before a new transmission can start[1]	t_{BUF}	500	—	ns

Notes:
1. Values are based on characterization and are not tested.
2. AC measurement conditions:
   - R_L (connects between SDA and V_{CC}): 1.2 kΩ (for V_{CC} = +2.0V to +5.0V)
   - Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
   - Input rise and fall times: ≤ 50 ns
   - Input and output timing reference voltage: $0.5V_{CC}$

3.4 DC Parameters: All I/O Interfaces

Table 3-5. DC Parameters on All I/O Interfaces

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Ambient Operating Temperature	T_A	-40	—	+85	°C	Standard Industrial Temperature Range
		-40	—	+100	°C	Extended Industrial Temperature Range
Power Supply Voltage	V_{CC}	2.0	—	5.5	V	—
Active Power Supply Current	I_{CC}	—	2	3	mA	Waiting for I/O during I/O transfers or execution of non-ECC commands. Independent of Clock Divider value.
		—	—	14	mA	During ECC command execution. Clock divider = 0x0
		—	—	6	mA	During ECC command execution. Clock divider = 0x5
		—	—	3	mA	During ECC command execution. Clock divider = 0xD
Idle Power Supply Current	I_{IDLE}	—	800	—	μA	When device is in Idle mode, V_{SDA} and V_{SCL} < 0.4V or > V_{CC} – 0.4
Sleep Current	I_{SLEEP}	—	30	150	nA	When device is in Sleep mode, V_{CC} ≤ 3.6V, V_{SDA} and V_{SCL} < 0.4V or > V_{CC} – 0.4, T_A ≤ +55°C
		—	—	2	μA	When device is in Sleep mode. Over full V_{CC} range and -40°C to 85°C temperature range.
		—	—	3	μA	When device is in Sleep mode. Over full V_{CC} range and -40°C to 100°C temperature range.

...........continued						
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Low Voltage	V_{OL}	—	—	0.4	V	When device is in Active mode, V_{CC} = 2.5 to 5.5V
Output Low Current	I_{OL}	—	—	4	mA	When device is in Active mode, V_{CC} = 2.5 to 5.5V, V_{OL} = 0.4V
Theta JA	θ_{JA}	—	166	—	°C/W	SOIC (SS)
		—	173	—	°C/W	UDFN (MA)
		—	146	—	°C/W	3-Lead Contact (RB)

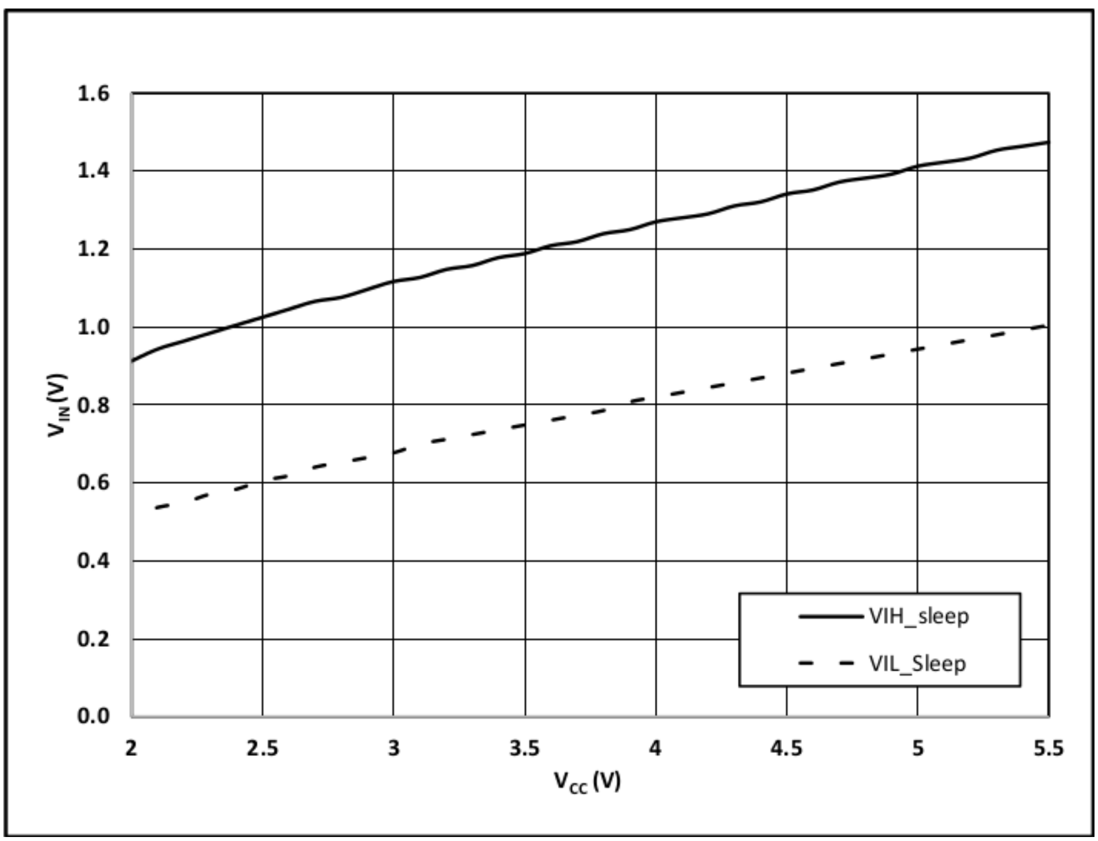
3.4.1 V_{IH} and V_{IL} Specifications

The input levels of the device will vary dependent on the mode and voltage of the device. The input voltage thresholds when in Sleep or Idle mode are dependent on the V_{CC} level as shown in Figure 3-5. When in Sleep or Idle mode the TTLenable bit has no effect.

Table 3-6. V_{IL}, V_{IH} on All I/O Interfaces (TTLenable = 0)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Low Voltage	V_{IL}	-0.5	—	0.5	V	When device is active and TTLenable bit in Configuration memory is zero; otherwise, see above.
Input High Voltage	V_{IH}	1.5	—	V_{CC} + 0.5	V	When device is active and TTLenable bit in Configuration memory is zero; otherwise, see above.

Figure 3-5. V_{IH} and V_{IL} in Sleep and Idle Mode



4. ATECC608C Trust Platform Variants and Provisioning Services

Microchip provides a variety of pre-configured variants of the ATECC608C secure elements and a suite of tools to assist customers in developing applications using secure elements while minimizing the learning curve associated with cryptographic security.

Microchip offers secure provisioning services for the ATECC608C through the Trust Platform. It leverages the Trust Platform Design Suite set of tools (TPDS), and offers 3 provisioning flows:

- Trust&GO: Pre-configured and pre-provisioned Secure Elements for fix-function Use Cases
- TrustFLEX: Pre-configured & provisioned Secure Element with customer-unique credentials
- TrustCUSTOM: Fully customizable Secure Element including configuration and provisioning with customer-unique credentials

The Trust&GO flow provides pre-configured and pre-provisioned secure elements. These products are defined to meet common use case applications for customers that do not require unique credentials. These devices are provided as is and can be ordered directly from Microchip as easily as any standard product.

The TrustFLEX flow leverages the TrustFLEX configurator to input unique customer credentials into a pre-defined configuration and generate a Secure Exchange Package. This package is, then, deployed via the Microchip Secure Provisioning System to enable device ordering. Then, only the customer designated in the Secure Exchange Package can order these devices.

The TrustCUSTOM flow leverages the TrustCUSTOM configurator and provides the ability to fully configure the ATECC608C device to meet the security requirements for a given application. At the end of the process, a Secure Exchange Package is generated that is deployed to the Microchip Secure Provisioning System. Then, only the customer designated in the Secure Exchange Package can order these devices.

Important: The Microchip Secure Provisioning System is based on Hardware Security Modules (HSMs).

Table 4-1. ATECC608C Trust Platform Ordering Codes[(1)]

Trust Platform Type	Production Ordering Code	Package Type	Temperature Range
Trust&GO[(2)]	ATECC608C-TNGTLSU	8-Pad UDFN	Standard Industrial. -40℃ to 85℃
	ATECC608C-TNGTLSS	8-Pin SOIC	Standard Industrial. -40℃ to 85℃
TrustFLEX[(2)]	ATECC608C-TFLXTLSU	8-Pad UDFN	Standard Industrial. -40℃ to 85℃
	ATECC608C-TFLXTLSS	8-Pin SOIC	Standard Industrial. -40℃ to 85℃
TrustCUSTOM[(3)]	ATECC608C-TCSMU	8-Pad UDFN	Standard Industrial. -40℃ to 85℃
	ATECC608C-TCSMS	8-Pin SOIC	Standard Industrial. -40℃ to 85℃

Notes:
1. This table is a representative sample of Trust Platform Devices. Please refer to each Trust Platform Type for a more complete list.
2. For a complete list of ordering codes, including sample devices, see the respective Trust&GO or TrustFLEX data sheets.
3. TrustCUSTOM sample devices correspond to the standard blank ATECC608C devices. ATECC608C-TCSMU / ATECC608C-TCSMS is equivalent to ATECC608C-MAHDA / ATECC608C-SSHDA.

5. Compatibility

5.1 Microchip ATECC608B

The ATECC608C is designed to provide enhanced security capabilities over that of the ATECC608B while maintaining backwards compatibility. The following details the changes and enhancements to the device. No configuration bit fields, voltage ranges, temperature ranges, package pinouts or power specifications have changed. Configurations defined for the ATECC608C will be functionally identical with the ATECC608B device.

Corrections, Enhancements

The following items were corrected or enhanced in the ATECC608C device:

- Low Temperature Lock-up issue after power-up state was corrected.
- t_{DVC_INIT} time was added to the data sheet. It is recommended that communications on the I^2C bus not occur until after this time has passed.
- Updated timing diagrams were added to the AC Characteristics. (Figure 3-1 and Figure 3-2)
- The `Read` command execution time increased from 2.0 ms to 2.5 ms max.

5.2 Microchip ATECC608A

The ATECC608B is designed to provide an enhanced security profile over that of the ATECC608A while maintaining backwards compatibility. The following details the changes and enhancements to the device. No configuration bit fields have changed. Configurations defined for the ATECC608A will be functionally identical with the ATECC608B device.

Corrections, Enhancements

The following items have been corrected or enhanced in the ATECC608B device:

- Two temperature ranges are now available:
  - Standard Industrial Temperature Range: -40℃ to +85℃
  - Standard Industrial Temperature Range: -40℃ to +100℃
- Operating at a low I^2C Frequency with multiple devices on the bus will no longer create a bus contention issue.
- Modifications to Command Timings for `Verify`, `SecureBoot`, `Lock` and `Read` commands.
- New Packaging Options: 3-Lead Contact Package and WLCSP for qualified customers. (Contact Microchip Sales for the WLCSP Option.)

5.3 Microchip ATECC508A

The ATECC608A is designed to be fully compatible with the ATECC508A devices with the limited exception of the functions listed below. If the ATECC608A is properly configured, software written for the ATECC508A will work with the ATECC608A without any required changes, again with the exception of the functions listed below.

Note: Most elements of the configuration zone in the ATECC608A are identical in both location and value with the ATECC508A. However, the initial values that had been stored in the LastKeyUse field may need to be changed to conform to the new definition of those bytes which can be found in this document. That field contained the initial count for the Slot 15 limited use function which is supported in the ATECC608A via the monotonic counters.

⚠ CAUTION The execution times of commands have changed between the ATECC608A and the ATECC508A. These changes will not cause an issue if polling has been implemented. If fixed timing has been used, this must be evaluated and updated as required.

New Features in ATECC608A vs. ATECC508A

- Secure boot function with IO encryption and authentication
- `KDF` command, supporting PRF, HKDF, AES
- `AES` command, including encrypt/decrypt
- GFM calculation function for GCM AEAD mode of AES
- Updated NIST SP800-90 A/B/C Random Number Generator
- Flexible `SHA/HMAC` command with context save/restore
- `SHA` command execution time significantly reduced
- Volatile Key Permitting to prevent device transfer
- Transport Key Locking to protect programmed devices during delivery
- Counter Limit Match function
- Ephemeral key generation in SRAM, also supported with ECDH and KDF
- `Verify` command output can be validated with a MAC
- Encrypted output for ECDH
- Added self test command, optional automatic power-on self test
- Unaligned public key for built-in X.509 cert key validation
- Optional power reduction at increased execution time
- Programmable I^2C address after data (secret) zone lock

Features Eliminated in ATECC608A vs. ATECC508A

- `HMAC` command removed, replaced via new more powerful `SHA` command
- OTP consumption mode eliminated, now read only
- Pause command eliminated along with related Selector function in UpdateExtra
- Slot 15 special limited use eliminated, replaced with standard monotonic counter limited use
- `SHA` command no longer uses TempKey during the digest calculation and the result in TempKey is unchanged throughout the SHA operation. TempKey can however still be used to initialize the SHA for the HMAC_Start or to store the final digest.

5.4 Microchip ATSHA204A, ATECC108A

The ATECC608C is generally compatible with all ATSHA204/A and ATECC108/A devices. If properly configured, it can be used in most situations where these devices are currently employed. For ATSHA204A and ATECC108A compatibility restrictions, see the ATECC508A data sheet.

6. Package Marking Information

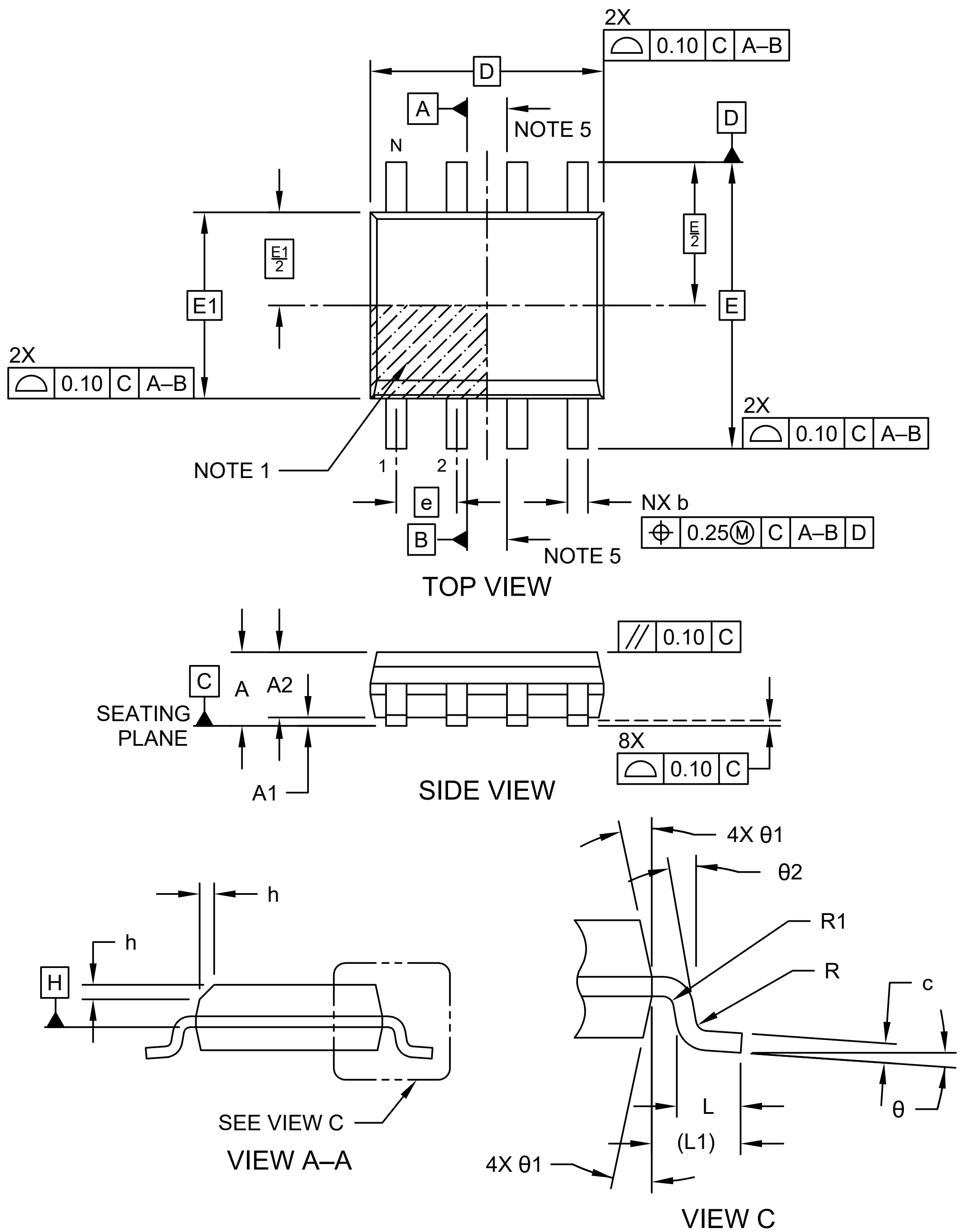
As part of Microchip's overall security features, the part marking for all crypto devices is intentionally vague. The marking on the top of the package does not provide any information as to the actual device type or the manufacturer of the device. The alphanumeric code on the package provides manufacturing information and will vary with assembly lot. It is recommended that the packaging mark not be used as part of any incoming inspection procedure.

7. Package Drawings

7.1 8-Lead SOIC

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

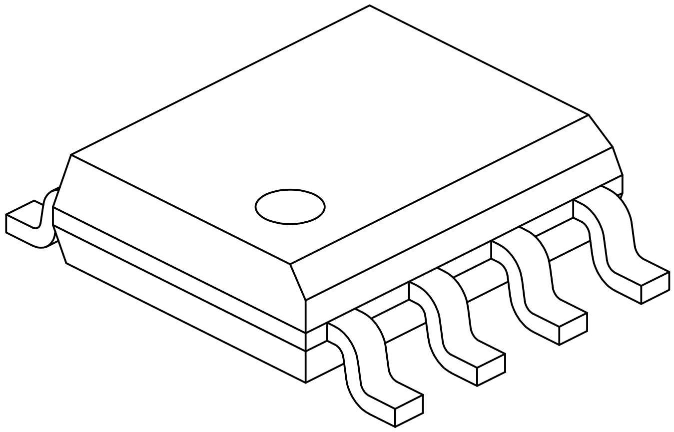
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC] Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

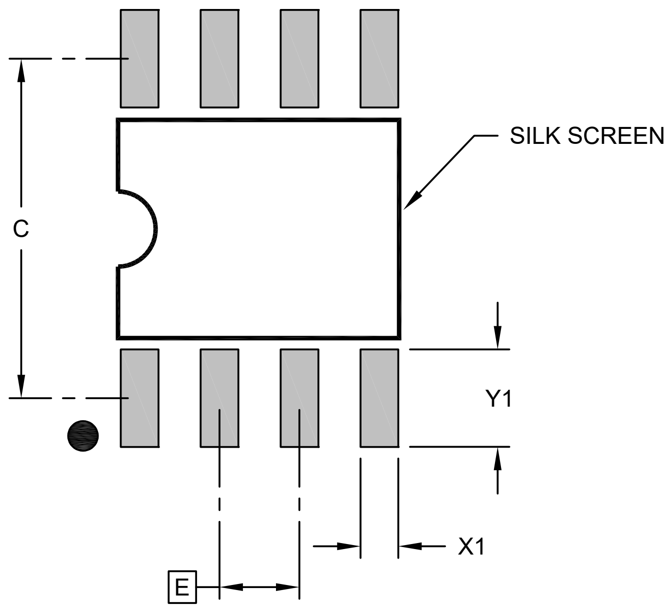
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

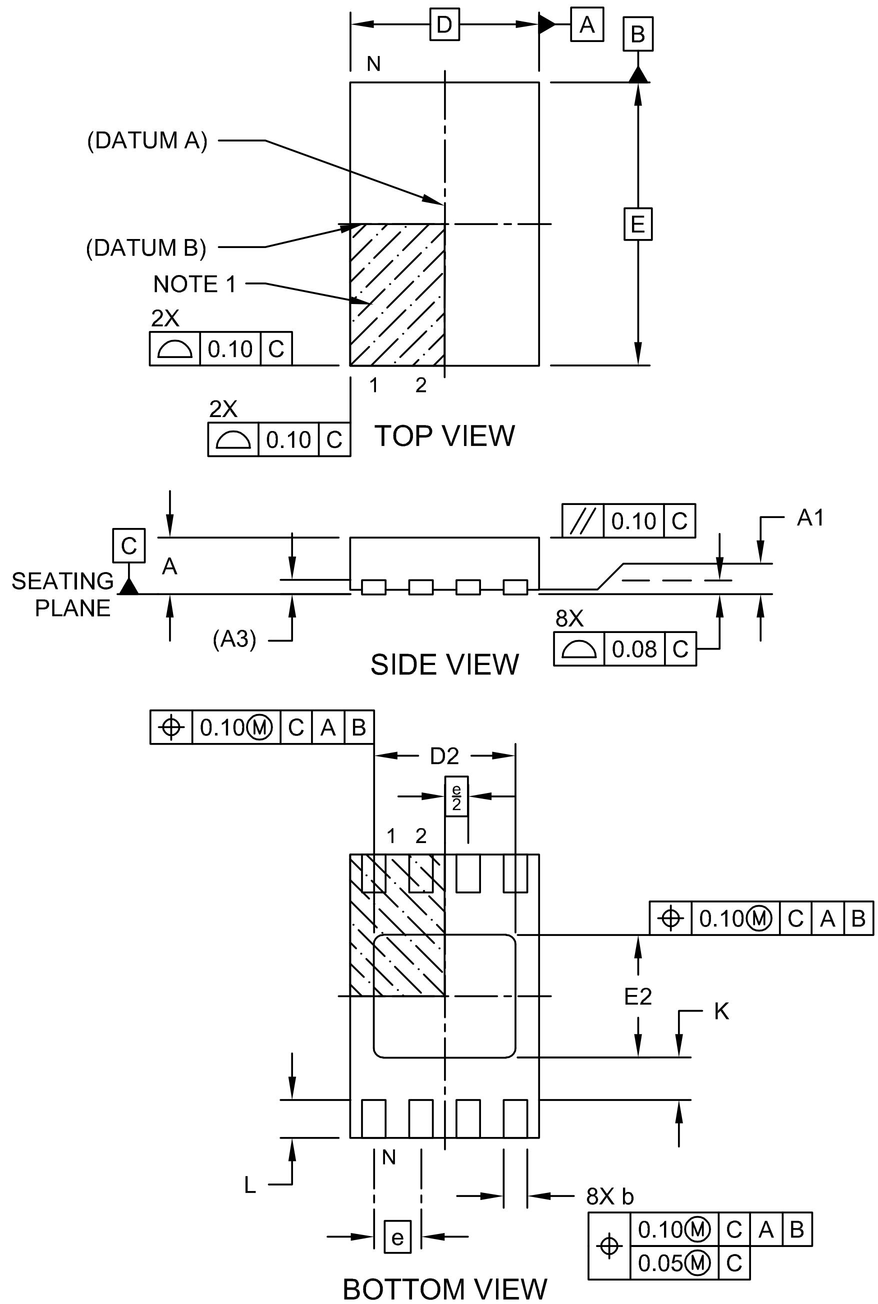
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

7.2 8-Pad UDFN

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

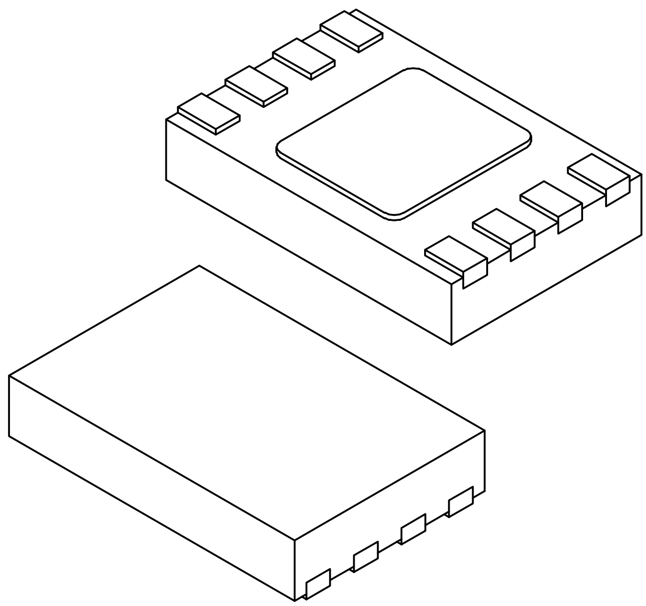
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 1 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN]
Atmel Legacy Global Package Code YNZ

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.40	1.50	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.20	1.30	1.40
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.25	0.35	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

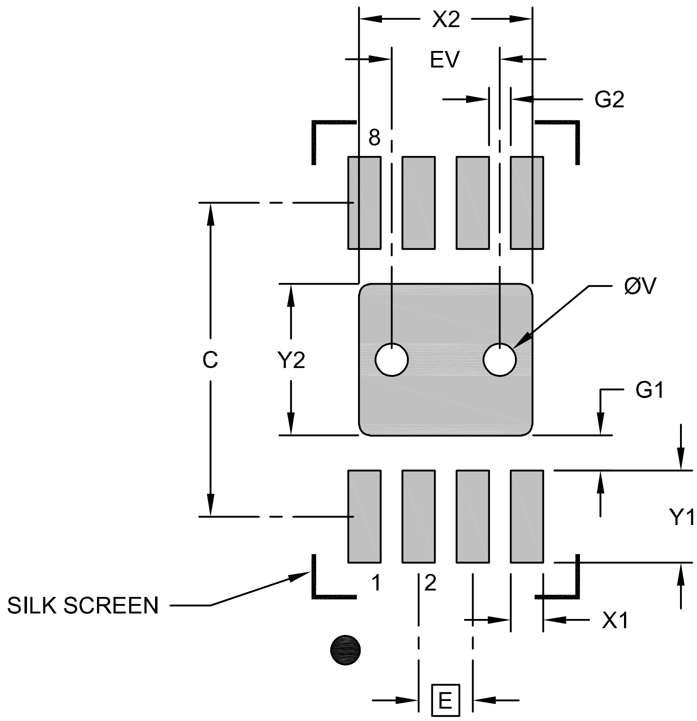
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21355-Q4B Rev C Sheet 2 of 2

8-Lead Ultra Thin Plastic Dual Flat, No Lead Package (Q4B) - 2x3 mm Body [UDFN] Atmel Legacy Global Package Code YNZ

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.40
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.85
Contact Pad to Center Pad (X8)	G1	0.33		
Contact Pad to Contact Pad (X6)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

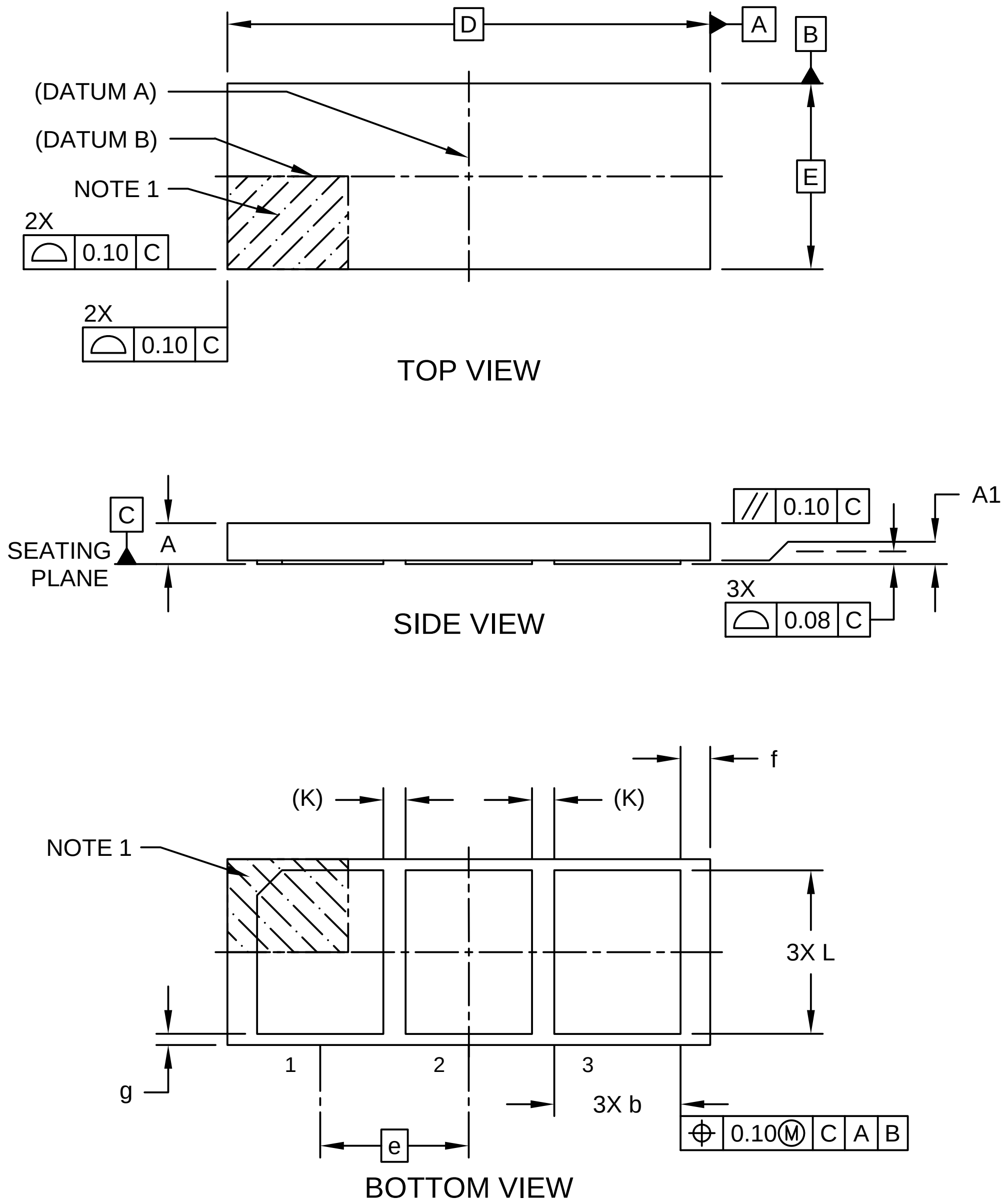
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23355-Q4B Rev C

7.3 3-Lead Contact

3-Lead Contact Package (LAB) - 6.54x2.5 mm Body [Contact]
Atmel Legacy Global Package Code RHB

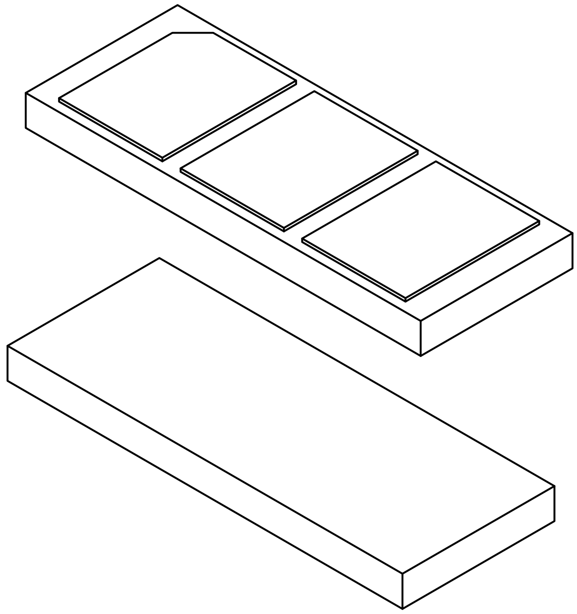
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21303 Rev A Sheet 1 of 2

3-Lead Contact Package (LAB) - 6.54x2.5 mm Body [Contact]
Atmel Legacy Global Package Code RHB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		3	
Pitch	e		2.00 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Overall Length	D		6.50 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b	1.60	1.70	1.80
Terminal Length	L	2.10	2.20	2.30
Terminal-to-Terminal Spacing	K		0.30 REF	
Package Edge to Terminal Edge	f	0.30	0.40	0.50
Package Edge to Terminal Edge	g	0.05	0.15	0.25

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21303 Rev A Sheet 2 of 2

8. Revision History

Revision B (November 2023)

- 2.1.5. Elliptic Curve Digital Signature Algorithm (ECDSA): Corrected specification value to FIPS 186-5
- 3.2. Reliability: Update to Data Retention values

Revision A (August 2023)

- Original Release. Based on ATECC608B - Summary Data Sheet DS40002239B

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PART NO.	-XX	X	XX	-X
Device	Package	Temp Range	I/O Type	Tape and Reel

Device:	ATECC608C: Cryptographic Co-processor with Secure Hardware-based Key Storage	
Package Options[3]	SS	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)
	MA	8-Pad 2 mm x 3 mm x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)
	RB	3RB, 3-Lead 2 mm x 5 mm x 6.5 mm Body, 2.0 mm pin pitch, Contact Package (Sawn)
Temperature Range	H	Standard Industrial Temperature Range: -40℃ to 85℃
	V	Extended Industrial Temperature Range: -40℃ to 100℃
I/O Type	CZ	Single Wire Interface
	DA	I²C Interface
Tape and Reel Options	B	Tube
	T	Large Reel (Size varies by package type)
	S	Small Reel (Only available for MA Package Type)

Device Ordering Codes

Temperature Range		Description
Standard Industrial	Extended Industrial	
ATECC608C-SSHCZ-T	ATECC608C-SSVCZ-T	8-Lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), Single-Wire, Tape and Reel, 4,000 per Reel
ATECC608C-SSHCZ-B	ATECC608C-SSVCZ-B	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), Single-Wire, Tube, 100 per Tube
ATECC608C-SSHDA-T[4]	ATECC608C-SSVDA-T	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), I²C, Tape and Reel, 4,000 per Reel
ATECC608C-SSHDA-B[4]	ATECC608C-SSVDA-B	8-Lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC), I²C, Tube, 100 per Tube
ATECC608C-MAHCZ-T	ATECC608C-MAVCZ-T	8-Pad 2 mm x 3 mm x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN), Single-Wire, Tape and Reel, 15,000 per Reel
ATECC608C-MAHDA-T[5]	ATECC608C-MAVDA-T	8-Pad 2 mm x 3 mm x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN), I²C, Tape and Reel, 15,000 per Reel
ATECC608C-MAHCZ-S	ATECC608C-MAVCZ-S	Pad 2 mm x 3 mm x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN), Single-Wire, Tape and Reel, 3,000 per Reel
ATECC608C-MAHDA-S[5]	ATECC608C-MAVDA-S	8-Pad 2 mm x 3 mm x 0.6 mm Body, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN), I²C, Tape and Reel, 3,000 per Reel
ATECC608C-RBHCZ-T	ATECC608C-RBVCZ-T	Single-Wire, Tape and Reel, 5,000 per Reel, 3-Lead Contact Package
ATECC608C-RBHCZ-B	ATECC608C-RBVCZ-B	Single-Wire, Tube, 56 per Tube, 3-Lead Contact Package

Notes:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
2. Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.
3. Die-on-Tape and Reel and WLCSP packages are available for qualified customers. Ordering codes for these packages are not shown in this table. Please contact Microchip sales for more information on these package options.
4. These products are also available as sample units for the TrustCUSTOM variant ATECC608B-TCSMS. More information on Trust Platform secure elements can be found in 4. ATECC608C Trust Platform Variants and Provisioning Services.
5. These products are also available as sample units for the TrustCUSTOM variant ATECC608B-TCSMU. More information on Trust Platform secure elements can be found in 4. ATECC608C Trust Platform Variants and Provisioning Services.

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