CBT3384

10-bit bus switch with 5-bit output enables

Rev. 9 — 25 June 2024 Product data sheet

1. General description

The CBT3384 is a dual 5-pole, single-throw bus switch. The device features two output enable inputs ($n\overline{OE}$) that each control five switch channels. The switches are disabled when the associated $n\overline{OE}$ input is HIGH. This device is fully specified for partial power down applications using I_{OFF}.

2. Features and benefits

- 5 Ω switch connection between two ports
- Direct interface with TTL levels
- Overvoltage tolerant control inputs to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBT3384PW	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Functional diagram

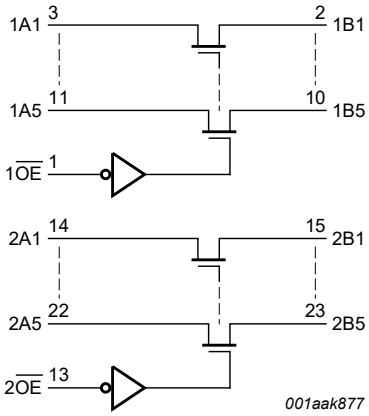
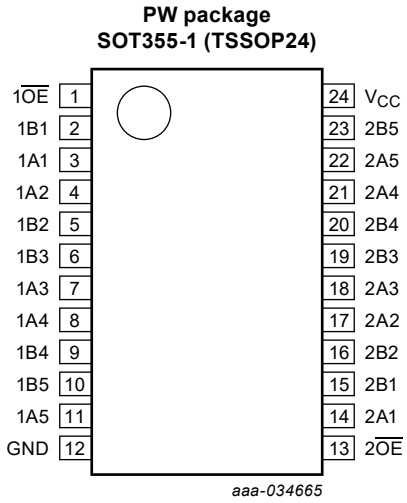


Fig. 1. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 13	output enable input (active LOW)
1A1, 1A2, 1A3, 1A4, 1A5	3, 4, 7, 8, 11	data input/output (A port)
2A1, 2A2, 2A3, 2A4, 2A5	14, 17, 18, 21, 22	data input/output (A port)
1B1, 1B2, 1B3, 1B4, 1B5	2, 5, 6, 9, 10	data input/output (B port)
2B1, 2B2, 2B3, 2B4, 2B5	15, 16, 19, 20, 23	data input/output (B port)
GND	12	ground (0 V)
V_{CC}	24	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input		Input/output	
$1\overline{OE}$	**$2\overline{OE}$**	**1An, 1Bn**	**2An, 2Bn**
L	L	1An = 1Bn	2An = 2Bn
L	H	1An = 1Bn	Z
H	L	Z	2An = 2Bn
H	H	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
I_O	output current	V_O < 0 V	-	±128	mA
I_{IK}	input clamping current	$V_{I/O}$ = 0 V	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = -18 mA	-	-	-1.2	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	-	3	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND [2]	-	-	2.5	mA
V_{pass}	pass voltage	output HIGH; V_I = V_{CC} = 5.0 V; I_O = -100 µA	3.6	3.9	4.2	V
C_I	input capacitance	control pins; V_I = 3 V or 0 V	-	4.0	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; V_I = 3 V or 0 V; $n\overline{OE}$ = V_{CC}	-	10.0	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA [3]	-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA [3]	-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = -15 mA [3]	-	10	15	Ω

[1] All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[3] Measured by the voltage drop between the nAn and the nBn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nAn or nBn) terminals.

10. Dynamic characteristics

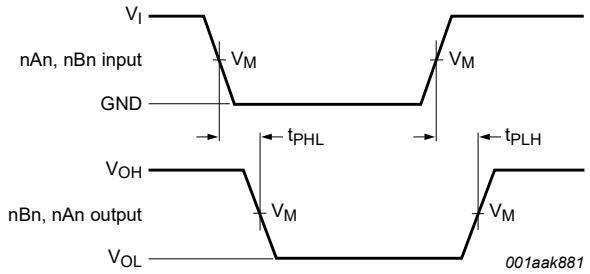
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 4.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{pd}	propagation delay	nAn, nBn to nBn, nAn; see Fig. 2 [1] [2]						
		V_{CC} = 5.0 V ± 0.5 V	-	-	0.25	-	0.25	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 3						
		V_{CC} = 5.0 V ± 0.5 V	1.2	2.3	5.7	1.2	5.6	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 3						
		V_{CC} = 5.0 V ± 0.5 V	1.2	2.3	5.7	1.2	6.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 3						
		V_{CC} = 5.0 V ± 0.5 V	1.7	3.6	5.2	1.7	5.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 3						
		V_{CC} = 5.0 V ± 0.5 V	1.7	2.7	5.2	1.7	6.6	ns

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

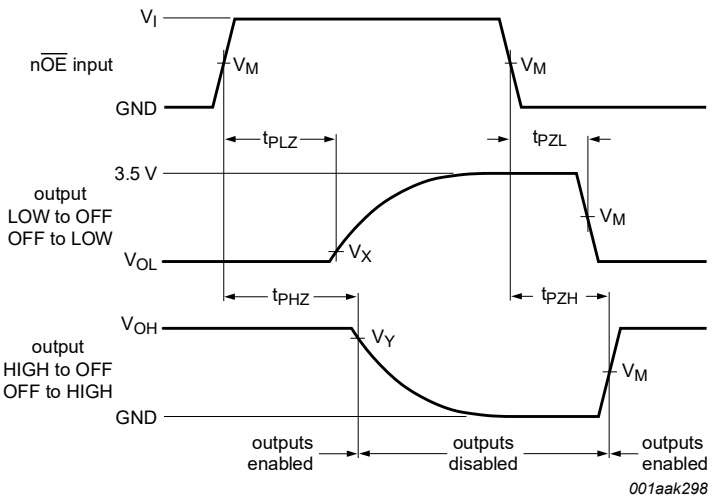
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 2. The data input (nAn, nBn) to output (nBn, nAn) propagation delay times



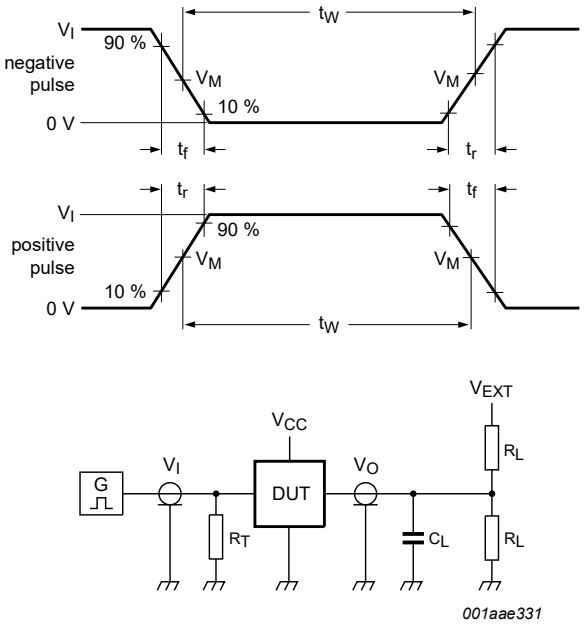
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 3. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

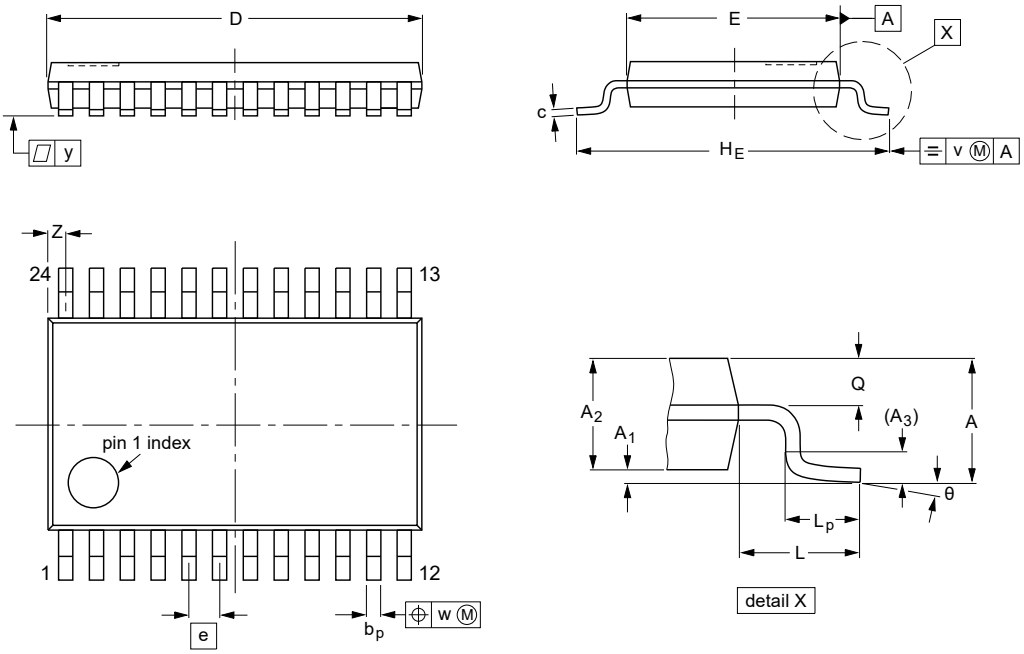
Fig. 4. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

11. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 5. Package outline SOT355-1 (TSSOP24)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3384 v.9	20240625	Product data sheet	-	CBT3384 v.8
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
CBT3384 v.8	20231113	Product data sheet	-	CBT3384 v.7
Modifications:	• Section 1 and Section 2 updated. • Type number CBT3384D (SOT137-1/SO24) removed.			
CBT3384 v.7	20190306	Product data sheet	-	CBT3384 v.6
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number CBT3384DB (SOT340-1) and CBT3384DK (SOT556-1) removed.			
CBT3384 v.6	20091102	Product data sheet	-	CBT3384 v.5

Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.
	• Legal texts have been adapted to the new company name where appropriate.
	• Changed: Table 6
	  • Pass voltage values have changed.
	  • Undershoot static current protection removed.
	• Changed: Table 7
	  • Enable and disable times values have changed.			

CBT3384 v.5	20011220	Product specification	-	CBT3384 v.4
CBT3384 v.4	20010319	Product specification	-	CBT3384 v.3
CBT3384 v.3	20001113	Product specification	-	CBT3384 v.2
CBT3384 v.2	20000128	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 25 June 2024