CEC173X-TFLX

Real Time Platform Root of Trust Controller

Hardware Features

- Hardware CNSA Based Secure Boot (P-384)
- AES256
- SHA-384
- ECDSA
- True Random Number Generator (SP800-90B)
- SPI Boot Flash Monitoring and Intervention (1.8V or 3.3V)
- Key Management Engine
- Hardware-Based Physically Unclonable Function (PUF)
- Differential Power Analysis Countermeasures
- User Configurable 3.3V or 1.8V Power Spec
- Internal Q-Switches
- Lifecycle Management
- 84-pin and 64-pin Package Sizes (7x7x0.8 mm and 5.5x5.5x0.92 mm)

Soteria-G3 Software Features

- NIST 800-193 and Open Compute Project Compliant
- Soteria-G3 code is cleared by MISRA, checked by Coverity® and CERT® C code analysis and certified by third-party penetration tests
- Secure Boot of up to two Application Processors and up to 16 AP FW images
- SPDM-Compliant Component Attestation
- Secure I^2C Crisis Recovery
- Secure Firmware Updates using PLDM and Crisis Recovery
- Transfer of Ownership
- Authentication Key Revocation
- Firmware Rollback Protection
- Run-time Status Reporting over I^2C
- Life Cycle Management

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1.0 GENERAL DESCRIPTION

The CEC173x-TFLX Trust Shield Family is the Real Time Platform Root of Trust Controller for Servers, Telecommunications, Networking, Industrials, and Embedded Computing applications.

The CEC173x-TFLX is a partially configured and provisioned variant of the CEC173x Trust Shield family of Real Time Platform Root of Trust Controllers. The devices come pre-provisioned with Soteria-G3 firmware, and the configuration enables customers to use unique credentials for Application Processor images.

The device configuration is designed to make CEC173x-TFLX support most common use cases, while minimizing the learning and development time to enable product quick time to market.

The CEC173x-TFLX is a highly configurable, mixed-signal, advanced I/O controller. It contains a 32-bit 96 MHz ARM® Cortex-M4F processor core with closely coupled memory for optimal code execution and data access.

The CEC173x-TFLX was designed to meet the NIST 800-193 Platform Resiliency Guidelines, as well as the Open Compute Project (OCP) Security Project requirements.

The immutable secure bootloader implemented in the CEC173x TrustFLEX ROM (Boot ROM) loads and authenticates the embedded controller firmware (EC_FW/Soteria-G3) from the internal SPI Flash. The Authenticated EC_FW (Soteria-G3) will then authenticate and validate Application Processor image stored in external SPI Flash.

The validated EC_FW (Soteria-G3) along with the Boot ROM code supports many additional security features of the device, including Key revocation, Code Rollback Protection and Transfer of Ownership. In addition, the Boot ROM implements Life Cycle Management and SPDM for Attestation. The SPDM implementation in EC_FW (Soteria-G3) supports commands that return certificates and measurement information for attestation.

Both the Boot ROM and the EC_FW (Soteria-G3) support more than one public key for image authentication and key revocation. A public key may be revoked, i.e., taken out of service, if the private key becomes compromised.

The Boot ROM and the EC_FW also support Rollback Protection, which prevents certain firmware images from being permitted to run in a system. This feature is used if an older image version may compromise the system security.

The CEC173x TrustFLEX SPI Flash Monitor blocks, one instance per Host, maintain Host firmware integrity both during Host Boot and Host Runtime. At Host Boot, it calculates and verifies signatures of the loaded code blocks in real time, while also verifying that the Host's firmware is executing the correct opcodes from Flash. At Host Runtime, it verifies that only legal Flash accesses are performed, using regional access permission settings, and that no illegal or questionable opcodes (such as Chip Erase) are attempted. Upon seeing an attempted violation of SPI integrity or access rules, it will intervene in real time, in such a way as to cancel a Read, Write, Program or Erase before it can be performed. The Intervention technique works with even the most economical 8-pin standard NOR Flash devices.

The CEC173x TrustFLEX also contains a core Crypto hardware accelerator engine supporting SHA-384, 256-bit AES encryption, ECDSA signing algorithms, Elliptic asymmetric public key algorithms, and a Deterministic Random Number Generator (DRNG). Runtime APIs are provided in the ROM for customer application code to use the cryptographic hardware. PUF ID generation resources and algorithms are included, as well as lockable OTP storage for keys and IDs. Fused Life Cycle security gives access to these resources only when appropriate for development, test, or production phases.

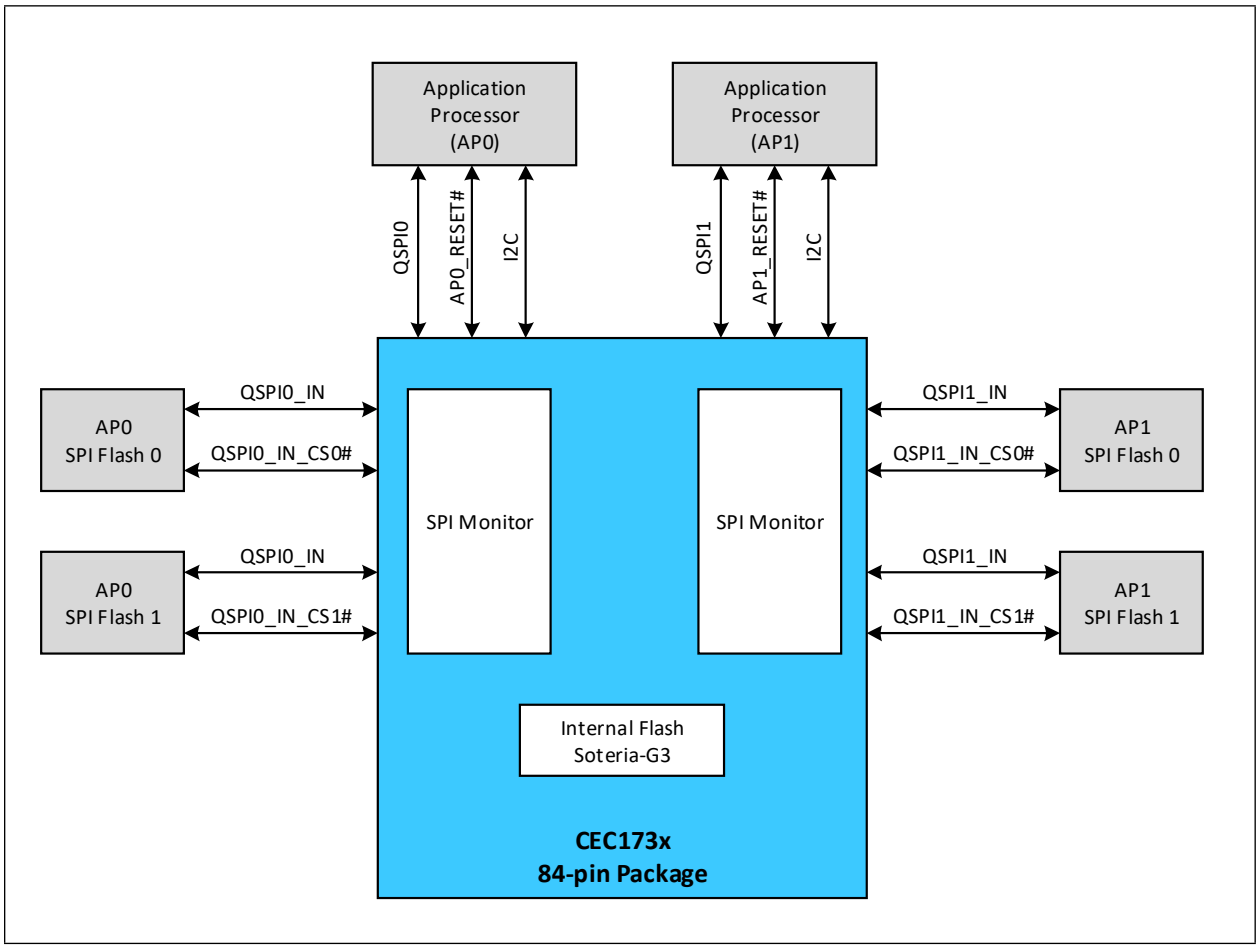
The CEC173x TrustFLEX is designed to be incorporated into low power designs. During normal operation, the hardware always operates in the lowest power state for a given configuration. The chip power management logic offers two low power states: light sleep and heavy sleep. When the chip is sleeping, it has many wake events that can be configured to return the device to normal operation, for example any GPIO pin.

The CEC173x TrustFLEX offers a software development system interface that includes a serial debug port (UART) and a 2-pin Serial Wire Debug (SWD) interface. Also included is a full 4-wire JTAG interface for Boundary Scan testing (disabled for production).

2.0 SYSTEM CONFIGURATION

Figure 2-1 shows an example usage of the CEC173x-TFLX device. In this configuration, there are two Application Processors, each on their own QSPI port connected to two SPI flash devices. Each Application Processor has their own I^2C port to request status information from the CEC173x-TFLX.

FIGURE 2-1: SYSTEM BLOCK DIAGRAM



3.0 SOTERIA-G3 OVERVIEW

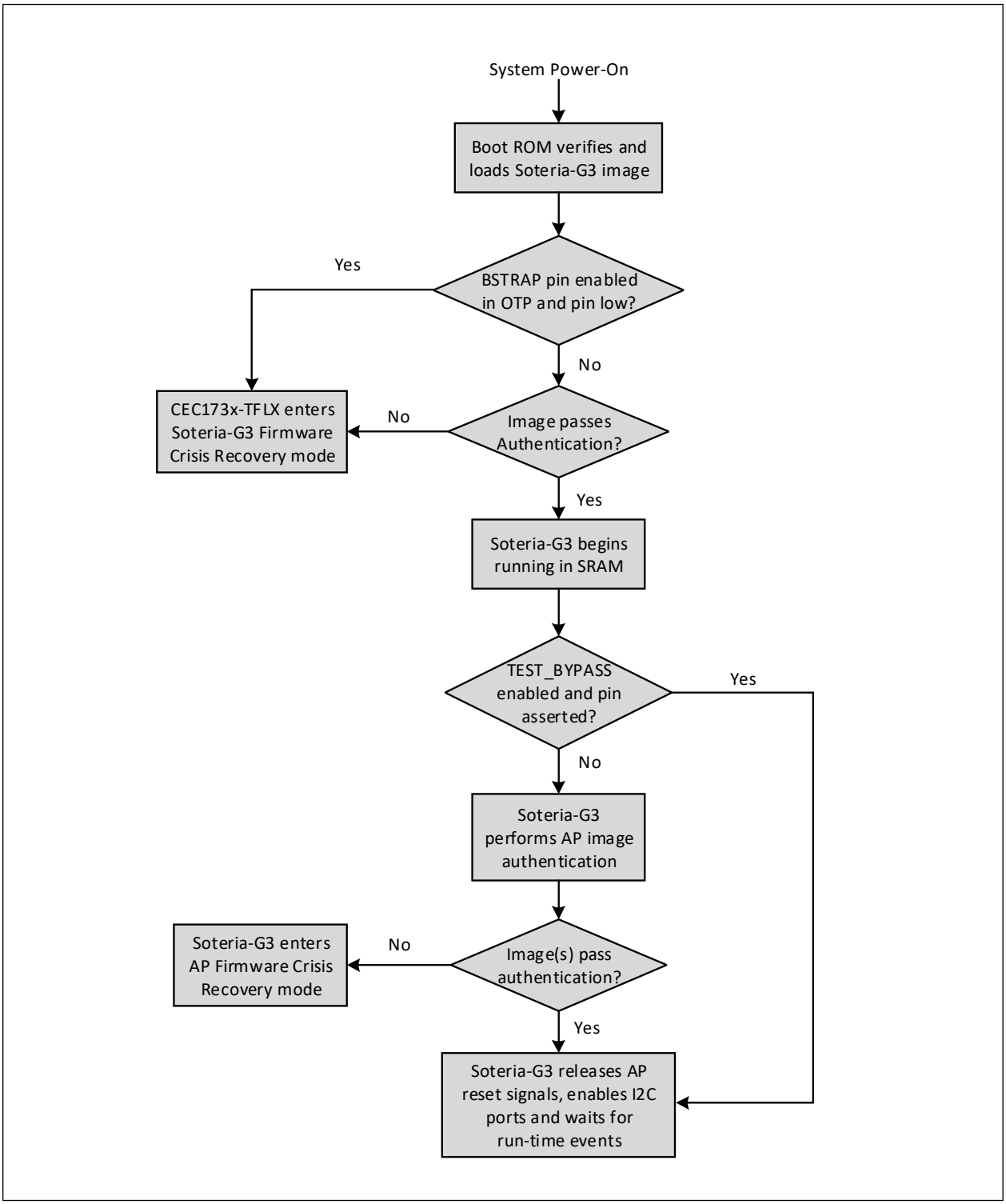
The Soteria-G3 Firmware is an all-in-one solution developed by Microchip to exercise all the available security features of the CEC173x-TFLX. Soteria-G3 provides an enhanced feature set, including the Secure Boot of Application Firmware images, Secure Firmware Updates, Platform Attestation compliant with SPDM, and much more.

At power-up, the CEC173x-TFLX will hold the Application Processor(s) (AP) in reset and isolate the external flash components. The authenticated Soteria-G3 Firmware running in the CEC173x-TFLX will use the AP Configuration (AP_CFG) Table, which provides all configuration information about the system, to perform any hardware initialization and firmware set-up required before Secure Boot. The Soteria-G3 Firmware will also read the Hash Table(s), which contain the hash values of all AP firmware images present in the external SPI flash components, as well as which images require authentication. Soteria-G3 then performs the Secure Boot process to authenticate the AP firmware images, if they are configured to be, before releasing the AP reset signal. Figure 3-1 below shows a flowchart outlining the boot process.

After AP reset is released, Soteria-G3 will reauthenticate the AP firmware images as they are being read by the AP. This image authentication status is made available through the AP I^2C port for additional validation. At this point, Soteria-G3 is ready to handle requests made for any of the additional software features available that have been enabled and configured by the customer.

Soteria-G3 code is cleared by MISRA, checked by Coverity® and CERT® C code analysis and certified by third-party penetration tests.

FIGURE 3-1: BOOT PROCESS



4.0 PIN CONFIGURATION

4.1 Packaging Options

The CEC173x-TFLX Family comes in both 64-pin and 84-pin packaging options. The 84-pin package (2ZW) has two QSPI ports with SPI monitoring to support up to two Application Processors with two SPI flash components each. The 64-pin package (2HW) supports only one QSPI port for one Application processor with up to two SPI flash components.

4.2 Pin List

The table below gives the pinout of the available CEC173x-TFLX packages.

FIGURE 4-1: CEC1736 PINOUT

CEC173x-S0-I/2ZW-TFLX	CEC1736-S0-I/2HW-TFLX	CEC173x Signal Name
A4	E2	GPIO000/SPI0_KILL/SPI0_RESET#
J2	F9	GPIO002/QSPI0_CS1#/SPIMON_QSPI0_CS1#
C6	J2	GPIO003/I2C00_SDA(FATAL_ERROR#)
C1	G2	GPIO004/I2C00_SCL
D6	J3	GPIO012(EXTRST#)
F2	K7	GPIO013/SP1_ALT_IO3(WDTRST2)
B3	F2	GPIO015/ICT10[BSTRAP]
K4	D10	GPIO016/QSPI0_IO3/QSPI0_IO3_CLAMP
K1	G9	GPIO020/QSPI0_IN_CS0#
J3	D9	GPIO021/QSPI0_IN_CS1#
J7	A7	GPIO022/QSPI0_IN_IO1
E9	A8	GPIO023/QSPI0_IN_IO0
F7		GPIO024/SPI1PER_CS#
A10	A4	GPIO026/SP0_AP_INTR[I2C_ADDR0]
D5	K2	GPIO027/TFDP_CLK_ALT(SPI0_BLEED#)
B6	D1	GPIO030/I2C10_SDA
A3	G1	GPIO031/SP1_ALT_IO0
K10		GPIO032/QSPI1_IN_IO1
B4		GPIO033(SPI1_BLEED#)
A5	F1	GPIO034/SP1_AP_INTR[I2C_ADDR1]
H9		GPIO045/QSPI1_IN_CS1#
A7	C2	GPIO046/SP1_ALT_CS#(WDTRST1)
C2	K3	GPIO047/SP1_ALT_IO1
B2	H2	GPIO050/ICT0(ASYNC_RST_DET#)
E1	J5	GPIO053/PWM0(EC_STS#)
K2	E9	GPIO055/QSPI0_CS0#/SPIMON_QSPI0_CS0#(QSPI0_PWRGD)
K7	B9	GPIO056/QSPI0_CLK/QSPI0_CLK_CLAMP
D4	J4	GPIO057/VCC_PWRGD
A1	H1	GPIO063/SP1_ALT_CLK(EXTRST_IN#)
D10		GPIO070/QSPI1_IN_IO0
J9		GPIO071/QSPI1_IN_CS0#

FIGURE 4-1: CEC1736 PINOUT

CEC173x-S0-I/2ZW-TFLX	CEC1736-S0-I/2HW-TFLX	CEC173x Signal Name
E4	K5	GPIO104/UART0_TX/TFDP_CLK
E2	J6	GPIO105/UART0_RX/TFDP_DATA
E3	K6	GPIO106/AP0_RESET#(AP0_RESET#)
A6	E1	GPIO107/I2C10_SCL/ALT_VIOL_0
F4	K8	GPIO112/ALT_VIOL_1/TFDP_DATA_ALT
A2		GPIO113/ICT9(AP1_RESET_IN#)
H10		GPIO120/QSPI1_CS1#/SPIMON_QSPI1_CS1#
F9		GPIO121/QSPI1_IO0/QSPI1_IO0_CLAMP
K9		GPIO122/QSPI1_IO1/QSPI1_IO1_CLAMP
F10		GPIO123/QSPI1_IO2/QSPI1_IO2_CLAMP
J8		GPIO124/QSPI1_CS0#/SPIMON_QSPI1_CS0#(QSPI1_PWRGD)
J10		GPIO125/QSPI1_CLK/QSPI1_CLK_CLAMP
G10		GPIO126/QSPI1_IO3/QSPI1_IO3_CLAMP
F3	J7	GPIO127/SP1_ALT_IO2(WDTRST1)
B1	J1	GPIO130/32KHZ_IN
D2		GPIO131/AP1_RESET# (AP1_RESET#)
C9	D2	GPIO132/I2C06_SDA
B7	C1	GPIO140/I2C06_SCL
A9	A2	GPIO143/I2C04_SDA
B9	A3	GPIO144/I2C04_SCL(REMOTE_ACCESS)
B10	B4	GPIO145/I2C09_SDA/JTAG_TDI
C10	B2	GPIO146/I2C09_SCL/ITM/JTAG_TDO(SWV)
B8	B1	GPIO147/I2C15_SDA/JTAG_CLK (SWDCLK)
A8	B3	GPIO150/I2C15_SCL/JTAG_TMS (SWDIO)
H2	J10	GPIO156/LED0
H1	G10	GPIO157/LED1
B5		GPIO163/SPI1_KILL/SPI1_RESET#
E10		GPIO165/QSPI1_IN_IO2
G5	J8	GPIO170[JTAG_STRAP]
G9		GPIO171/QSPI1_IN_IO3
K8		GPIO200/QSPI1_IN_CLK
G2	J9	GPIO201/32KHZ_OUT[CR_FLASH]
K5	C9	GPIO202/QSPI0_IN_IO2
K3	E10	GPIO203/QSPI0_IN_IO3
K6	B10	GPIO204/QSPI0_IN_CLK
F8	A6	GPIO223/QSPI0_IO0/QSPI0_IO0_CLAMP
J6	A9	GPIO224/QSPI0_IO1/QSPI0_IO1_CLAMP
J4	B7	GPIO227/QSPI0_IO2/QSPI0_IO2_CLAMP
J5	C10	GPIO250/SPI0PER_CS#
E8	B6	GPIO253/TST_CLK_OUT

FIGURE 4-1: CEC1736 PINOUT

CEC173x-S0-I/2ZW-TFLX	CEC1736-S0-I/2HW-TFLX	CEC173x Signal Name
G1	H9	JTAG_RST#
G4	H10	nRESET_IN
G6	G4	VSS_ANALOG
F1	K9	VTR_PLL
D9	D7	VSS
D7	G7	VTR_REG
H5	B8	VTR1
C5	D4	VTR_ANALOG
D1	K4	VR_CAP
E7	A5	VSS
H6		VTR2
J1	F10	VSS
G7	B5	VSS

4.3 Package Information

4.3.1 64 PIN VFBGA PACKAGE

FIGURE 4-2: 2HW Package Dimensions, Sheet 1

64-Ball Very Thin Fine-Pitch Ball Grid Array (2HW) - 5.5x5.5x0.92 mm Body [VFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

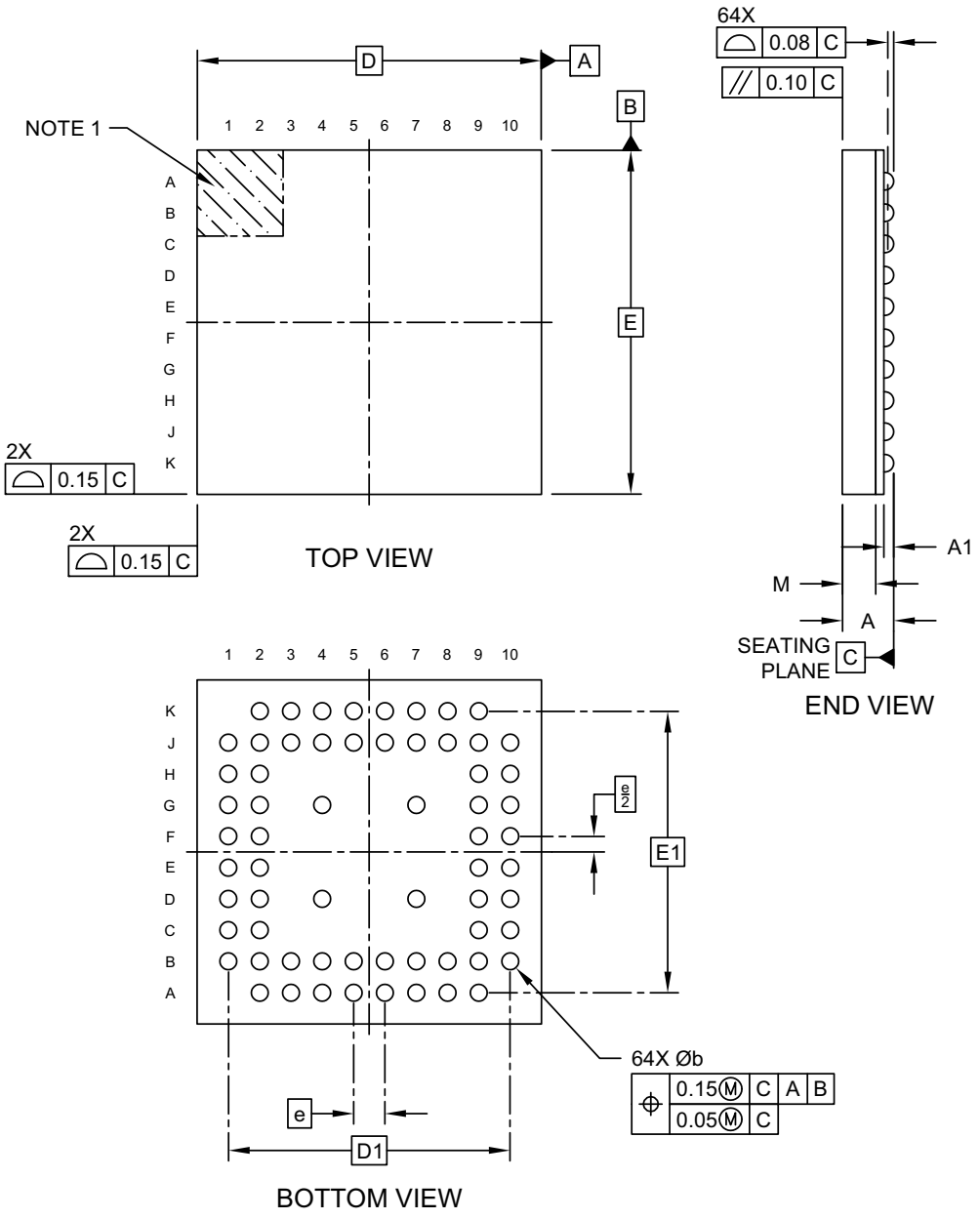
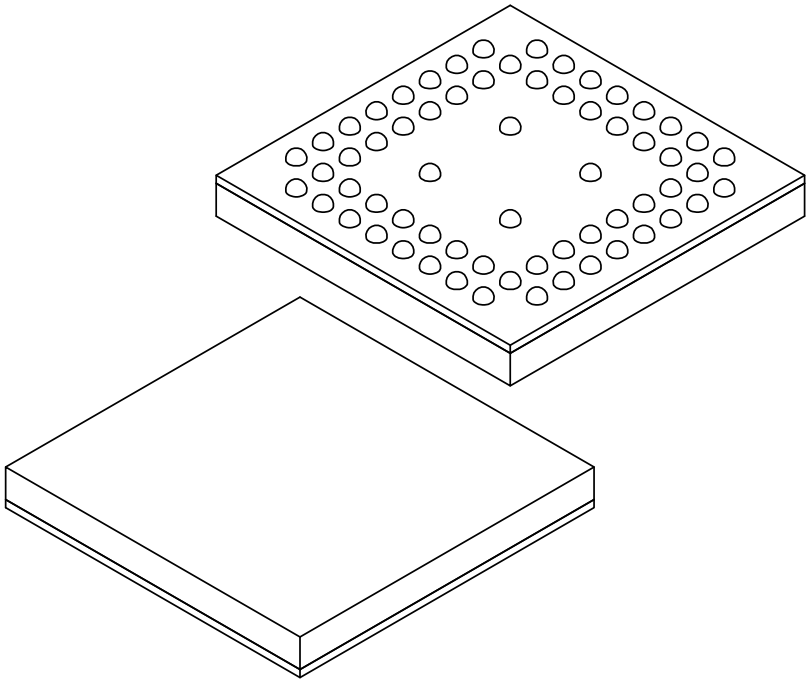


FIGURE 4-3: 2HW Package Dimensions, Sheet 2

64-Ball Very Thin Fine-Pitch Ball Grid Array (2HW) - 5.5x5.5x0.92 mm Body [VFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	0.92
Ball Height	A1	0.12	0.16	–
Mold Thickness	M	0.48	0.53	0.58
Overall Length	D		5.50 BSC	
Ball Array Length	D1		4.50 BSC	
Overall Width	E		5.50 BSC	
Ball Array Width	E1		4.50 BSC	
Ball Diameter	b	0.23	0.28	0.33

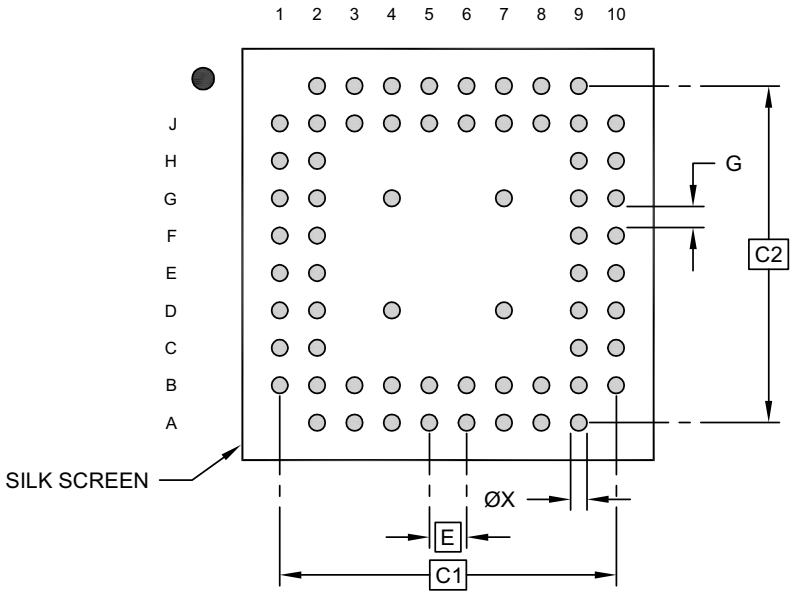
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

FIGURE 4-4: 2HW Package Dimensions, Sheet 3

64-Ball Very Thin Fine-Pitch Ball Grid Array (2HW) - 5.5x5.5x0.92 mm Body [VFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1	4.50 BSC		
Contact Pad Spacing	C2	4.50 BSC		
Contact Pad Diameter (X64)	X1			X.XX
Contact Pad to Contact Pad (Xnn)	G	0.28		

Notes:

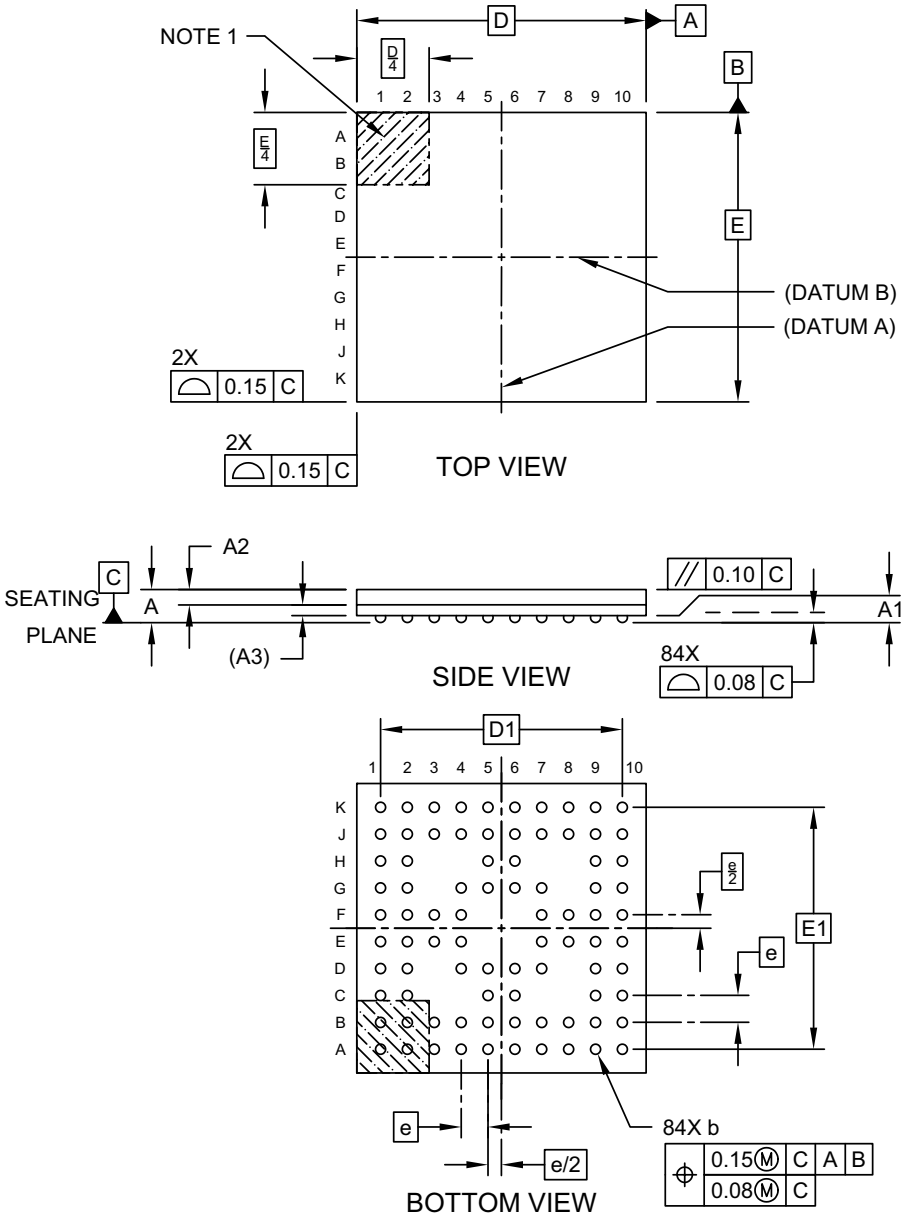
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

4.3.2 84 PIN WFBGA PACKAGE

FIGURE 4-5: 2ZW Package Dimensions, Sheet 1

84-Ball Very, Very Thin fine Pitch Ball Grid Array (2ZW) - 7x7x0.8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

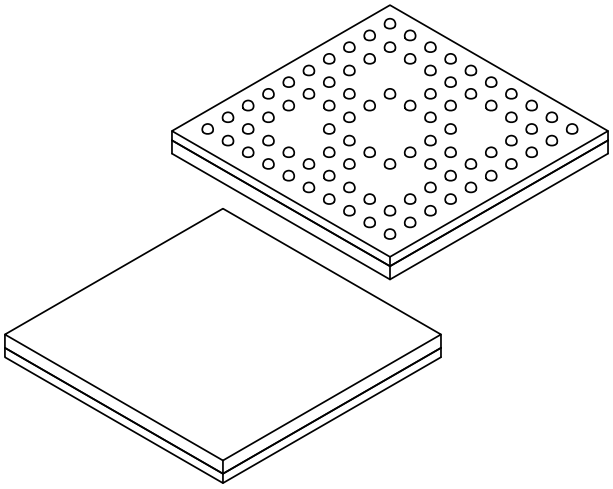


Microchip Technology Drawing C04-390-2ZW Rev C Sheet 1 of 2

FIGURE 4-6: 2ZW Package Dimensions, Sheet 2

84-Ball Very, Very Thin fine Pitch Ball Grid Array (2ZW) - 7x7x0.8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		84	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	0.80
Standoff	A1	0.12	0.17	-
Mold Cap Thickness	A2	0.35	0.40	0.45
Substrate Thickness	A3		0.13 REF	
Overall Length	D		7.00 BSC	
Overall Termnal Spacing	D1		5.85 BSC	
Overall Width	E		7.00 BSC	
Overall Termnal Spacing	E1		5.85 BSC	
Ball Diameter	b	0.20	0.25	0.30

Notes:

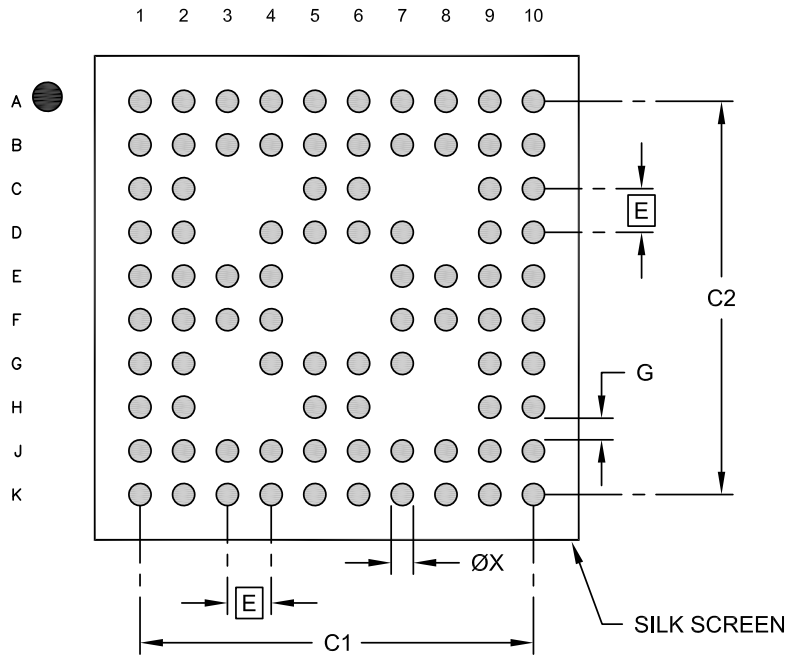
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-390-2ZW Rev C Sheet 2 of 2

FIGURE 4-7: 2ZW Package Dimensions, Sheet 3

84-Ball Very, Very Thin Fine Pitch Ball Grid Array (2ZW) - 7x7x0.8 mm Body [WFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Overall Contact Pad Spacing	C1		5.85	
Overall Contact Pad Spacing	C2		5.85	
Contact Pad Width (X84)	X1			0.33
Contact Pad to Contact Pad	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2390-2WX Rev C

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

Revision	Section/Figure/Entry	Description
DS00005379A (03-25-24)	Initial Release	

PRODUCT IDENTIFICATION SYSTEM

Not all of the possible combinations of Device, Temperature Range and Package may be offered for sale. To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.[1]	-	XX	-	X/XXX[2]	-	[X]	-	[X][3]
Device		Version/ Revision		Temp Range/ Package		Device Option		Tape and Reel Option

Device:	CEC1736		Cryptographic Embedded Controller, Temperature and Voltage Countermeasures
Version/ Revision:	S#		S = Soteria Version # = Revision Version Number
Temperature Range	I/	=	-40°C to +85°C (Industrial)
Package:	2ZW		84 ball WFBGA, 7x7x0.8 mm body, 0.65 pitch, 4MB Flash, Dual SPI Monitor
	2HW		64 ball VFBGA, 5.5x5.5x0.92 mm body, 0.5 pitch, 2MB Flash, Single SPI Monitor
Device Option	TFLX	=	TrustFLEX Device
Tape and Reel Option:	Blank	=	Tray packaging
	TR	=	Tape and Reel[3]

Example:

a) CEC1736-S0-I/2ZW-TFLX = CEC1736, TrustFLEX Variant, Revision Version 0, 84 ball WFBGA, 7mm x 7mm body, 4MB Flash, Dual SPI Monitor, Industrial grade, Tray packaging

b) CEC1736-S0-I/2HW-TFLX-TR = CEC1736, TrustFLEX Variant, Revision Version 0, 64 ball VFBGA, 5.5mm x 5.5mm body, 2MB Flash, Single SPI Monitor, Industrial grade, Tape and Reel packaging

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.microchip.com/pagehandler/en-us/aboutus/ehs.html

3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option

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