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INTEGRATION

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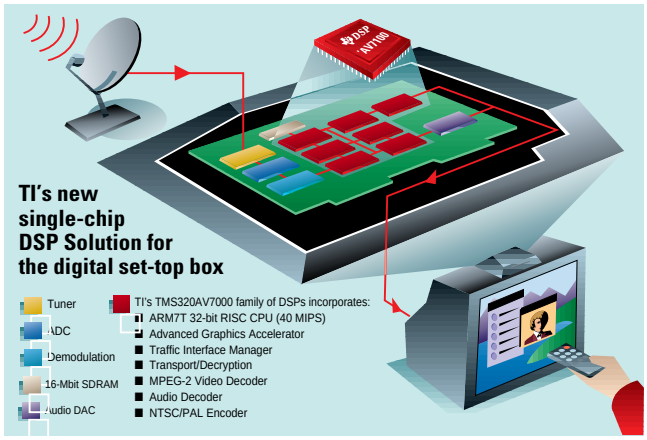
design to win

SET-TOP BOX

New DSPs invigorate digital set-top boxes



The first single-chip DSP solution for decrypting, decoding and displaying digital video on a TV is now available from TI.

Specifically designed for digital set-top applications, the new TMS320AV7000 series of digital signal processors (DSPs) is compliant with the Digital Video Broadcast (DVB) and Digital Satellite System (DSS) standards used worldwide.

The 'AV7000 series obsoletes an entire generation of set-top architectures that separate the CPU and transport functions from the audio/video decompression and graphics overlay functions. The 'AV7000 architecture integrates these functions along with the NTSC/PAL video encoder, reducing three components to one. Further reduction in system cost results from consolidating the

See SET-TOP BOX on page 2

WIRELESS

TI delivers customizable digital wireless baseband platform

A new single-chip DSP Solution from TI integrates all the digital baseband functions necessary for the design of digital wireless telephones using any transmission standard.

The industry's first standard-independent digital baseband platform helps manufacturers reduce the size, weight, component costs and power consumption in digital cellular phones, digital cordless phones, two-way voice/data pagers and other types of wireless communications systems.

At the heart of the digital baseband platform is a high-performance, low-power processing engine — the TMS320C54x digital signal processor (DSP) core. Optimized for high-speed number-crunching functions such as voice coding, channel coding, error correction, equalization, demodulation and encryption, the 'C54x DSP core is approximately 30 percent more MIPS-efficient in wireless applications than comparable DSPs.

Also integrated in the platform is a 16-bit/32-bit 'c470 microcontroller unit (MCU) based on the ARM7TDMI (ARM Thumb™) core licensed from Advanced RISC Machines Ltd. The MCU handles general system control, such as mobility management and the man-machine interface. Since the DSP and MCU cores and the

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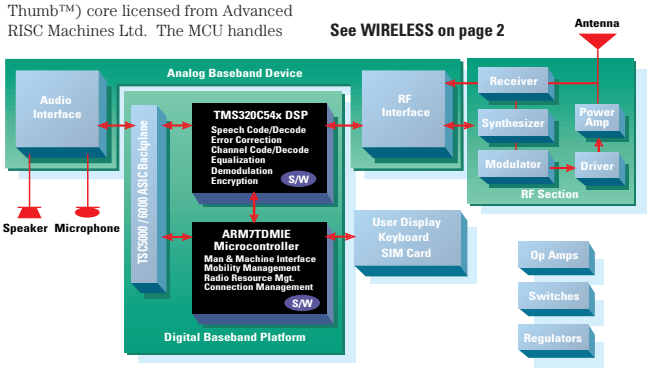


TI's Digital Baseband Platform integrates all the digital baseband functions needed for the design of digital cellular and PCS telephones using any transmission standard.

MODEMS

New x2 modem chip sets speed OEM production

By year end, OEMs can get modem reference designs from Texas Instruments that enable systems to deliver twice the performance of today's fastest modems over conventional telephone lines.

Based on existing modem chip-set architectures, the chip sets are compliant with 56 kilobits-per-second (kbps) x2™ technology from U.S. Robotics Corp. (USR, Chicago, Illinois) and implemented with a software-programmable digital signal

See MODEMS on page 2

What is x2?

x2 is a higher speed data communications technology, developed by U.S. Robotics, to take advantage of the changes in today's network systems. It is an asymmetrical technology that allows 56-kbps data rates downstream and 28.8-kbps upstream data rates when connecting to central site hubs. Several applications — Internet access, Bulletin Board Services and corporate networks — can take advantage of this higher data rate technology.

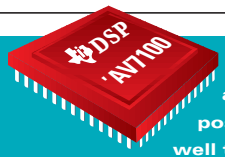
TECHNOLOGY

SET-TOP BOX

Continued from page 1

multiple banks of memory required in the system into a single 16-Mbit synchronous DRAM.

The first member of the 'AV7000 series, the TMS320AV7100, integrates a 16-bit/32-bit ARM7T™ RISC microprocessor core licensed from Advanced RISC Machines Ltd. The 'AV7100 also integrates an advanced graphics accelerator, transport demultiplexer, conditional access and decryption modules, MPEG-2 video decoder, MPEG audio decoder, and NTSC/PAL video encoder with Macrovision™ copy protection. The 'AV7100's transport demultiplexer, conditional access and decryption are optimized for DSS system requirements.Another device, the TMS320AV7110, integrates the same functions but has a DVB-optimized transport demultiplexer and can support externally the multiple conditional access and decryption implementations used by different service providers.



The processor performance and graphics capabilities position the 'AV7000 architecture well to support future data services currently evolving over the broadband networks.

The architecture of the new processors includes features targeted at three distinct needs of DVB- and DSS-compliant digital set-top boxes: greater integration and memory consolidation for reduced system cost; higher CPU performance for more sophisticated applications software; and advanced graphics acceleration for a more intuitive user interface.

In addition to integrating three chips into one, the 'AV7000 architecture reduces costs through its Traffic Interface Manager (TIM). This consolidates the memory requirements of each on-chip function into a single bank of memory, providing the flexibility to dynamically allocate system resources. The ARM7T processor's dual instruction set allows on-chip firmware to execute at the full 32-bit performance, while off-chip software can take advantage of the 16-bit mode to greatly reduce the application software memory size and still achieve excellent performance. The 40-MIPS ARM processor not only supports the TIM and transport demultiplex functions, but also provides over half of its processing power for application software. Combined with on-chip graphics acceleration, the processing performance enables instantaneous response to users.

The graphics accelerator supports 256 colors, transparency, blending, sizing and positioning in multiple graphics windows that can be displayed and overlapped simultaneously, providing a larger viewing area for the video and more intuitive access to information on-screen. The processor performance and graphics capabilities position the 'AV7000 architecture well to support future data services currently evolving over the broadband networks.

TMS320AV7100 sampling is planned for December and TMS320AV7110 sampling for February. Production for both devices is planned for 2Q97, with pricing below $45 in quantities of 100K. ▼

WIRELESS

Continued from page 1

logic gates can be programmed to support any digital wireless standard, the TI digital baseband platform can be used to design systems in any region of the world. In order to accelerate customer time to market, TI offers a library of various DSP and MCU software modules, as well as ASIC hardware peripherals that can be licensed to customers to support various worldwide standards.

The DSP and MCU cores are both supported by extensive suites of TI development tools and are accessible for in-circuit emulation through an IEEE 1149.1/JTAG test port. Special on-chip logic allows simultaneous co-emulation of both cores with a single set of emulation hardware. This unique, proprietary co-emulation capability can save designers months of development time, speeding time to market.

The announcement of the TI digital baseband platform follows an extensive period of customer testing. Nokia, Europe's largest manufacturer of cellular phones, for example, has been receiving samples of a device based on this platform. "This integrated digital baseband platform will support increased functionality and performance while reducing system cost and power dissipation of our digital cellular programs," said Yrjo Neuvo, senior vice president, R&D, Nokia.

"This integrated digital baseband platform will support increased functionality and performance while reducing system cost and power dissipation of our digital cellular programs."

— Yrjo Neuvo, senior vice president, R&D, Nokia

The TI digital baseband platform is supported by TI's 0.25-micron TSC5000 CMOS standard cell ASIC library, enabling designers to integrate additional logic functions, RAM, ROM and mixed-signal functions such as phase-locked loops and analog-to-digital converters. At this node, the platform allows sub-2V operation, thereby reducing power consumption by 50 percent as compared with a conventional 2.7-V system. The TI digital baseband platform will be ported in 1997 to the 0.18-micron TSC6000 library based on TI's 125-million transistor TImeline™ technology, enabling 1-V functionality and reducing power consumption by another 75 percent.

"With this proven platform, designers have the capability to integrate and customize the entire digital baseband section of their systems on a single chip while also addressing any transmission standard," said Gilles Delfassy, TI Semiconductor Group vice president and worldwide general manager for the Wireless Communications Business Unit. "This capability not only gives designers flexibility, it also helps them speed up the design cycle."

The digital baseband platform is ready for current engagements for use in high-volume digital wireless communications designs. ▼

Two processors, one platform

The two core processors in the TI digital baseband platform have been selected for their suitability in wireless communications systems, which demand high performance, low cost and low power dissipation.

In the TSC5000 ASIC backplane, the TMS320C54x DSP core operates at 100 MIPS at 2.5 V with accompanying power dissipation of 0.59 mA/MHz. Features include:

- ▼ Viterbi accelerator
- ▼ Four internal buses and dual address generators to enable multiple operand operations
- ▼ 40-bit adder and two 40-bit accumulators to facilitate parallelism
- ▼ Single-cycle normalization and exponential encoding
- ▼ Single-cycle instructions including 17-bit unsigned multiplication
- ▼ Power-down modes

The 'C470 RISC MCU core can operate in two modes with 75 MHz of performance: 32-bit instructions for faster execution and 16-bit instructions for high code density. The 16-bit capability saves a remarkable amount of memory space, helping reduce system costs. The microcontroller is also extremely thrifty in terms of cost and power dissipation. The 0.25-micron version, compatible with the TSC5000 ASIC library and operating at 2.5 V, requires only 2.0 square millimeters on the die (about one-third the size of similar cores) and dissipates only 0.36 mA/MHz. ▼

MODEMS

Continued from page 1

processor from Texas Instruments.

The new 56 kbps x2 technology uses traditional telephone lines to allow Internet and on-line services users to download text, image and video data at twice the speed of today's 28.8 kbps modems. Advanced, DSP-based handshaking techniques allow TI-based modems to connect over a highly unpredictable assortment of line conditions throughout the worldwide telecom infrastructure.

"Any kind of 56 kbps connectivity requires identical protocols both in the user's modem and at the Internet service providers [ISPs] where reprogrammable USR modems are already widely installed," said Mike Hames, vice president Semiconductor Group and worldwide manager of DSP at TI. "This alone will make x2 an automatic de facto standard for Internet access equipment."

"Based on TI's leading DSP technology, we will be able to upgrade many of our existing modem architectures without any hardware changes."

— Casey Cowell, chairman, CEO, and president of U.S. Robotics

Any modem product designed using the TI chip sets, including PC modem cards, external PC modems, and Internet access equipment, will be backwardly compatible to current standards including: V.34 (33.6Kbps) data, V.17 (14.4Kps) fax and all of the fall backs.

TI's operating-system-independent and Windows™-based modem chip sets are built around one of the company's TMS320 DSP cores. This allows designers to upgrade end equipment with new technology through software reprogrammability both at the host level and at the DSP level, protecting end users against hardware obsolescence.

"USR has long depended on programmable TI DSP solutions to give our modems significant performance advantages, and we are pleased to be working with Texas Instruments to bring this new technology to market," Casey Cowell, chairman, CEO, and president of U.S. Robotics. "Based on TI's leading DSP technology, we will be able to upgrade many of our existing modem architectures without any hardware changes. This flexibility is key in bringing x2 to market quickly."

TI's OS-independent and Windows-based modem chip sets are now available directly from Texas Instruments. Pricing is $75 for 10K unit quantities. ▼

INTEGRATION

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Texas Instruments

MESSAGING

Chip set supports FLEX messaging

A new two-chip DSP Solution from TI will enable OEMs to rapidly develop messaging devices that conform to the emerging FLEX™ messaging protocol. Targeted at alphanumeric pagers and other embedded wireless messaging applications, the new TMS320FLEX1 chip set simplifies implementation of the FLEX protocol in these systems by interfacing directly with most receivers and off-the-shelf microcontrollers. As a result, pager OEMs can develop FLEX-compliant products quickly from existing designs with minimal hardware changes.

The chip set consists of the TLV5591 FLEX Protocol Decoder, a signal processor that decodes the FLEX messaging protocol transmission, and the TLV5590 A/D Converter, which converts the analog signal from the receiver into a digital signal for decoding by the TLV5591. A complement to the chip set is FLEXstack™ software, designed to facilitate application development. Running on the system processor, FLEXstack handles interchip communications and interprets host commands for the TLV5591, simplifing development of OEM software. FLEXstack is available on Motorola's World Wide Web site at http://www.mot.com/FLEXstack.

The new product supports the 1600-, 3200- and 6400-bit-per-second (bps) transmission speeds of the FLEX standard, allowing OEMs to easily migrate their end equipments up the performance path as higher transmission rates are supported by flex service providers. The substantial increase in the number of subscribers per channel can help

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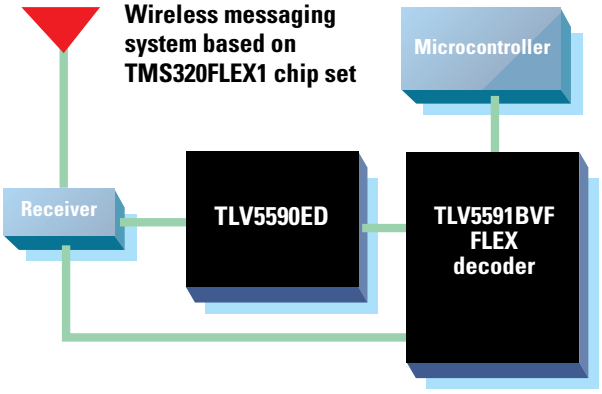

TI's new TMS320FLEX1 Chip Set interfaces directly with most receivers and off-the-shelf microcontrollers for fast redesigns with minimal hardware changes.

NETWORKING

TImeline Technology defines the next level of high-speed networking

Every day, more than 300 million pages of text are sent over the Internet.

Yet to many, those pages creep along at a snail's pace, getting bumped and stalled by network collisions and collapses. Demand for bandwidth — and speed — far exceeds supply. TI's 0.18-micron TImeline Technology™, combined with the company's architectural approach to networking, will enable OEM partners to leap one to two generations ahead with high-speed internetworking products. These products will provide unlimited bandwidth at a much lower price point than today's products.

With 0.18-micron TImeline Technology, the advanced traffic management capabilities and sophisticated network management functions required to support thousands-of-gigabits-per-second throughput will be implemented in silicon. These functions have historically been implemented in software. But the performance and sophistication of products that leverage the 0.18-micron technology will require a hardware solution made possible by TImeline integration. TI will use ASIC products, standard products and reusable engineering in the form of system-level core functions to provide these solutions.

The TI 0.18-micron technology delivers other significant benefits for networking OEMs. Higher integration reduces the number of components per system, thereby reducing system costs. Power dissipation is significantly reduced. By eliminating heat sinks and other costly thermal management add-ons in the system, TI reduced overall cost.

The benefits of the 0.18-micron technology also extend to managers and users of enterprise networks, addressing new network technologies and giving networking devices better feature/value sets, lower cost per port, smaller footprint and simpler management.

Initial design engagements employing the TImeline Technology are currently in progress. Samples are scheduled to be available in 1997 with full production targeted for 1998. ▼

CONNECTIVITY

New link-layer added to 1394 product family

TI announced a new general purpose IEEE 1394 link-layer chip optimized for use in consumer electronics and computer peripherals. The chip is the industry's first available general purpose 1394 link-layer device with a 8/16-bit interface. The part, designated TSB12LV31 and called GPLynx, will make it easier and less expensive to integrate the IEEE 1394-1995 high performance serial bus.

GPLynx has a programmable 8- or 16-bit microcontroller interface, making it easily compatible with a wide selection of standard microcontrollers and DSPs used in consumer electronic equipment and computer peripherals. It also incorporates a separate 8-bit, high speed isochronous data interface with an integrated data mover for high volume isochronous data.

At nearly half the price of TI's preceding generation of link-layer silicon, designing with GPLynx is also very affordable.

Applications include digital consumer electronics such as cameras, televisions, CD players, tape decks and computer peripherals such as printers, scanners, CD ROM drives, hard disk drives, and digital video disk (DVD) drives.

GPLynx works with currently available 1394 physical-layer chips to provide speeds of 100 or 200 megabits per second (Mbps).

The TSB12LV31 GPLynx comes in a 100-pin plastic quad flat pack (PQFP) carrier. It is available now from TI and its authorized distributors. Suggested resale pricing in quantities of 1,000 is $9.72. A new GPLynx 1394 Design Kit, the sixth from TI, will soon be available.

For more information , please visit our Web site at www.ti.com/sc/1394. ▼

PCI bus-to-cardbus controller complies with PC97 guidelines

As the industry's first PC 97-compliant CardBus™ controller, Texas Instruments PCI1131 simplifies hardware and software development efforts for designers of PCI bus-based notebook and desktop PCs and offers throughput bandwidth significantly greater than that of other CardBus controllers on the market today.

Because TI's new PCI1131 controller meets Microsoft's PC 97 design guidelines for next generation PCs, designers can be assured that the PCI bus-to-CardBus interface will function efficiently with future releases of Microsoft's Windows operating system and Windows-based application programs.

The PCI1131 supports two 32-bit CardBus credit-card-size add-in modules that give the PC access to peripheral devices, such as modems, video programming, printers, external video monitors and local area networks. The device will also support 16-bit PCMCIA (Personal Computer Memory Card Industry Association) or PC Card add-in modules.

The PCI1131 is TI's second generation CardBus controller. It follows the PCI1130, the industry's first CardBus controller introduced over a year ago. An easy migration path is provided to the PCI1131 from TI's previous generation controllers.

All devices in TI's family of CardBus controllers are packaged in 208-pin Thin Quad Flat Pack (TQFP) carriers and they are all pin-for-pin compatible with each other.

The PCI1131 is available now from TI and its authorized distributors. ▼

TI announces family of Universal Serial Bus interface chips

Texas Instruments disclosed the development of the industry's most comprehensive family of Universal Serial Bus (USB) interface chips. Samples of a seven-port USB hub device, the TUSB2070, and a four-port hub device, the TUSB2040, are available now. Other initial devices in the product family include a Hub with I2C Interface to enable USB Monitor Control and a Peripheral Interface Controller for use with popular microcontrollers and DSPs. Lastly, a Peripheral Interface Macrocell will soon be available such that USB functionality can be easily and rapidly included in Application Specific Integrated Circuit (ASIC) and customizable Digital Signal Processor (cDSP) designs.

USB is an emerging industry standard designed for PC peripherals with low-to-medium data transfer requirements. Its 12 Mbps transmission capability provides both asychronous and isochronous (real-time) data transmission over a 4-wire cable. This more than meets the needs of most existing peripherals including keyboards, mice, modems, printers, and digital stereo audio. Additionally, USB supports hot plug-and-play so that adding a peripheral becomes as simple as plugging it into a USB connector.

Suggested resale pricing of the TUSB2070 in quantities of 1,000 is $5.00. Suggested resale pricing of the TUSB2040 in quantities of 1,000 is $4.10. ▼

PRODUCT UPDATE

First self-calibrating precision dual op amp

The TLC4502 is the first product in a new generation of self-calibrating, precision operational amplifiers. During the calibration procedure, the operational amplifier is removed from the signal path and both inputs are tied to GND. The offset cancellation uses a current-mode digital-to-analog converter (DAC), whose full-scale current allows for an adjustment of approximately ±5mV to the input offset voltage.

Key features

- Self-calibration of input offset voltage to 50mV max (TLC4502A)
- Rail-to-rail output voltage swing
- Offers significant advantages over chopper-stabilized and precision bipolar solutions
- High output drive capability (±50 mA)
- 300ms typical calibration time
- 5V single supply operation
- Standard dual op amp pinout; 8-pin SOIC
- Specified over commercial (0°C to 70°C) and industrial(-40°C to 85°C) temperature ranges

Suggested price per device in quantities of 1,000:

TLC4502CDR	$1.18	TLC4502IDR	$1.30
TLC4502ACDR	$1.28	TLC4502AIDR	$1.41

ARM7T, ARMThumb and Macrovision are trademarks of Advanced RISC Machines, Ltd. Windows is a registered trademark of Microsoft Corporation. x2 is a trademark of U.S. Robotics Corporation. CardBus is a trademark of PCMCIA.

16-bit analog interface to DSP Solutions

The TLC320AD56 is a 16-bit analog interface circuit (AIC) that is a versatile analog front end for modem and business audio applications. It provides high resolution low-speed signal conversion from analog-to-digital and from digital-to-analog using an oversampling sigma delta technique.

The TLC320AD56 optimizes TI's world leadership in digital signal processing solutions. The newest member of the family has a glueless interface, via serial port, to the TMS320 family of digital signal processors (DSPs) reducing overall system cost and board space.

Key features

- 16 bit sigma delta AIC
- Power dissipation: 100 mW (typ), Power down 2.5mW (typ)
- Programmable serial port interface
- Internal 64X oversampling
- THD of 103 dB on ADC, and 96 dB on DAC

The TLC320AD56 is available in the 28-pin PLCC (plastic lead chip carrier) package and the 48-pin TQFP (quad flat pack) package, and will be available in the 28-pin SOIC package. Suggested retail price in 1K quantities is $4.15.

FLEX

Continued from page 7

lower infrastructure costs.

The chip set helps systems provide up to five times the battery life of older paging protocol standards, enabling miniaturization and improvements in design because of the smaller batteries required. With support for alphanumeric messages and group pages, the chip set also helps improve signal integrity for greater error protection and positive message termination.

Samples of both the TLV5590 A/D Converter and TLV5591 FLEX Protocol Decoder are available now, with volume production planned for January. Purchase of the TMS320FLEX1 chip set satisfies all FLEX protocol licensing requirements for OEMs. No separate licensing agreement with Motorola is necessary.

The TMS320FLEX1 chip set is $9.80 in 1K quantities. ▼

For TI SC literature, see http://www.ti.com/sc/9612

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To order the following TI SC product literature, simply call 1-800-477-8924 ext. 9612. Please allow 2-3 weeks for delivery.

1 ❑ WCBU Digital Baseband Technical Brief (SPRY006)
2 ❑ Wireless Brochure (SPRB115A)
3 ❑ TI/USR X2 Product Brief (SPRT134)
4 ❑ DCP AV7000 Product Bulletin (SCST004)
5 ❑ MSP 1394 GPLynx Data Sheet (SLLS255)
6 ❑ EVM Kits Flier (SLLZ001)
7 ❑ EVM Kits Product Bulletin (SLLM001B)
8 ❑ MSP USB Data Sheet (SLLS239)
9 ❑ MSP USB Product Bulletin (SLLT137)
10 ❑ MSP Op Amp Product Update (SLOS161)
11 ❑ MSP AD56 Data Manual (SLAS101A)
12 ❑ PCIbus 1131 Product Bulletin (SCPV002)
13 ❑ TMS320FLEX1 Design Manual (SLWS048)
14 ❑ TMS320FLEX1 Wireless Brochure (SPRB115A)
15 ❑ TMS320 DSP Brochure (SPRB118)

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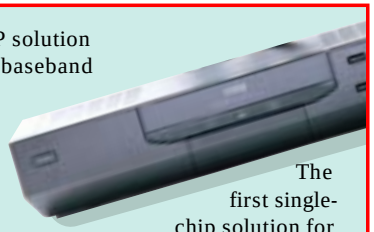
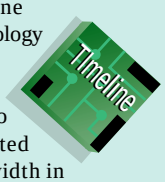


The first single-chip solution for the digital set-top box reduces three components to one. **Page 1**

design to win

TI's 0.18-micron TImeline Technology opens the door to unlimited bandwidth in networking. **Page 7**



Chip set makes developing messaging devices that conform to the FLEX protocol easier for OEMs. **Page 7**

TI and U.S. Robotics announce protocol for super-fast 56.6-Kbits/s modems. **Page 1**

DSP Solutions from TMS320 Third Parties help our customers launch tomorrow's end products today. **Special Pullout**