

# **TPT1043Q**

# Automotive Low-Power Fault Protected High-Speed CAN FD

## Transceiver with Sleep Mode

## Features

- Meet the ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5 Physical Layer Standards
- Supports CAN FD and Data Rating up to 5 Mbps
- Short Propagation Delay Times and Fast Loop Times
- 5-V Power Supply, I/O Voltage Range Supports 2.8-V to 5.5-V MCU Interface
- Standby Mode and Extra Low Current Sleep Mode with Local and Remote Bus Wake-Up Capability and INH Output
- Ideal Passive Behavior to CAN Bus when Unpowered
- Common-Mode Input Voltage: ±30 V
- Protection Feature:
  - IEC 61000-4-2 ESD Protection up to ±12 kV
  - Bus Fault Protection: ±70 V
  - VCC Undervoltage Protection
  - TXD Dominant Time-Out Function and Bus-Dominant Time-Out Function
  - Thermal Shutdown Protection
- Available in SOP14 Package and Leadless DFN4.5X3-14L Package
- AEC-Q100 Qualified for Automotive Application, Grade 1

## Applications

- All Devices Supporting Highly Loaded CAN Networks
- Automotive and Transportation
  - Body Electronics / Lighting
  - Power Train / Chassis
  - Infotainment / Cluster
  - ADAS / Safety

### Description

The TPT1043 is a CAN transceiver that meets the ISO11898 high-speed CAN (Controller Area Network) physical layer standard. The device is designed to be used in CAN FD networks up to 5 Mbps, with enhanced timing margins and higher data rates in long and highly loaded networks. As designed, the device features a -30-V to +30-V common-mode range, CAN-Bus fault protection from -70 V to +70 V, over-voltage protection, and overtemperature shutdown. TPT1043 has an I/O power supply for interface I/O to connect to microcontrollers with supply voltages from 2.8 V to 5.5 V. The device comes with a standby mode, which can be waked up from the CAN BUS. The ultra-low power management controls the Electronic Control Unit (ECU) in standby and sleep modes. The device enables the power supply by the INH interface through the local and remote wake-up with wakeup source recognition, and it includes many protection features to enhance the device and network robustness.

The TPT1043 is available in SOP14 and DFN4.5X3.0-14L packages, and is characterized from -40°C to +125°C.

## **Typical Application Circuit**





## **Table of Contents**

Features	1
Applications	1
Description	
Typical Application Circuit	1
Product Family Table	3
Revision History	
Pin Configuration and Functions	4
Specifications	5
Absolute Maximum Ratings	
ESD (Electrostatic Discharge Protection)	6
Recommended Operating Conditions	6
Thermal Information	6
Electrical Characteristics	7
AC Timing Requirements	11
Parameter Measurement Information	13
Test Circuit	13
Parameter Diagram	14
Detailed Description	15
Overview	15
Functional Block Diagram	15
Feature Description	16
Device Operating Modes	16
Internal Flags	18
Remote Wake-up	19
Device Local Faults	19
Application and Implementation	21
Application Information	21
Typical Application	21
Tape and Reel Information	22
Package Outline Dimensions	23
SOP14	23
DFN4.5X3-14	24
Order Information	25
IMPORTANT NOTICE AND DISCLAIMER	26



# **Product Family Table**

Order Number	VCC (V)	VIO (V)	BUS Protection (V)	Package
TPT1043Q-SO2R-S	5.0	2.8 to 5.5	±70	SOP14
TPT1043Q-DFKR-S	5.0	2.8 to 5.5	±70	DFN4.5X3-14L

## **Revision History**

Date	Revision	Notes	
2021-11-02	Rev.Pre.0	Initial Version	
2022-11-25	Rev.A.0	Released Version	
2023-10-25	Rev.A.1	Typo correction	
2024-08-27	Rev.A.2	<ul> <li>Updated R<sub>IN</sub> and R<sub>ID</sub> test CAN bus range</li> <li>V<sub>OD_REC</sub>, V<sub>_REC</sub> typo correction</li> <li>Updated V<sub>O_DOM</sub> test condition</li> </ul>	



## **Pin Configuration and Functions**





#### Table 1. Pin Functions: TPT1043

Р	Pin I/O		Description		
No.	Name	1/0	Description		
1	TXD	Input	CAN transmit data input (low for dominant and high for recessive bus states)		
2	GND	GND	Ground connection		
3	VCC	Power	5-V CAN bus supply voltage		
4	RXD	Output	CAN receive data output (low for dominant and high for recessive bus states), tri-state		
5	VIO	Power	I/O supply voltage		
6	EN	Input	Enable input for mode control, integrated pull-down		
7	INH	Output	Can be used to control system voltage regulators		
8	ERR_N	Output	Fault output, inverted logic		
9	WAKE	Input	Wake input terminal, high voltage input		
10	VBAT	Power	Reverse-blocked battery supply input		
11	NC	-	No connection (not internally connected)		
12	CANL	Bus I/O	Low-level CAN bus input/output line		
13	CANH	Bus I/O	High-level CAN bus input/output line		
14	STB_N	Input	Standby input for mode control, integrated pull-down		
	Exposed pad	GND	Thermal pad of DFN package, required to connect the exposed pad to GND		



## **Specifications**

### **Absolute Maximum Ratings**

	Parameter	Min	Max	Unit
V <sub>BAT</sub>	Battery Supply Voltage Range	-0.3	60	V
V <sub>cc</sub>	5-V Bus Supply Voltage Range	-0.3	7	V
V <sub>IO</sub>	I/O Level-Shifting Voltage Range	-0.3	7	V
V <sub>BUS</sub>	CAN Bus I/O Voltage Range (CANH, CANL)	-70	70	V
V <sub>BUS_DIFF</sub>	Differential Voltage of CAN Bus, CANH - CANL	-70	70	V
VLOGIC	Logic Input and Output Terminal Voltage Range (TXD, RXD, STB_N, ERR_N, EN)		7	V
Vwake	WAKE Input Pin Voltage Range	-0.3	60 and V <sub>WAKE</sub> ≤ V <sub>BAT</sub> + 0.3 V	V
VINH	INH Output Pin Voltage Range	-0.3	60 and V <sub>INH</sub> ≤ V <sub>BAT</sub> + 0.3 V	V
Io_logic	RXD and ERR_N Output Current	-8	8	mA
I <sub>O_INH_</sub>	INH Output Current	-4	4	mA
TJ	Maximum Junction Temperature	-40	150	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C
T <sub>OTP</sub>	Shutdown Junction Temperature	-	170	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.



### ESD (Electrostatic Discharge Protection)

	Parameter Condition		Minimum Level	Unit
	IEC Contact Discharge	IEC-61000-4-2, Bus Pin	±12	kV
IEC	IEC Air-Gap Discharge	IEC-61000-4-2, Bus Pin	±15	kV
НВМ	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001, All Pin	±8	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, All Pin	±1.5	kV
		LU, per JESD78, All Pin, 25°C		mA
LU	Latch Up	LU, per JESD78, All Pin, 125°C	±100	mA
		Pulse 1	-100	V
.,	ISO7637-2 transients per IEC	Pulse 2a	75	V
Vtran	62228-3, CANH, CANL, WAKE, VBAT	Pulse 3a	-150	V
	VDAI	Pulse 3b	100	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### **Recommended Operating Conditions**

	Description	Min	Max	Unit
VBAT	Battery Supply Voltage Range	4.5	40	V
VIO	Input/output Voltage TXD, RXD, STB_N, ERR_N, EN	2.8	5.5	V
Vcc	Power Supply	4.5	5.5	V
IOH_RXD	RXD Terminal High-Level Output Current	-4	-	mA
I <sub>OL_RXD</sub>	RXD Terminal Low-Level Output Current	-	4	mA
I <sub>O_INH</sub>	INH Output Current	-	1	mA
TA	Operating Ambient Temperature	-40	125	°C

### **Thermal Information**

Package Type	θյΑ	θις	Unit
SOP14	65.5	33.7	°C/W
DFN4.5x3-14	35.8	31.6	°C/W



### **Electrical Characteristics**

All test conditions:  $V_{CC}$  = 4.5 V to 5.5 V,  $V_{IO}$  = 2.8 V to 5.5 V,  $V_{BAT}$  = 4.5 V to 40 V,  $R_L$  = 60  $\Omega$ , T = -40°C to 125°C, unless otherwise noted.

	Parameter	Test Conditions	Min	Тур	Max	Unit
Pin VCC (F	Power Supply)	· · · · · ·			1	
Vcc	Supply Voltage		4.5	-	5.5	V
UV <sub>VCC_R</sub>	Undervoltage Recovery on V <sub>CC</sub> for Protected Mode	V <sub>CC</sub> Rising	-	3.6	4.4	V
UV <sub>VCC_F</sub>	Undervoltage Detection on $V_{CC}$ for Protected Mode	V <sub>cc</sub> Falling	3	3.4	-	V
VHYS_UVVCC	Hysteresis Voltage on $U_{VVCC}$ <sup>(1)</sup>		-	200	-	mV
		Normal mode (dominant), $V_{TXD}$ = 0 V, $R_L$ = 50 $\Omega$ , $C_L$ = open	-	45	65	mA
		Normal mode (recessive), $V_{TXD}$ = $V_{IO}$ , $R_L$ = 50 $\Omega$ , $C_L$ = open	-	1.2	3	mA
lcc	Supply Current	Standby/Sleep mode $V_{BAT}$ > $V_{CC}$ , $R_L$ = 50 $\Omega$ , $C_L$ = open	-	2	3	μA
		Dominant with bus fault, short circuit on bus line, $V_{TXD} = 0 V$ , $-3V < (V_{CANH} = V_{CANL}) < +18V$ , $R_L = Open, C_L = open$	-	63	110	mA
Pin VIO (I/0	O Supply)					
V <sub>IO</sub>	Supply Voltage on V <sub>IO</sub> Pin		2.8	-	5.5	V
UV <sub>VIO_R</sub>	Undervoltage Recovery on V <sub>IO</sub> for Protected Mode	V <sub>IO</sub> Rising	-	1.8	2.5	V
UV <sub>VIO_F</sub>	Undervoltage Detection on V <sub>IO</sub> for Protected Mode	V <sub>IO</sub> Falling	0.8	1.7	-	V
V <sub>HYS_UVVIO</sub>	Hysteresis Voltage on U <sub>VVIO</sub> for Protected Mode <sup>(1)</sup>		-	100	-	mV
		Normal mode, V <sub>TXD</sub> = 0 V, Dominant	-	150	500	μA
l <sub>IO</sub>	Supply Current from VIO	Normal/Silent mode, V <sub>TXD</sub> = V <sub>IO</sub> , Recessive	-	2	4	μA
		Standby/Sleep mode	-	2	4	μA
Pin VBAT (	Supply from battery)					
UV <sub>BAT_R</sub>	Undervoltage Recovery on VBAT for Protected Mode	VBAT rising	-	3.5	4.3	V
UV <sub>BAT_F</sub>	Undervoltage Detection on VBAT for Protected Mode	VBAT falling	3	3.3	-	V
V <sub>HYS_UVBAT</sub>	Hysteresis Voltage on U <sub>VBAT</sub> <sup>(1)</sup>		-	200	-	mV



	Parameter	Test Conditions	Min	Тур	Max	Unit
		Normal/Silent mode	-	34	70	μA
		Standby mode, V <sub>CC</sub> > 4.5 V,		45	20	
I <sub>BAT</sub>	Battery Supply Current	V <sub>INH</sub> = V <sub>WAKE</sub> = V <sub>BAT</sub>	-	15	30	μA
		Sleep mode, $V_{INH} = V_{CC} = V_{IO}$ = 0 V, $V_{WAKE} = V_{BAT}$	-	15	30	μA
Pin TXD (	CAN transmit data input)					
V <sub>IH_TXD</sub>	High-Level Input Voltage	$3 \text{ V} \leq \text{V}_{\text{IO}} \leq 5.5 \text{ V}$	0.7 x V <sub>IO</sub>	-	V <sub>IO</sub> + 0.3	V
VIL_TXD	Low-Level Input Voltage	$3 \text{ V} \leq \text{V}_{10} \leq 5.5 \text{ V}$	-0.3	-	0.3 x V <sub>IO</sub>	V
I <sub>IH_TXD</sub>	High-Level Input Current	V <sub>TXD</sub> = V <sub>IO</sub>	-5	0	5	μA
$I_{\text{IL}_{\text{TXD}}}$	Low-Level Input Current	V <sub>TXD</sub> = 0 V, Normal mode	-300	-63	-30	μA
Cı	Input Capacitance (1)		-	5	10	pF
Pin RXD (	CAN Receive data output)					
I <sub>OH_RXD</sub>	High-Level Output Current	$V_{RXD} = V_{IO} - 0.4 \text{ V}, V_{IO} = V_{CC}$	-12	-6	-1	mA
Iol_rxd	Low-Level Output Current	$V_{RXD} = 0.4 V, V_{TXD} = V_{IO},$ Bus dominant	2	6	14	mA
I <sub>LKG_OFF</sub>	Unpowered Leakage Current <sup>(1)</sup>	$V_{RXD} = 5.5 V, V_{CC} = 0 V,$ $V_{IO} = 0 V$	-1	0	1	μA
Pin STB_I	N, EN (Standby and enable control	input)		1	· · ·	
VIH	High-Level Input Voltage		0.7 x V <sub>IO</sub>	-	V <sub>IO</sub> + 0.3	V
VIL	Low-Level Input Voltage		-0.3	-	0.3 x V <sub>IO</sub>	V
I <sub>IH</sub>	High-Level Input Current	$V_{STB_N}$ or $V_{EN} \ge 0.7 V$	1	4	10	μA
IIL	Low-Level Input Current	$V_{STB_N} = V_{EN} = 0 V$	-1	-	1	μA
Pin ERR_	N (Error and power-on indication o	utput)				
I <sub>IH_ERR_N</sub>	High-Level Input Current	$V_{ERR_N} = V_{IO} - 0.4 V, V_{IO} = V_{CC}$	-50	-20	-4	μA
I <sub>IL_ERR_N</sub>	Low-Level Input Current	V <sub>ERR_N</sub> = 0.4 V	0.1	0.5	2	mA
Pin WAKE	(Local wake-up pin)					
IIH_WAKE	High-Level Input Current	V <sub>WAKE</sub> = V <sub>BAT</sub> – 1.9 V	-10	-5	-1	μA
IIL_WKAE	Low-Level Input Current	V <sub>WAKE</sub> = V <sub>BAT</sub> – 3.1 V	1	5	10	μA
VTH_WAKE	Threshold Voltage	V <sub>WAKE</sub> = 0 V	V <sub>BAT</sub> – 3	V <sub>BAT</sub>	V <sub>BAT</sub> – 2	V
Pin INH (I	nhibit high voltage output)					
V <sub>O_INH</sub>	High-Level Output Voltage	I <sub>INH</sub> = −180 μA	V <sub>BAT</sub> – 0.8	-	VBAT	V
I <sub>L_INH</sub>	Leakage Current	Sleep mode	-2	-	2	μA
	, CANL (CAN Bus lines)					



	Parameter		Test Conditions	Min	Тур	Max	Unit
		CANH	CAN active mode, $4.75V \le V_{CC}$	2.75	3.5	4.5	V
Vo_dom	Dominant Bus Output Voltage	CANL	$\leq 5.25 \text{ V}, \text{ V}_{\text{TXD}} = 0 \text{ V}, 50 \Omega \leq \text{R}_{\text{L}}$ $\leq 65 \Omega, \text{ C}_{\text{L}} = \text{open},$ $t < t_{\text{to(dom)TXD}}$	0.5	1.5	2.25	V
V <sub>SYM_DC</sub>	DC Output Symmetry (domina recessive) (V <sub>CC</sub> – V <sub>O(CANH)</sub> – V <sub>O(CANL)</sub> ) <sup>(1)</sup>	int or	$V_{CC}$ = 5 V, R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open,	-0.6	-	0.6	V
V <sub>SYM</sub>	Transient Symmetry (dominan recessive) (V <sub>O(CANH)</sub> + V <sub>O(CANL)</sub> ) / V <sub>CC</sub> <sup>(1)</sup>	it or	4.75V $\leq$ V <sub>CC</sub> $\leq$ 5.25 V, R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open, C <sub>SPLIT</sub> = 4.7 nF, T <sub>XD</sub> = 250 kHz, 1 MHz, 2.5MHz	0.9	1	1.1	V/V
			CAN active mode, t < $t_{to(dom)TXD}, 4.75V \le V_{CC} \le 5.25$ V, V <sub>TXD</sub> = 0 V, 45 $\Omega \le R_L < 50$ $\Omega$ , C <sub>L</sub> = open	1.5	-	3	V
			CAN active mode, t < $t_{to(dom)TXD}$ , 4.75V $\leq$ V <sub>CC</sub> $\leq$ 5.25 V, V <sub>TXD</sub> = 0 V, 50 $\Omega \leq$ R <sub>L</sub> $\leq$ 65 $\Omega$ , C <sub>L</sub> = open	1.5	-	3	V
Vod_dom	Differential Output Voltage (do	ominant)	CAN active mode, t < $t_{to(dom)TXD}$ , 4.75V $\leq$ V <sub>CC</sub> $\leq$ 5.25 V, V <sub>TXD</sub> = 0 V, 65 $\Omega \leq$ R <sub>L</sub> $\leq$ 70 $\Omega$ , C <sub>L</sub> = open	1.5	-	3.3	V
			CAN active mode, t < $t_{to(dom)TXD}$ , 4.75V $\leq V_{CC} \leq 5.25$ V, $V_{TXD}$ = 0 V, R <sub>L</sub> = 2240 $\Omega$ , C <sub>L</sub> = open	1.5	-	5.0	V
V <sub>OD_REC</sub>	Differential Output Voltage (ree	cessive)	Normal/Silent mode, V <sub>TXD</sub> = V <sub>IO</sub> , no load	-50	-	50	mV
			Standby/sleep mode <sup>(1)</sup>	-0.2	-	0.2	V
V <sub>O_REC</sub>	Recessive Output Voltage		Normal/Silent mode, V <sub>TXD</sub> = V <sub>IO</sub> , no load	2	0.5 x V <sub>CC</sub>	3	V
-			Standby/sleep mode <sup>(1)</sup>	-0.1	-	0.1	V
	Dominant Short-Circuit	CANH	$V_{STB} = 0 V, -15 V \le V_{CANH} \le 18$ V, CANL = open, $V_{TXD} = 0 V$	-115	-	-	mA
Io_sc_dom	Output Current	CANL	$V_{STB} = 0 V, -15 V \le V_{CANL} \le 18$ V CANH = open, $V_{TXD} = 0 V$	-	-	115	mA
Io_sc_rec	Recessive Short-Circuit Output Current		$-27 \text{ V} \le \text{V}_{CANH}/\text{ V}_{CANL} \le 32 \text{ V},$ V <sub>TXD</sub> = V <sub>CC</sub> , normal modes	-5	-	5	mA
V <sub>CM</sub>	Common Mode Range			-30	-	30	V
VTH_RX_DIF	Differential Receiver Threshole	d Voltage	Normal or Silent mode $-30 V \le V_{CANH} / V_{CANL} \le 30 V$	0.5	0.7	0.9	V



	Parameter	Test Conditions	Min	Тур	Max	Unit
		Standby or Sleep mode,	0.4	0.7	4.45	N
		$-30 \text{ V} \le \text{V}_{\text{CANH}}/\text{ V}_{\text{CANL}} \le 30 \text{ V}$	0.4	0.7	1.15	V
		Normal or Silent mode	0		0.5	
		$-30 \text{ V} \le \text{V}_{\text{CANH}}/\text{ V}_{\text{CANL}} \le 30 \text{ V}$	-3	-	0.5	V
V <sub>REC_RX</sub>	Receiver Recessive Voltage	Standby or Sleep mode,	-3		0.4	N
		$-30 \text{ V} \leq \text{V}_{\text{CANH}}/\text{ V}_{\text{CANL}} \leq 30 \text{ V}$		-	0.4	V
		Normal or Silent mode	0.0		0	N
		$-30 \text{ V} \le \text{V}_{\text{CANH}}/\text{ V}_{\text{CANL}} \le 30 \text{ V}$	0.9	-	8	V
V <sub>DOM_RX</sub>	Receiver Dominant Voltage	Standby or Sleep mode,	1.15			
		$-30 \text{ V} \le \text{V}_{\text{CANH}}/\text{ V}_{\text{CANL}} \le 30 \text{ V}$		-	8	V
	Differential Receiver Hysteresis Voltage <sup>(1)</sup>	Normal or Silent mode,	-	400		
V <sub>HYS_RX_DIF</sub>		$-30 \text{ V} \leq \text{V}_{\text{CANH}}/\text{ V}_{\text{CANL}} \leq 30 \text{ V}$		130	-	mV
		$V_{CC} = 0 V$ , $V_{CANH} = V_{CANL} = 5 V$	-5	-	5	μA
		$V_{BAT} = 0 V$ , $V_{CANH} = V_{CANL} = 5 V$	-5	-	5	μA
ΙL	Leakage Current	$V_{BAT} = V_{CC} = V_{CC} = 0 \text{ V or } V_{BAT}$ $= V_{CC} = V_{CC} \text{ shorted to ground}$ $via 47 \text{ k}\Omega; V_{CANH} = 5 \text{ V}, V_{CANL} = 5 \text{ V}$	-5	-	5	μA
R <sub>IN</sub>	Input Resistance (CANH or CANL)	$V_{TXD} = V_{CC} = V_{IO} = 5 \text{ V},  V_{STB} = 0  \text{V}, -2  \text{V} \leq  \text{V}_{CANH}/ \text{V}_{CANL} \leq +7  \text{V}$	10	23	30	kΩ
R <sub>IN_M</sub>	Input Resistance Matching: [1 – RIN(CANH) / RIN(CANL)] × 100%	$V_{TXD} = V_{CC} = V_{IO} = 5 \text{ V}, \text{ V}_{STB} = 0 \text{ V},$ $V_{CANH} = V_{CANL} = 5 \text{ V},$	-2	-	2	%
R <sub>ID</sub>	Differential Input Resistance	$V_{TXD} = V_{CC} = V_{IO} = 5 \text{ V}, V_{STB} = 0 \text{ V}, -2 \text{ V} \leq V_{CANH}/V_{CANL} \leq +7 \text{ V}$	30	47	60	kΩ
Cı	Input Capacitance to Ground (CANH or CANL) <sup>(1)</sup>		-	-	20	pF
CID	Differential Input Capacitance <sup>(1)</sup>		-	-	10	pF

(1) The data is based on bench tests and design simulation.



### **AC Timing Requirements**

All test conditions:  $V_{CC}$  = 4.5 V to 5.5 V,  $V_{IO}$  = 2.8 V to 5.5 V,  $V_{BAT}$  = 4.5 V to 40 V,  $R_L$  = 60  $\Omega$ ,  $T_A$  = -40°C to 125°C, unless otherwise noted.

Parameter		Test Conditions	Min	Тур	Max	Unit
Transceive	er Switching Characteristics					
t <sub>pLD</sub>	Propagation delay time, low TXD to driver dominant (recessive to dominant) <sup>(1)</sup>		-	60	100	ns
t <sub>pHR</sub>	Propagation delay time, high TXD to driver recessive (dominant to recessive) <sup>(1)</sup>	Normal mode or Silent mode, $R_L$ = 60 $\Omega$ , $C_L$ = 100 pF	-	60	100	ns
t <sub>sK_P</sub>	Pulse Skew ( $ t_{pHR} - t_{pLD} $ ) <sup>(1)</sup>		-	10	35	ns
t <sub>R</sub>	Differential Output Signal Rise Time <sup>(1)</sup>		-	45	-	ns
t <sub>F</sub>	Differential Output Signal Fall Time <sup>(1)</sup>		-	45	-	ns
t <sub>pRH</sub>	Propagation Delay Time, Bus Recessive Input to RXD High Output (Dominant to Recessive) (1)		-	90	-	ns
t <sub>pDL</sub>	Propagation Delay Time, Bus Dominant Input to RXD Low Output (Recessive to Dominant) (1)	V <sub>STB</sub> = 0 V, C <sub>L(RXD)</sub> = 15 pF	-	90	-	ns
t <sub>R_R</sub>	RXD Output Signal Rise Time <sup>(1)</sup>		-	20	-	ns
t <sub>R_F</sub>	RXD Output Signal Fall Time <sup>(1)</sup>		-	20	-	ns
t <sub>PROP_TXDL-</sub> RXDL	Total loop delay, driver input (TXD) low to receiver output (RXD) low, recessive to dominant (1)	Normal mode, $R_L = 60 \Omega$ , $C_L =$	-	110	220	ns
tprop_txdh- rxdh)	Total loop delay, driver input (TXD) high to receiver output (RXD) high, dominant to recessive <sup>(1)</sup>	100 pF, C <sub>L(RXD)</sub> = 15 pF,	-	140	220	ns
FD Timing	Parameters					
t <sub>BIT_BUS</sub>	Bit time on CAN bus output pins with $t_{BIT_TXD}$ = 500 ns <sup>(1)</sup>	V <sub>STB</sub> = Vcc, R <sub>L</sub> = 60 Ω,	435	-	530	ns
	Bit time on CAN bus output pins with $t_{BIT_TXD}$ = 200 ns <sup>(1)</sup>	$C_{L} = 100 \text{ pF},$ $C_{L(RXD)} = 15 \text{ pF},$	155	-	210	ns
tbit_rxd	Bit time on RXD output pins with $t_{BIT_TXD} = 500 \text{ ns}$	$\Delta t_{\text{REC}} = t_{\text{BIT}_{\text{RXD}}} - t_{\text{BIT}_{\text{BUS}}}$	400	-	550	ns



	Parameter	Test Conditions	Min	Тур	Max	Unit
	Bit time on RXD output pins with $t_{BIT_TXD}$ = 200 ns		120	-	220	ns
A.+	Receiver timing symmetry with $t_{BIT_TXD}$ = 500 ns <sup>(1)</sup>		-65	-	40	ns
∆t <sub>REC</sub>	Receiver timing symmetry with $t_{BIT_TXD}$ = 200 ns <sup>(1)</sup>		-45	-	15	ns
Device Tin	ning Parameters					
t <sub>UV_DET</sub>	Undervoltage detection time <sup>(1)</sup>		100	-	350	ms
tuv_rec	Undervoltage recovery time <sup>(1)</sup>		1	-	5	ms
t <sub>тхд_дто</sub>	TXD dominant time-out time	Normal mode, $R_L = 60 \Omega$ , $C_L = open$ , $V_{TXD} = 0 V$	0.4	-	4	ms
t <sub>BUS_DTO</sub>	Bus dominant time-out time	Normal mode	0.4	-	4	ms
td_MODE	Issue goes to sleep command to enter sleep mode delay time		20	35	50	μs
tbus_wake_ Dom	Bus dominant wake-up time	Standby or Sleep mode	0.5	1.5	3	μs
t <sub>BUS_WAKE_</sub> REC	Bus recessive wake-up time	Standby or Sleep mode	0.5	1.5	3	μs
t <sub>WAKE_TO</sub>	Bus wake-up time-out time		0.5	-	2	ms
t <sub>WAKE</sub>	Wake up time		20	-	55	μs

(1) The test data is based on bench tests and design simulation.



### **Parameter Measurement Information**

**Test Circuit** 



Figure 1. CAN Transceiver Timing Parameter Test Circuit



Figure 2. CAN Transceiver Driver Symmetry Test Circuit



### Parameter Diagram



Figure 3. CAN Transceiver Timing Diagram



Figure 4. CAN FD Timing Parameter Diagram



Figure 5. Wake-up Timing Diagram



## **Detailed Description**

### Overview

The TPT1043 is a CAN transceiver that meets the ISO11898 High-Speed CAN (Controller Area Network) physical layer standard. The device is designed to be used in CAN FD networks up to 5 Mbps, with enhanced timing margins and higher data rates in long and highly loaded networks. As designed, the device features a -30-V to +30-V common-mode range, CAN-Bus fault protection ranges from -70 V to +70 V, with over-voltage protection and over-temperature shutdown. TPT1043 has an I/O power supply for interface I/O to connect to microcontrollers with supply voltages ranging from 2.8 V to 5.5 V. The device, coming with the standby mode, is also waked up from the CAN BUS. The ultra-low power management controls the Electronic Control Unit (ECU) in standby and sleep modes. The power supply is enabled by the INH interface through the local and remote waking up with wake-up source recognition. The device includes many protection features to enhance device and network robustness.

### Functional Block Diagram



Figure 6. Functional Block Diagram



# **TPT1043Q**

# Automotive Low-Power Fault Protected High-Speed CAN FD Transceiver with Sleep Mode

### **Feature Description**

Device Mede	Inputs	Outputs		Driven BUS State
Device Mode	TXD	CANH	CANL	Driven BUS State
Nomed	L	Н	L	Dominant
Normal	H or Open	Z	Z	Bus biased to VCC/2
Silent	X	Z	Z	Bus biased to VCC/2
Standby	X	Z	Z	Bus biased to GND
Go-to-Sleep	Х	Z	Z	Bus biased to GND
Sleep	Х	Z	Z	Bus biased to GND

#### Table 3. Receiver Function Table

Device Mode	CAN Differential Inputs VID = VCANH – VCANL	BUS State	RXD Terminal
	$V_{ID} \ge V_{IT+(MAX)}$	Dominant	L
Nermel en Ctendhu	$V_{IT-(MIN)} < V_{ID} < V_{IT+(MAX)}$	Indeterminate	Indeterminate
Normal or Standby	$V_{ID} \le V_{IT-(MIN)}$	Recessive	Н
	Open (V <sub>ID</sub> ≈ 0 V)	Open	Н

### **Device Operating Modes**

The device has 5 operating modes: normal mode, standby mode, silent mode, go-to-sleep mode, and sleep mode. Operating mode selection is made via the EN pin and the STB\_N pin and wake-up events when the power supply is valid.





Figure 7. Mode Transition State Diagram

### Normal Mode

This is the normal operating mode of the device. In the normal mode, the CAN driver and receiver block are fully operational. The transceiver will transmit and receive data via the bus lines CANH and CANL. The driver translates the digital input data on the TXD pin to differential analog output on the CAN bus. The receiver translates the differential analog data on the CAN bus to digital data output to the RXD pin. The slopes of the CAN bus output signals are controlled by an internal circuit that optimizes the Electro Magnetic Emission (EME) performance. The CAN bus pin is biased to the 1/2 VCC voltage. The INH pin is active to enable the voltage regulated controlled by the INH pin.

#### Silent Mode

This is the listen-only mode and receive-only mode of the device. In the silent mode, the driver is disabled, releasing the bus pins to a recessive state. All other blocks, including the receiver, continue to operate in the normal mode. The silent mode can be used to prevent a faulty CAN controller from disrupting CAN bus network communications. The CAN bus pin is biased to the 1/2 VCC voltage. The INH pin is active to enable the voltage regulated controlled by the INH pin.



#### Standby Mode

This is the first level of the low-power mode. In the standby mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data. The low-power receiver monitors bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is active to enable the voltage regulator controlled by the INH pin. The pins RXD will reflect active wake-up requests as that  $V_{IO}$  and  $V_{BAT}$  are powered.

#### Go-to-Sleep Mode

This is the transitional mode between any mode and sleep mode. In the go-to-sleep mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data. The device transitions to sleep mode and the INH pin floats if the device is in the go-to sleep mode longer than  $t_{d_{MODE}}$ . The device will not enter sleep mode if the wake flag is set.

#### Sleep Mode

This is the second level of low-power mode as well as the lowest power mode. In the sleep mode, the driver and receiver of the CAN transceiver are disabled, and the device is unable to transmit or receive data, the low-power receiver is monitoring bus activity for valid wake-up requirements. The CAN bus pin is biased to the ground. The INH pin is floating to disable the voltage regulator controlled by the INH pin for additional system-level power saving. The EN and STB\_N pins can be used to change modes.

#### Internal Flags

The TPT1043 has 7 Internal flags to support system diagnosis, 5 of these flags can output via ERR\_N to allow the MCU to determine the status of the device and the system.

Internal Flag	Description	Available on ERR_N	Flag is cleared
UV <sub>NOM</sub>	$UV_{\text{NOM}}$ is the $V_{\text{CC}}$ and $V_{\text{IO}}$ undervoltage detection flag	No	Setting the Pwon or Wake flags, by a LOW-to-HIGH transition on STB_N or when both $V_{IO}$ and $V_{CC}$ have recovered.
UV <sub>BAT</sub>	UV <sub>BAT</sub> is the V <sub>BAT</sub> undervoltage detection flag	No	V <sub>BAT</sub> recovered
Pwon	$P_{WON}$ is the $V_{BAT}$ power-on flag	In silent mode	Entering normal mode
Wake	The Wake flag is set when the transceiver detects a local or remote wake-up request.	In standby mode, go-to-sleep mode, and sleep mode	Entering normal mode or by setting the $\mathrm{UV}_{\mathrm{NOM}}$ flag
Wake-up source	Wake-up source recognition is provided via the wake-up source flag, which is set when the wake flag is set by a local wake-up request via the wake pin.	In normal mode	Leaving normal mode

#### Table 4. Internal flags via ERR\_N



Internal Flag	Description	Available on ERR_N	Flag is cleared
Bus failure	The bus failure flag is set if the transceiver detects a bus line short-circuit condition to VBAT, VCC, or GND during four consecutive dominant- recessive cycles on pin TXD, while trying to drive the bus lines dominant.	In normal mode	Re-entering normal mode or by setting the P <sub>WON</sub> flag
The four local failure events will cause the local failure flag to be set: TXD dominant clamping, TXD-to- RXD short circuit, bus dominant clamping, and an overtemperature event.		In silent mode	Entering the normal mode or when RXD is dominant while TXD is recessive or by setting the P <sub>WON</sub> flag

#### Remote Wake-up

A dedicated wake-up pattern (ISO11898-2:2016) wakes up the TPT1043 from standby mode or sleep mode, this filtering prevents the device from being woken up by noise or spikes on the bus.

The wake-up pattern consists of the following:

- a dominant phase of at least t wake (busdom) followed by
- a recessive phase of at least t wake (busrec) followed by
- a dominant phase of at least twake (busdom)

The complete wake-up pattern must be received within  $t_{to_wake_bus}$ , otherwise, the wake-up logic will be reset to wait for the next valid wake-up pattern.

#### Device Local Faults

#### TXD Dominant Time-out

The device is featured with the TXD dominant time-out detection function. This function prevents a permanent low on the TXD pin, resulting in the CAN bus being driven into permanent dominance, which causes the CAN bus network communication to be blocked. If the TXD remains low for longer than  $t_{TXD_DTO}$ , the transmitter will be disabled until the fault flag has been cleared.

#### TXD Shorted to RXD Detection

The device is featured with the function of a short circuit between TXD and RXD detection. This function prevents the CAN bus from being locked in permanent dominance, which will result in the CAN bus network communication being blocked. The transmitter will be disabled until the fault flag has been cleared.

#### Bus Dominant Time-out

The device features the bus-dominant time-out detection function. This function prevents the CAN bus from being locked in permanent dominance, which will result in the CAN bus network communication being blocked. The fault flag is set if the CAN bus remains dominant for longer than t<sub>BUS\_DTO</sub>, and is released as soon as the bus returns to recessive.



#### Under-Voltage Lockout (UVLO)

The device integrates an under-voltage detect and lockout circuit of the supply terminal to keep the device in the protected mode if the supply voltage drops below the threshold until the supply voltage is higher than the UVLO threshold. This protects the device and system during under-voltage events on supply terminals.

#### **Over-Temperature Protection (OTP)**

The device integrates over-temperature protection circuit to prevent the device from over-heated induced damage. When the junction temperature is higher than the over-temperature protection threshold  $T_{OTP}$ , the device will shut down until the junction temperature  $T_J$  drops below the recovery threshold.



## **Application and Implementation**

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### **Application Information**

The TPT1043 device is a CAN transceiver to support CAN FD function up to 5 Mbps, with BUS protection voltage from -70 V to +70 V, over-temperature shutdown, and a -30 V to +30 V common-mode range. The VIO of TPT1043 can support the voltage level of TXD and RXD from 2.8 V to 5.5 V, and V<sub>BAT</sub> is from the battery power supply. The following sections show a typical application of the TPT1043.

### **Typical Application**

Figure 8 shows the typical application schematic of the TPT1043.



Figure 8. Typical Application Circuit



## **Tape and Reel Information**





Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPT1043Q- SO2R-S	SOP14	330	20.4	6.6	9.3	2.1	8.0	16	Q1
TPT1043Q- DFKR-S	DFN4.5X3-14L	330	16.8	3.3	4.8	1.15	8.0	12	Q1



## **Package Outline Dimensions**

### SOP14





DFN4.5X3-14





### **Order Information**

Order Number Operating Temperature Range		Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT1043Q-SO2R-S	−40 to 125°C	SOP14	1043Q	MSL1	Tape and Reel, 2500	Green
TPT1043Q-DFKR-S	−40 to 125°C	DFN4.5X3-14	1043Q	MSL1	Tape and Reel, 4000	Green

**Green**: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.



## IMPORTANT NOTICE AND DISCLAIMER

Copyright<sup>©</sup> 3PEAK 2012-2024. All rights reserved.

**Trademarks.** Any of the 思瑞浦 or 3PEAK trade names, trademarks, graphic marks, and domain names contained in this document /material are the property of 3PEAK. You may NOT reproduce, modify, publish, transmit or distribute any Trademark without the prior written consent of 3PEAK.

**Performance Information.** Performance tests or performance range contained in this document/material are either results of design simulation or actual tests conducted under designated testing environment. Any variation in testing environment or simulation environment, including but not limited to testing method, testing process or testing temperature, may affect actual performance of the product.

**Disclaimer.** 3PEAK provides technical and reliability data (including data sheets), design resources (including reference designs), application or other design recommendations, networking tools, security information and other resources "As Is". 3PEAK makes no warranty as to the absence of defects, and makes no warranties of any kind, express or implied, including without limitation, implied warranties as to merchantability, fitness for a particular purpose or non-infringement of any third-party's intellectual property rights. Unless otherwise specified in writing, products supplied by 3PEAK are not designed to be used in any life-threatening scenarios, including critical medical applications, automotive safety-critical systems, aviation, aerospace, or any situations where failure could result in bodily harm, loss of life, or significant property damage. 3PEAK disclaims all liability for any such unauthorized use.