3-V to 5.5-V, 250-kbps RS-232 Transceivers

Features

- Meets the Requirements of TIA/EIA- 232-F and ITU V.28 Standards
- Wide Power Supply Range: Single +3 V to +5.5 V
- Two Drivers and Two Receivers
- Data Rate: 250 kbps
- Requires Only Four External 0.1-μF Capacitors
- ESD Protection for RS-232 Bus Pins
  - ±15 kV (HBM)
  - ±12 kV (IEC61000-4-2, Contact Discharge)
  - ±15 kV (IEC61000-4-2, Air-Gap Discharge)

Applications

- Battery-Powered Equipment
- Industry Human Machine Interface
- Notebook, Computers
- Printers

Description

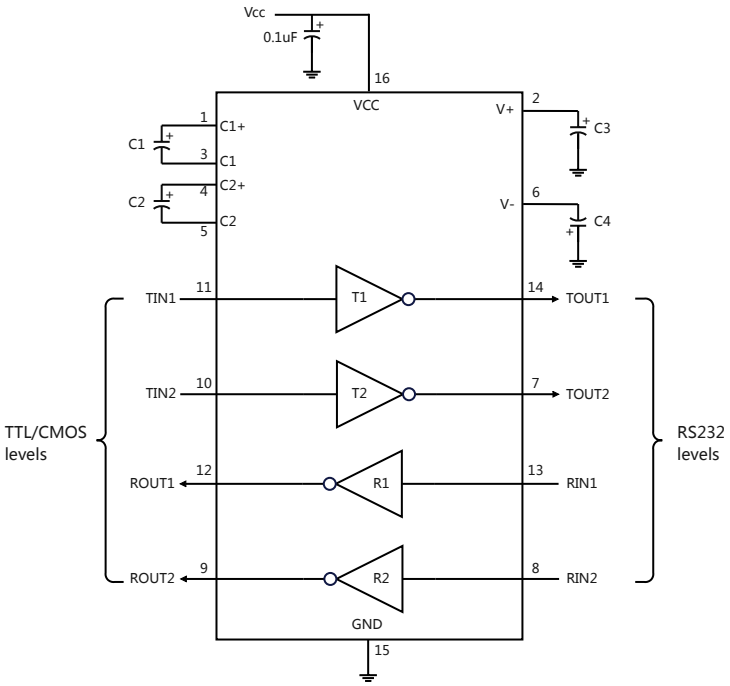
The TPT3232A is IEC61000 ESD protected, 3.0-V to 5.5-V powered transceivers that meet the RS-232 standards for balanced communication. Each receiver converts TIA/RS-232 inputs to TTL/CMOS levels.

The devices can accept ±25-V RIN inputs. The device operates at data signaling rate of 250 kbps. The TPT3232A is available in SOP16, SSOP16, and TSSOP16 packages, and is characterized from –40°C to 125°C.

Device Table

Device	Package	Body size
TPT3232A-SS3R	SSOP16	6.2 mm x 5.3 mm
TPT3232A-TS3R	TSSOP16	5.0 mm x 4.4 mm
TPT3232A-SO3R	SOP16	9.9 mm x 3.9 mm

Typical Application Circuit



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Revision History

Date	Revision	Notes
2024-03-24	Rev.A.0	Released version

Pin Configuration and Functions

TPT3232A
SOP16/TSSOP16/SSOP16 Package
Top View

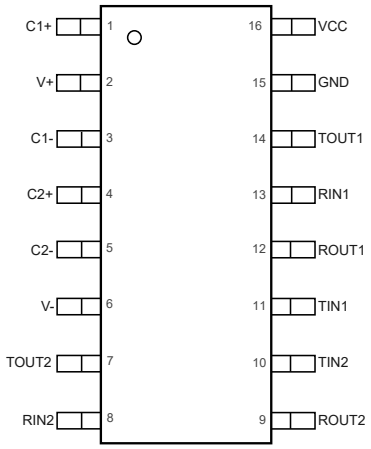


Table 1. Pin Functions: TPT3232A

Pin		I/O	Description
No.	Name		
1	C1+		Positive lead of C1 capacitor
2	V+	Output	Positive charge pump output for storage capacitor only
3	C1-		Negative lead of C1 capacitor
4	C2+		Positive lead of C2 capacitor
5	C2-		Negative lead of C2 capacitor
6	V-	Output	Negative charge pump output for storage capacitor only
7	TOUT2	Output	Output of RS232 driver, RS232 level
8	RIN2	Input	Input of RS232 receiver, RS232 level
9	ROUT2	Output	Output of RS232 receiver, TTL/CMOS level
10	TIN2	Input	Input of RS232 driver, TTL/CMOS level
11	TIN1	Input	Input of RS232 driver, TTL/CMOS level
12	ROUT1	Output	Output of RS232 receiver, TTL/CMOS level
13	RIN1	Input	Input of RS232 receiver, RS232 level
14	TOUT1	Output	Output of RS232 driver, RS232 level
15	GND		Ground
16	VCC		Supply voltage

Specifications

Absolute Maximum Ratings (1)

Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	−0.3	6	V
V+	Positive Output Supply Voltage	−0.3	7	V
V–	Negative Output Supply Voltage	−7	0.3	V
V+ – V–	Supply Voltage Difference		13	V
T_{IN1}, T_{IN2}	Input Voltage of Driver, TTL/CMOS Level	−0.3	6	V
T_{OUT1}, T_{OUT2}	Output Voltage of Driver, RS232 Level	−13.2	+13.2	V
R_{IN1}, R_{IN2}	Input Voltage of Receiver, RS232 Level	−25	+25	V
R_{OUT1}, R_{OUT2}	Output Voltage of Receiver, TTL/CMOS Level	−0.3	VCC + 0.3	V
T_J	Operating Virtual Junction Temperature		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
(2) This data was taken with the JEDEC low effective thermal conductivity test board.
(3) This data was taken with the JEDEC standard multilayer test boards.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Value	Unit
IEC	IEC Contact Discharge	IEC-61000-4-2, Bus Pin: TOUT1, TOUT2, RIN1, RIN2	±12	kV
	IEC Air-Gap Discharge	IEC-61000-4-2, Bus Pin: TOUT1, TOUT2, RIN1, RIN2	±15	kV
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001, Bus Pin: TOUT1, TOUT2, RIN1, RIN2	±15	kV
		ANSI/ESDA/JEDEC JS-001, All Pin	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002, All Pin	±1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Unit
V_{CC}	Power Supply	3.0	5.5	V
$V_{IH(TXD)}$	Driver HIGH Level Input Voltage, V_{CC} = 5 V	2.4	5.5	V
	Driver HIGH Level Input Voltage, V_{CC} = 3.3 V	2	5.5	V
$V_{IL(TXD)}$	Driver LOW Level Input Voltage		0.8	V
T_A	Operating Ambient Temperature	−40	125	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SSOP16	103	45	°C/W
TSSOP16	115	48	°C/W
SOP16	91	43	°C/W

Electrical Characteristics

All test conditions: V_{CC} = 3.0 V to 5.5 V, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
I_{CC}	Icc = Supply Current	no load, V_{CC} = 3.3 V, TINx = GND or V_{CC}, T_A = 25°C		0.3	1	mA
Driver (TX)						
V_{OH}	Output High Voltage	D_{IN} = GND	5.0	5.4		V
V_{OL}	Output Low Voltage	T_{OUT} at R_L = 3 kΩ to GND		−5.4	−5.0	V
I_{IH}	High-level Input Leakage Current	T_{IN1}, T_{IN2}, V_{IN} = V_{CC}	−1		1	μA
I_{IL}	Low-level Input Leakage Current	T_{IN1}, T_{IN2}, V_{IN} = 0 V	−1		1	μA
I_{OS}	Output Short-Circuit Current (1)	T_{OUT} = 0 V	−60		60	mA
R_O	Output Resistance (1) (2)	V_{CC} = V+ = V− = 0 V, T_{OUTx} = ±2 V (1)	0.3	1500		kΩ
Receiver (RX)						
V_{IH}	Input Voltage of Logic High	T_{IN1}, T_{IN2}, V_{CC} = 3.3 V	2			V
		T_{IN1}, T_{IN2}, V_{CC} = 5.0 V	2.4			V
V_{IL}	Input Voltage of Logic Low	T_{IN1}, T_{IN2}, V_{CC} = 3.3 V			0.8	V
		T_{IN1}, T_{IN2}, V_{CC} = 5.0 V			0.8	V
V_{OL}	Output Voltage Low	V_{OL}, I_{OUT} = −1.5 mA			0.3	V
V_{OH}	Output Voltage High	V_{OH}, I_{OUT} = 1.5 mA	VCC − 0.5			V
V_I	Receiver Input Voltage (1)		−25		25	V
V_{TH-}	Input Threshold Low	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5.0 V	0.8	1.5		V
V_{TH+}	Input Threshold High	V_{CC} = 3.3 V		1.3	2.4	V
		V_{CC} = 5.0 V		1.7	2.4	V
V_{hys}	Input Hysteresis (1)			0.3		V
R_I	Input Resistance (1)(2)			5		kΩ

(1) Test data based on bench test and design simulation, NOT test in production.
(2) Typ data is based on bench test by LRC meter E4980AL.

Electrical Characteristics (continued)

All test conditions: V_{CC} = 3.0 V to 5.5 V, T_A = −40°C to 125°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
f_{max}	Maximum Data Rate (1)	R_L = 3 kΩ, C_L = 1000 pF (max), one driver switching		250		kbps
tDPHL	Driver Propagation Delay, high to low output, tDPHL (1)	Driver input to Driver output, C_L = 150 pF~1000 pF R_L = 3 kΩ, C_L = 150 pF~1000 pF		500	1000	ns
tDPLH	Driver Propagation Delay, low to high output, tDPLH (1)	Driver input to Driver output, C_L = 150 pF~1000 pF R_L = 3 kΩ, C_L = 150 pF~1000 pF		500	1000	ns
tDsk	Driver Skew (1)	| tDPHL – tDPLH |		200		ns
SR_{tr}	Transition-Region Slew Rate	Vcc = 3.3 V or 5.0 V, R_L = 3 kΩ, C_L = 150 pF~1000 pF	6	16	30	V/μs
tRPHL	Receiver Propagation Delay, high to low output, tRPHL	Receiver input to receiver output, CL = 150 pF		150	300	ns
tRPLH	Receiver Propagation Delay, low to high output, tRPLH	Receiver input to receiver output, CL = 150 pF		150	300	ns
tRsk	Receiver Skew (1)	| tRPHL – tRPLH |		50		ns

(1) Test data is based on bench test and design simulation, NOT test in production.

Typical Performance Characteristics

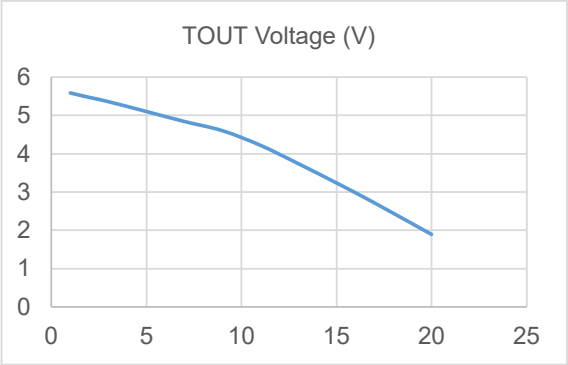


Figure 1. TOUT_VOH(V) vs TOUT Current (mA)

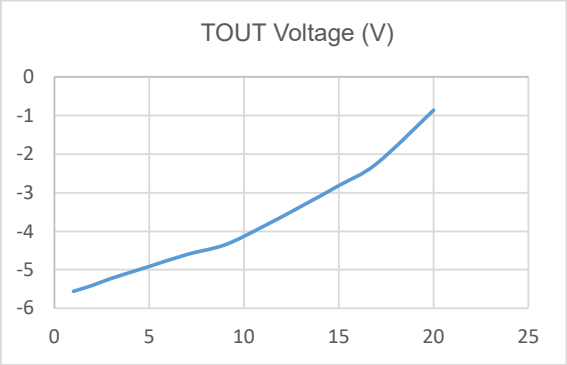


Figure 2. TOUT_VOL(V) vs TOUT Current (mA)

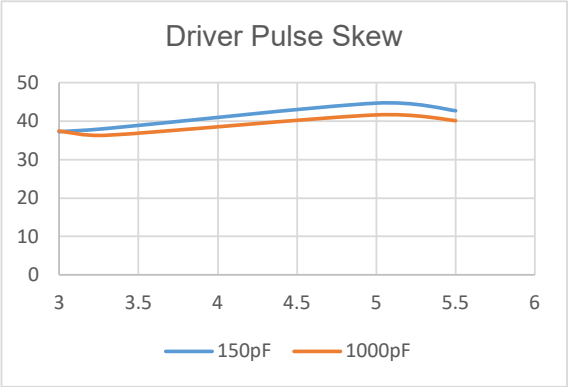


Figure 3. Driver Skew (ns) per VCC(V) with C_{Load}

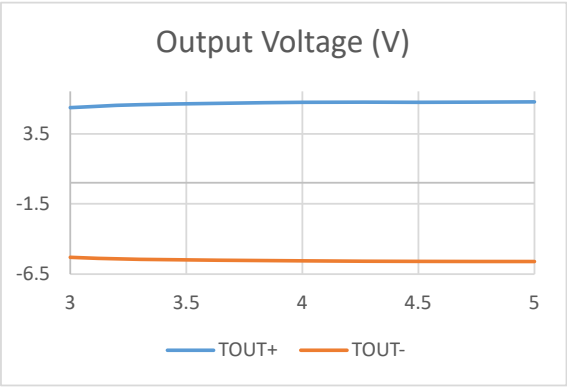


Figure 4. Output Votage(V) per VCC(V)

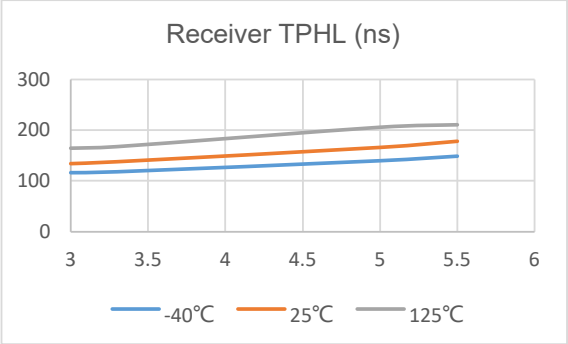


Figure 5. Receiver TPHL(ns) per Temperature(℃)

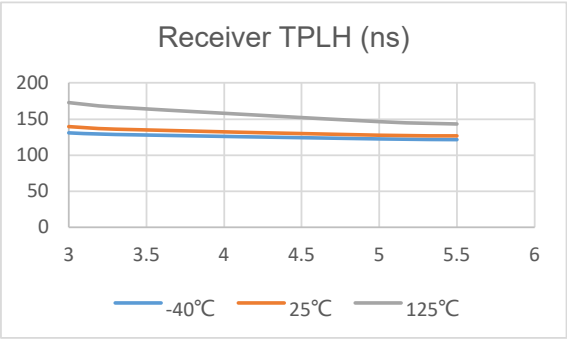


Figure 6. Receiver TPLH(ns) per Temperature(℃)

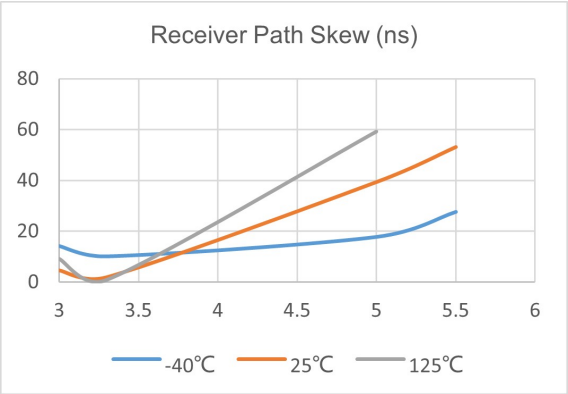


Figure 7. Receiver Skew(ns) per Temperature(℃)

Detailed Description

Overview

The TPT3232A is IEC61000 ESD protected, 3.0-V to 5.5-V powered transceivers that meet the RS-232 standards for balanced communication. Each receiver converts TIA/RS-232 inputs to TTL/CMOS levels.

The devices can accept ±25-V RIN inputs. The device operates at data signaling rate of 250 kbps. The TPT3232A is available in SOP16, SSOP16, and TSSOP16 packages, and is characterized from –40°C to 125°C.

Functional Block Diagram

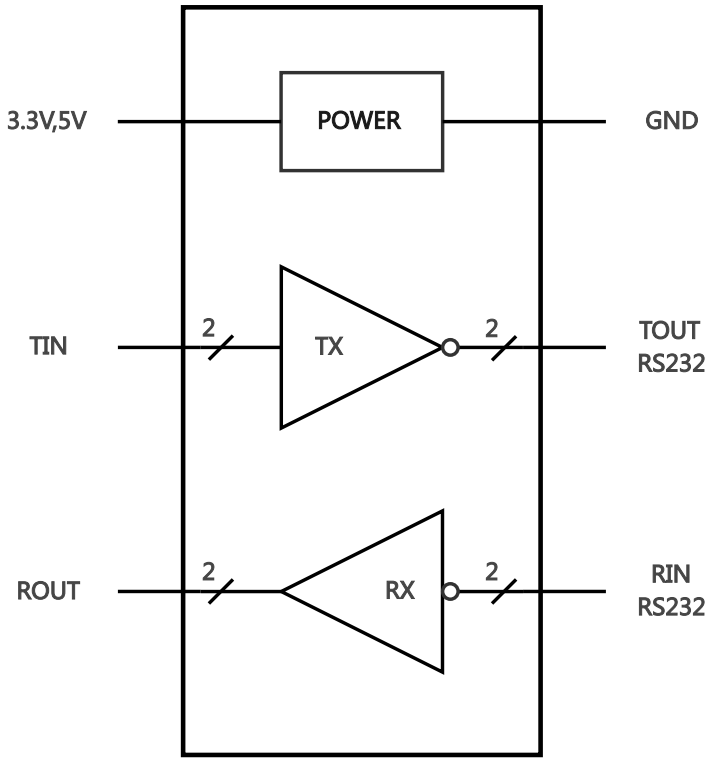


Figure 8. Functional Block Diagram

Parameter Measurement Information

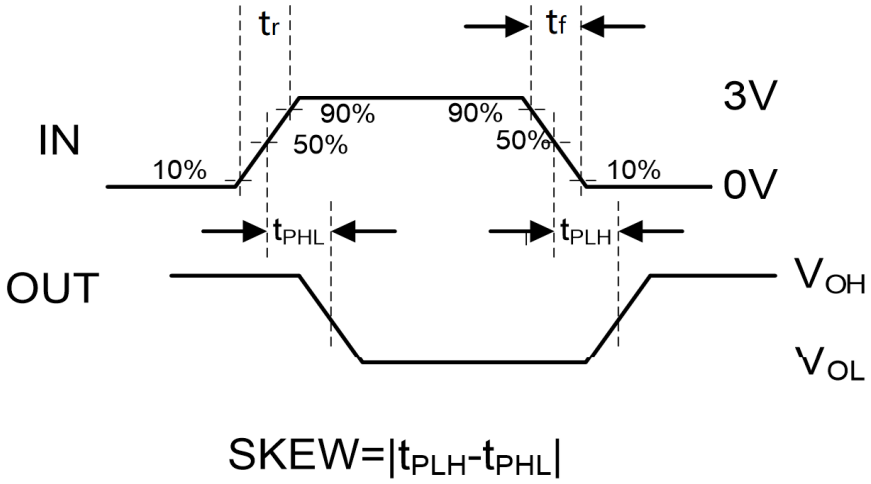


Figure 9. Receiver Propagation Delay and Receiver Skew

Application and Implementation

Note

Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Typical Application

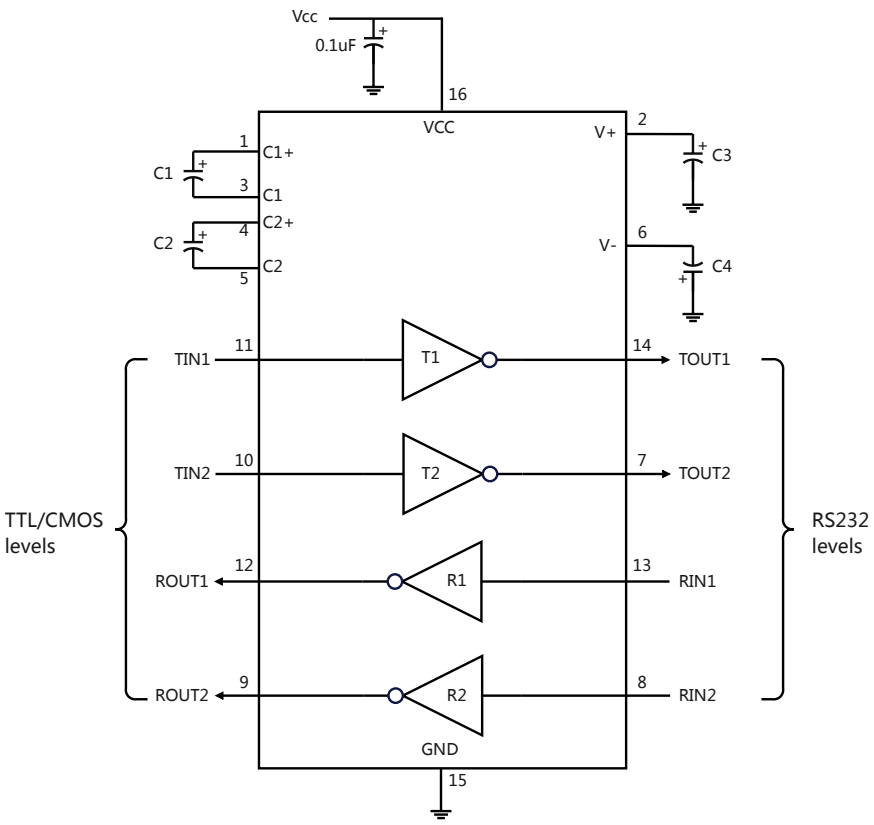


Figure 10. Typical Application Circuit

Non-polarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown in Figure 10. The recommended capacitor value of C1 to C4 is in Table 2. All cap is 0.1 uF for TPT3232A.

Table 2. Required Minimum Capacitor Values

V_{CC}(V)	C1(μF)	C2, C3, C4(μF)
3.0 to 5.5	0.1	0.1

Layout

Layout Guideline

Keep the traces of external capacitors as short as possible and help the C1 and C2 nodes to have the fastest rise and fall times.

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. Figure 12 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

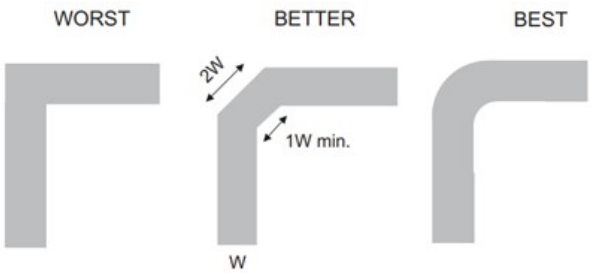


Figure 11. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Layout Example

Figure 12 shows the location of external components as they appear on the PCB diagram.

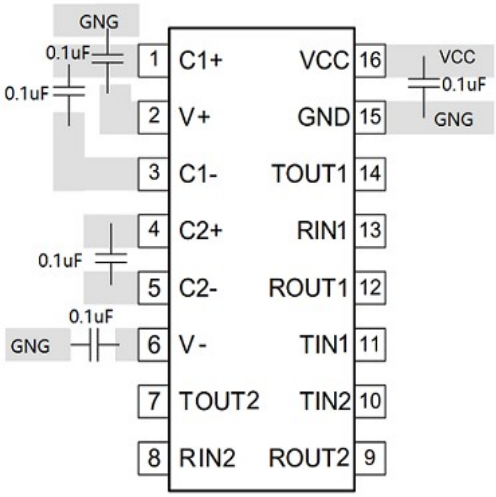
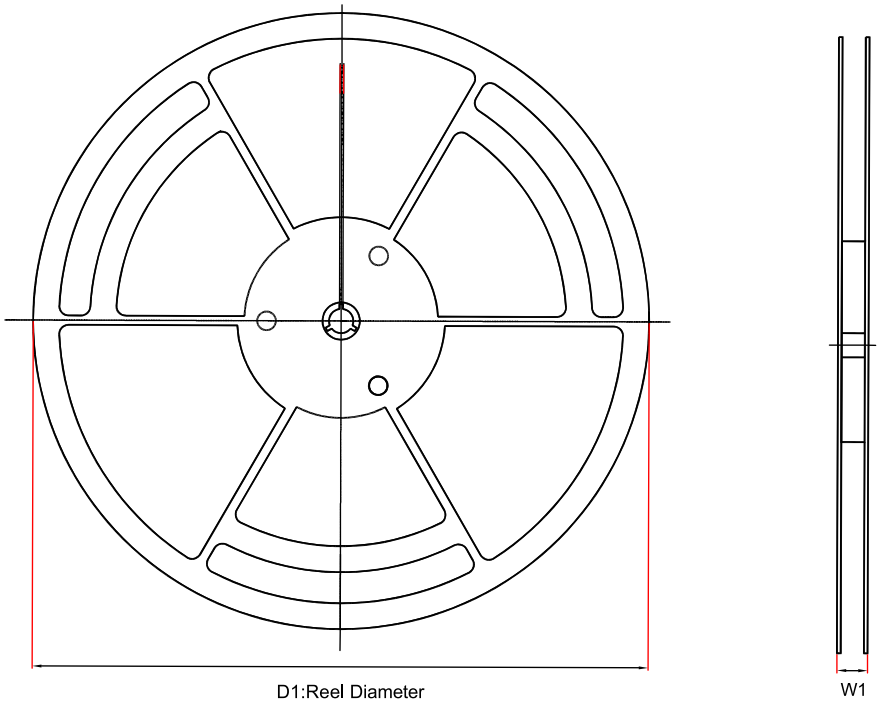
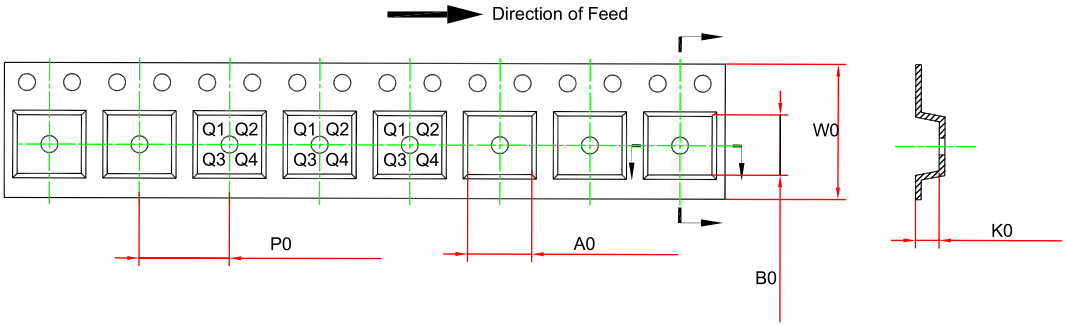


Figure 12. Layout Example Diagram

Tape and Reel Information



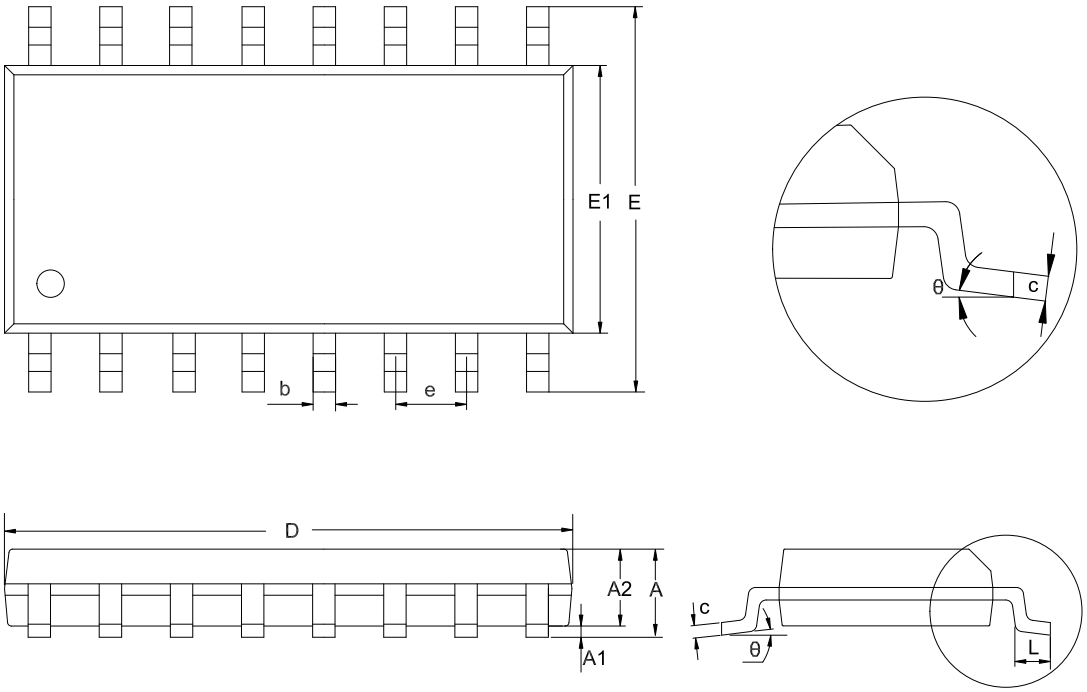


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT3232A-SO3R	SOP16	330	6.6	2.1	16.0	21.6	10.4	8.0	Q1
TPT3232A-TS3R	TSSOP16	330	6.8	1.3	12.0	17.6	5.5	8.0	Q1
TPT3232A-SS3R	SSOP16	330	6.4	2.1	12.0	17.6	5.4	8.0	Q1

Package Outline Dimensions

SOP16-A

Package Outline Dimensions SO3(SOP-16-A)



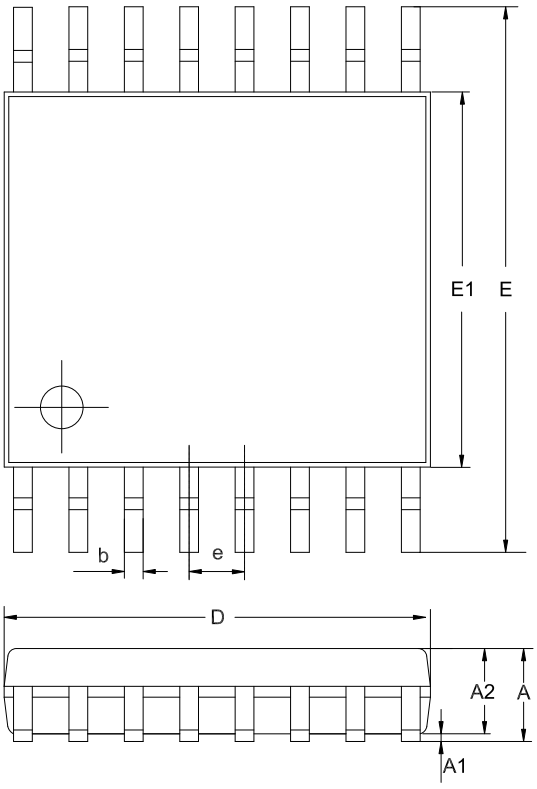
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.300	1.600	0.051	0.063
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.000	0.386	0.394
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

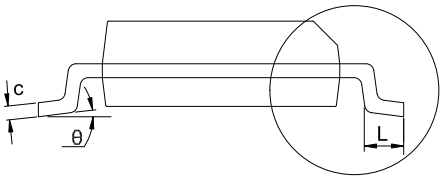
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

TSSOP16

Package Outline Dimensions TS3(TSSOP-16-A)





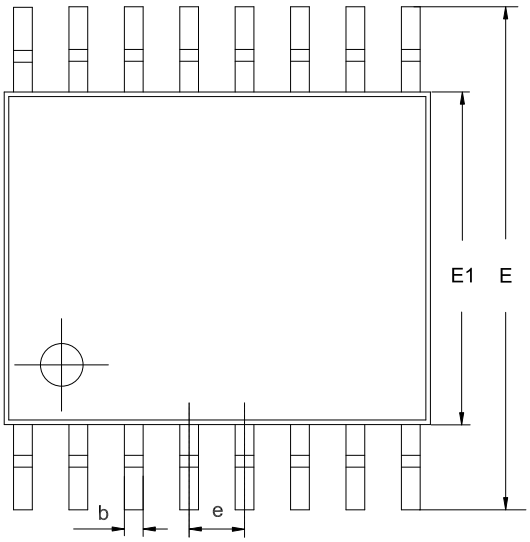
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.200	6.600	0.244	0.260
E1	4.300	4.500	0.169	0.177
e	0.650 BSC		0.026 BSC	
L	0.450	0.750	0.018	0.030
θ	0	8°	0	8°

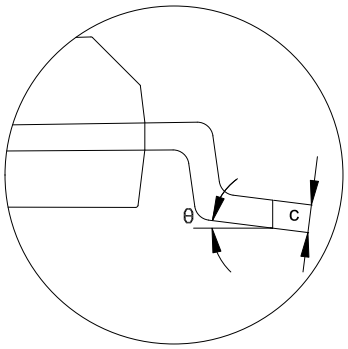
NOTES

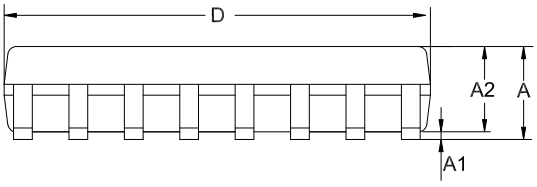
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

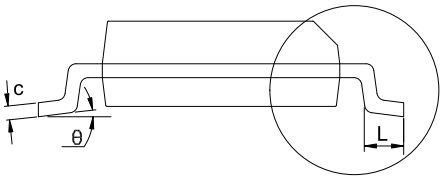
SSOP16

Package Outline Dimensions SS3(SSOP-16-A)









Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.500	2.000	0.059	0.079
A1	0.050	0.250	0.002	0.010
A2	1.400	1.850	0.055	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	5.900	6.500	0.232	0.256
E	7.400	8.200	0.291	0.323
E1	5.000	5.600	0.197	0.220
e	0.650 BSC		0.026 BSC	
L	0.550	1.050	0.022	0.041
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Junction Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT3232A-SS3R	−40 to 125°C	SSOP16	3232A	MSL3	Tape and Reel,2000	Green
TPT3232A-TS3R	−40 to 125°C	TSSOP16	3232A	MSL3	Tape and Reel,3000	Green
TPT3232A-SO3R	−40 to 125°C	SOP16	3232A	MSL3	Tape and Reel,2500	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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