Features

- Meet the Full Duplex EIA-485 Standard
- Hot Plug Circuitry - Tx and Rx Outputs Remain Three-State During Power-up/Power-down
- Supply voltage: 3.0V ~ 5.5V
- Input Common-mode Range: -7V ~ +12 V
- Data Rate: 32Mbps
- Up to 256 Nodes on a Bus (1/8 unit load)
- Full Fail-safe Receiver (Open, Short, Terminated)
- Bus-Pin Protection:
  - ±20 kV HBM ESD
  - ±12 kV IEC61000-4-2 Contact Discharge
  - ±15 kV IEC61000-4-2 Air Discharge
- –40°C to 125°C Operation Temperature Range

Description

The TPT480 and TPT482 is IEC61000 ESD protected, which support ±12 kV IEC contact and ±15 kV IEC air discharge. 3.0V ~ 5.5V transceivers that meet the RS-485 and RS-422 standards for Full Duplex communication.

Transmitters in this family deliver exceptional differential output voltages into the RS-485 required 54Ω load. The devices have very low bus currents so they present a true “1/8 unit load” to the RS-485 bus. This allows up to 256 transceivers on the network without using repeaters.

Receiver (Rx) inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven bus.

The TPT480 and TPT482 is designed for full-duplex RS485, and support SOP8, DFN3X3-8, MSOP10 and SOP14 package, which is characterized from –40°C to 125°C.

Applications

- Industrial Control
- Grid Infrastructure
- Video Surveillance
- Communication Infrastructure

Simplified Schematic

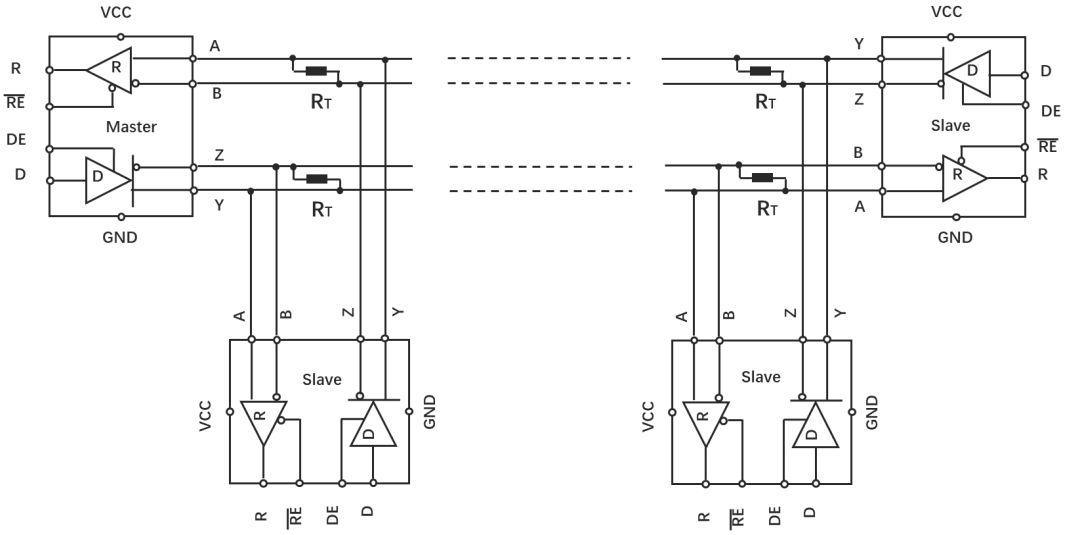


Table of Contents

Features 1
Applications 1
Description 1
Simplified Schematic 1
Table of Contents 2
Revision History 3
Device Table 4
Pin Configuration and Functions – TPT480 5
Pin Configuration and Functions – TPT482-SO2R 6
Pin Configuration and Functions – TPT482-VS2R 7
Absolute Maximum Ratings 8
Recommended Operating Conditions 8
ESD Rating 9
Thermal Information 9
Electrical Characteristics 10
Test Circuits and Waveforms 13
Test Circuits and Waveforms (continue) 14
Detailed Description 15
Overview 15
Function Block diagram: 15
Functional Table 15
Application and Implementation 18
Application Information 18
Layout 19
Layout Guideline 19
Tape and Reel Information 20
Package Outline Dimensions 21
SO1R (SOP-8) 21
DF6R (DFN3x3-8L) 22
Package Outline Dimensions (Continued) 23
SO2R (SOP-14) 23
Package Outline Dimensions (Continued) 24
VS2R (MSOP-10) 24
Order Information 25
IMPORTANT NOTICE AND DISCLAIMER 26

Revision History

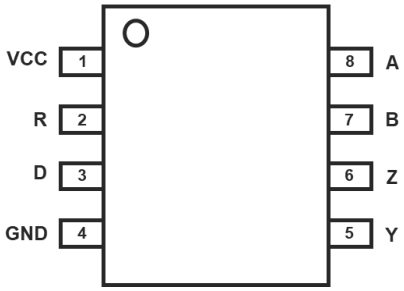
Date	Revision	Notes
2023/01/31	Rev. A0	Released version
2023/04/04	Rev. A1	Updated DF6R POD as DFN3X3-8-B
2023/08/15	Rev. A2	Added TPT482 MSOP10 version
2024/03/06	Rev. A3	Added the truth table of TPT480

Device Table

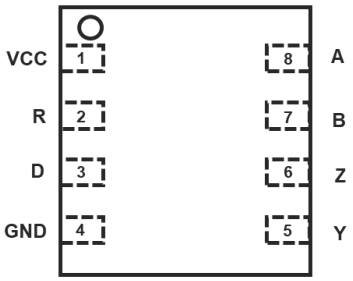
Part Number	Duplex	Enable	Data Rate	Package
TPT480L1-SO1R	Full	None	32Mbps	SOP-8
TPT480-DF6R	Full	None	32Mbps	DFN3X3-8
TPT482-SO2R	Full	DE, /RE	32Mbps	SOP-14
TPT482-VS2R	Full	DE, /RE	32Mbps	MSOP10

Pin Configuration and Functions – TPT480

SOP8

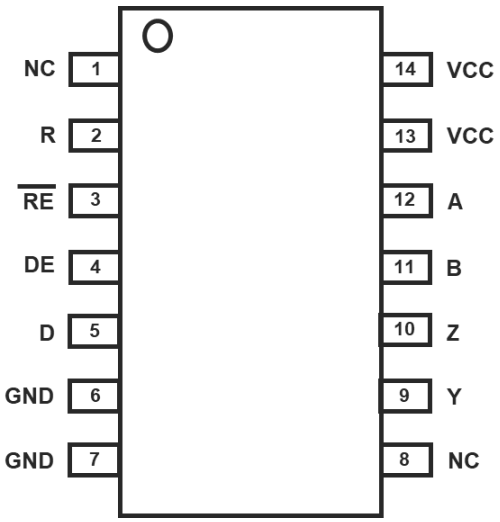


DFN3X3-8L



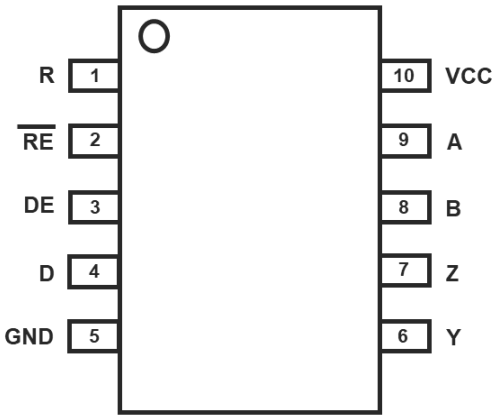
Pin No.	Pin Name	I/O	Description
1	VCC	Power	Power Supply
2	R	Digital output	Receiver Output
3	D	Digital input	Driver Input
4	GND	Ground	Ground
5	Y	Bus output	Noninverting Driver Output
6	Z	Bus output	Inverting Driver Output
7	B	Bus input	Inverting Receiver Input
8	A	Bus input	Noninverting Receiver Input
	Thermal pad		Internal connected to Ground as DFN package

Pin Configuration and Functions – TPT482-SO2R



Pin No.	Pin Name	I/O	Description
1	NC		
2	R	Digital output	Receiver Output
3	/RE	Digital input	Receiver Output Enable
4	DE	Digital input	Driver Output Enable
5	D	Digital input	Driver Input
6	GND	Ground	Ground
7	GND	Ground	Ground
8	NC		
9	Y	Bus output	Noninverting Driver Output
10	Z	Bus output	Inverting Driver Output
11	B	Bus input	Inverting Receiver Input
12	A	Bus input	Noninverting Receiver Input
13	VCC	Power	Power Supply
14	VCC	Power	Power Supply

Pin Configuration and Functions – TPT482-VS2R



Pin No.	Pin Name	I/O	Description
1	R	Digital output	Receiver Output
2	/RE	Digital input	Receiver Output Enable
3	DE	Digital input	Driver Output Enable
4	D	Digital input	Driver Input
5	GND	Ground	Ground
6	Y	Bus output	Noninverting Driver Output
7	Z	Bus output	Inverting Driver Output
8	B	Bus input	Inverting Receiver Input
9	A	Bus input	Noninverting Receiver Input
10	VCC	Power	Power Supply

Absolute Maximum Ratings

Parameters	Rating
VCC to GND	-0.3V to +7V
Voltage at Logic pin: D, DE, /RE, R	-0.3V to VCC + 0.3V
Voltage at Bus pin: A, B, Y, Z (1)	-15V to +15V
Operating Temperature Range	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C

(1) Support ±15V in receiver mode, and -8 ~+13V in driver mode

(2) Stresses beyond the *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*.

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Supply voltage	3.0		5.5	V
V_I	Input voltage at any bus terminal(1)	-7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		VCC	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V
V_{ID}	Differential input voltage	-7		12	V
R_L	Differential load resistance	54			Ω
T_A	Operating ambient temperature	-40		125	°C
T_J	Junction temperature	-40		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

ESD Rating

		Value	Unit
IEC-61000-4-2, Contact Discharge	Bus Pin	±12	kV
IEC-61000-4-2, Air-Gap Discharge	Bus Pin	±15	kV
HBM, per ANSI/ESDA/JEDEC JS-001 / ANSI/ESD STM5.5.1	Bus Pin	±20	kV
	All Pin Except Bus Pin	±4	kV
CDM, per ANSI/ESDA/JEDEC JS-002	All Pin	±1.5	kV

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
8-Pin SOP	120	64	°C/W
8-Pin DFN	65	45	°C/W
10-Pin MSOP	150	58	°C/W
14-Pin SOIC	102	39	°C/W

Electrical Characteristics

All test condition is VCC = 3.3V~5.0V, T_A = -40 ~ +125°C, unless otherwise noted.

Symbol	Parameter	Test Conditions		Min		MAX	Unit
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 54 Ω , VCC=3.3V		1.5	2.2		V
		R_L = 54 Ω , VCC=5.0V		2.0	3.3		V
		R_L = 100 Ω, VCC = 3.3V		1.5	2.6		V
		R_L = 100 Ω, VCC = 5.0V		3.0	3.9		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver	R_L = 54 Ω, C_L = 50 pF，375 Ω on A/B: –7 V to 12V, VCC=3.3V		–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output	Center of two 27-Ω load resistors		1	VCC/2	3	V
ΔV_{OC}	Change in differential driver output			–200		200	mV
C_{OD}	Differential output capacitance [1]				15		pF
V_{IT+}	Positive-going receiver differential				-110	–50	mV
V_{IT-}	Negative-going receiver differential			–200	–130		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} – V_{IT-}) [1]				50		mV
V_{OH}	Receiver high-level output voltage	VCC = 3.3 V, I_{OH} = -8 mA		2.6	3.0		V
		VCC = 5 V, I_{OH} = -8 mA		4.1	4.8		
V_{OL}	Receiver low-level output voltage	VCC = 3.3 V, I_{OH} = -8 mA			0.19	0.4	V
		VCC = 5 V, I_{OH} = -8 mA			0.02	0.4	
V_{IH}	Input High Logic Leve	D, DE, /RE		2.0			V
V_{IL}	Input Low Logic Leve	D, DE, /RE				0.8	V
I_{IN}	Driver input, driver enable, and	D, DE, /RE		–5		5	μA
I_{OZ}	Driver output high-Z current	V_O = -7V		–100		0	μA
		V_O = 12V		0		125	
I_{OZ}	Receiver high-Z current	V_O = 0 V or VCC		–1		1	μA
I_{OS}	Driver short-circuit output current	VY, VZ= -7V ~ 12V		–250		250	mA
		VY, VZ =0V or VCC		-180		180	mA
$I_{IA/B}$	Bus input current (disabled driver)	DE = 0 V, RE=VCC	V_I = 12 V,		55	125	μA
			V_I = –7 V,	-100	-50		μA
I_{CC}	Supply current (quiescent), 32Mpbs	Driver and Receiver enabled	DE=VCC, RE = GND, No load		1200	2500	μA
		Driver enabled, receiver disabled	DE=VCC, RE = VCC, No load		1200	2500	μA
		Driver disabled, receiver enabled	DE=GND, RE = GND, No load		1000	2200	μA
		Driver and receiver disabled	DE=GND, RE = VCC, No load	-5		5	μA

Note:

[1]. Parameters are provided by lab bench test and design simulation, NOT test in production

Switching Characteristics, VCC= 5.0V

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times (1)	RL = 54 Ω, CL=50pF	See Figure 2	4	6	10	ns
t_{PHL}, t_{PLH}	Driver propagation delay				19	30	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$ (2)					10	
t_{PHZ}, t_{PLZ}	Driver disable time	/RE=0 or VCC	See Figure 3		37	50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			21	40	ns
		Receiver disabled			1760	2500	
Receiver							
t_r, t_f	Driver differential-output rise and fall times (1)			2	4	6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				36	45	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$ (2)					20	
t_{PHZ}, t_{PLZ}	Receiver disable time	DE=0 or VCC	See Figure 6		15	25	ns
t_{PZH}, t_{PZL}	Receiver enable time	Driver enabled			14	25	ns
		Driver disabled			1750	2500	

Note:

(1) For the typical value of tr, tf, it is provided by lab bench test. The maximum and minimum value is provided by design simulation. NOT test in production

(2) The maximum value of tSK(P) is provided by design simulation, NOT test in production

Switching Characteristics, VCC=3.3V

Parameter		Conditions		Min	Typ	Max	Units
Driver							
t_r, t_f	Driver differential-output rise and fall times (1)	RL = 54 Ω, CL=50pF	See Figure 2	4	6	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay				22	30	
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$ (2)					10	
t_{PHZ}, t_{PLZ}	Driver disable time	/RE=0 or VCC	See Figure 3		40	55	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			30	50	ns
		Receiver disabled			2560	4000	

Parameter		Conditions		Min	Typ	Max	Units
Receiver							
t_r, t_f	Driver differential-output rise and fall times (1)			2	4	8	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				47	60	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$ (2)					20	
t_{PHZ}, t_{PLZ}	Receiver disable time	DE=0 or VCC	See Figure 6		21	30	ns
t_{PZH}, t_{PZL}	Receiver enable time	Driver enabled			17	30	ns
		Driver disabled			2550	4000	

Note:

(1) For the typical value of tr, tf, it is provided by lab bench test. The maximum and minimum value is provided by design simulation, NOT test in production

(2) The maximum value of tSK(P) is provided by design simulation, NOT test in production

Test Circuits and Waveforms

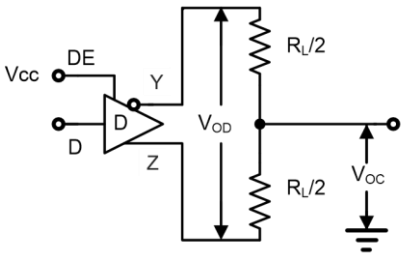


Figure 1A. VOD and VOC

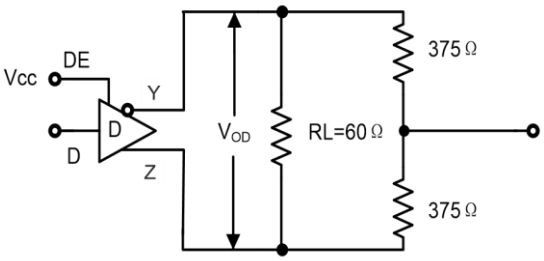


Figure 1B. VOD with Common Mode Load

Figure 1. DC Driver Test Circuits

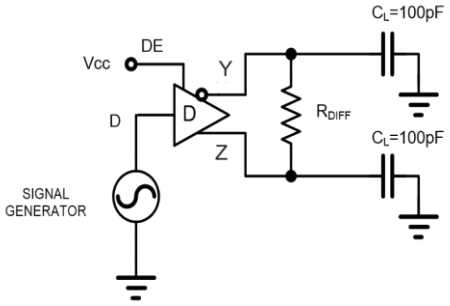


Figure 2A. Test Circuit

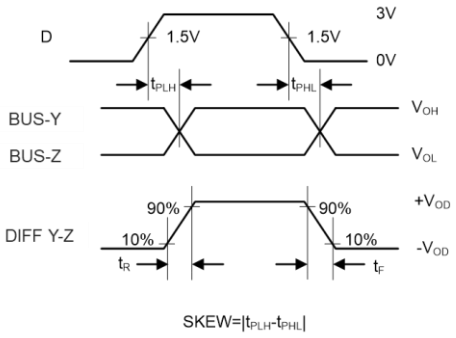


Figure 2B. Measurement Points

Figure 2. Driver Propagation Delay and Differential Transition Times

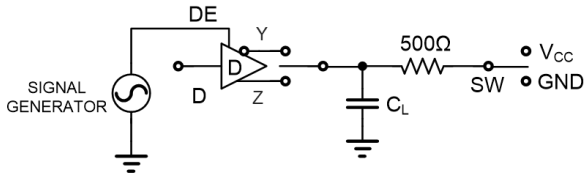


Figure 3A. Test Circuit

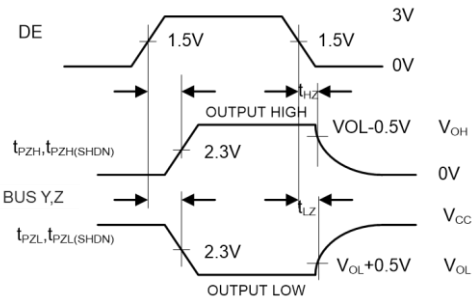


Figure 3B. Measurement Points

PARAMETER	OUTPUT	RE	DI	SW	CL (pF)
tPHZ	Y/Z	X	1/0	GND	15
tPLZ	Y/Z	X	0/1	VCC	15
tPZH	Y/Z	0	1/0	GND	100
tPZL	Y/Z	0	0/1	VCC	100
tPZH(SHDN)	Y/Z	1	1/0	GND	100
tPZL(SHDN)	Y/Z	1	0/1	VCC	100

Figure 3. Driver Enable and Disable Times

Test Circuits and Waveforms (continue)

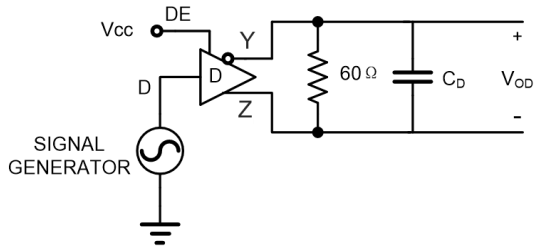


Figure 4A. Test Circuit

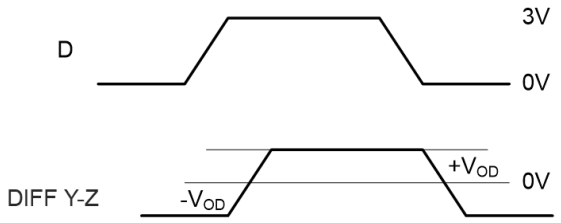


Figure 4B. Measurement Points

Figure 4. Driver Data rate

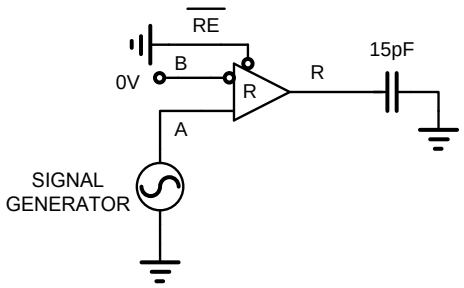


Figure 5A. Test Circuit

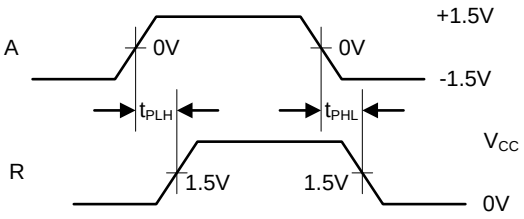
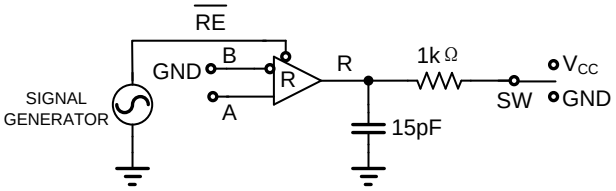


Figure 5B. Measurement Points

Figure 5. Receiver Propagation Delay and Data rate



PARAMETER	DE	A	SW
tPHZ	1	+1.5V	GND
tPLZ	1	-1.5V	VCC
tPZH	1	+1.5V	GND
tPZL	1	-1.5V	VCC
tPZH(SHDN)	0	+1.5V	GND
tPZL(SHDN)	0	-1.5V	VCC

Figure 6A. Test Circuit

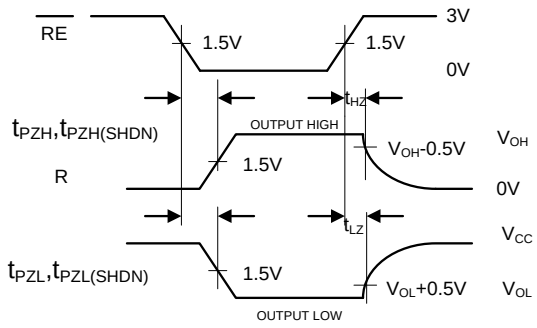


Figure 6B. Measurement Points

Figure 6. Receiver Enable and Disable Times

Detailed Description

Overview

The TPT480/482 is a Full-Duplex RS-485/RS-422 transceivers with robust HBM and IEC 61000 ESD protection. The device build in fail-safe circuit, when the receiver input is open or shorted, or idle mode, it will generate a logic-high receiver output. The TPT48x supports hot-swap function allowing line insertion to avoid wrong data transmission, and optimizes the drivers slew-rate to minimize EMI and reduce reflections caused by different terminated cables, then TPT48x can support the high communication speed up to 32Mbps.

The TPT48x operates from a single +3.3V to 5.0V power supply, the driver is designed with output short-circuit current limitation, together with thermal-shutdown circuitry to protect drivers in the status of excessive power dissipation. In active mode, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

In the typical RS485 communication, twisted-pair lines are connected backward in the network.

Function Block diagram:

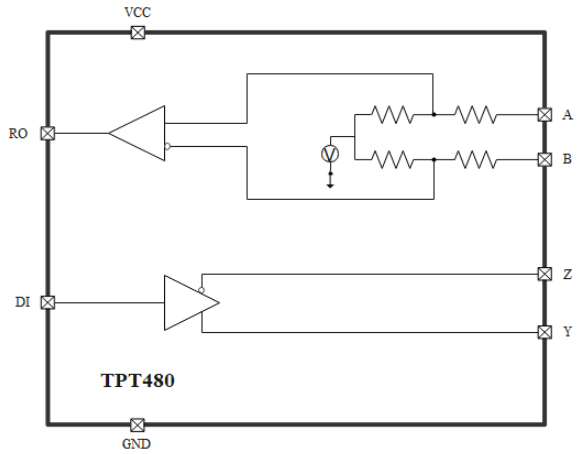


Figure 7-A. TPT480 block diagram

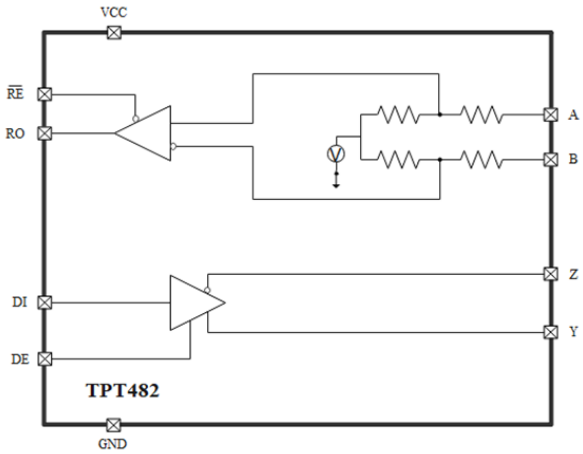


Figure 7-B. TPT482 block diagram

Functional Table

Device Functional Modes for TPT482 – driver function

When the DE (driver enable pin) is in high level, the differential outputs Y and Z follow the logic states at data input DI(D in pinout mapping). A logic high D makes Y as high level and Z as low level output, then the differential output voltage V_{OD} = V_Y – V_Z is positive. When D is low, the output states reverse: Z is high and Y is low, then V_{OD} is negative.

When DE is in low level, both outputs turn high-Z (high-impedance), and logic state at D is uncorrelated. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-Z) as default. The D pin has an internal

pull-up resistor to V_{CC}, when left open while the driver is enabled, output Y turns high and Z turns low. Please see details in below truth table.

Driver Function Table of TPT482

Input	Enable	Output	Output	Description
D	DE	Y	Z	
H	H	H	L	Actively drives bus High
L	H	L	H	Actively drives bus Low
X	L	Z	Z	Driver disabled
Open	H	H	L	Actively drives bus High by default

X = don't care

Z = high impedance

Device Functional Modes for TPT482 – receiver function

When the pin /RE (receiver enable) is in logic low, the receiver is enabled. When the differential input voltage defined as V_{ID} = V_A – V_B is higher than the V_{IT+} (positive input threshold), the receiver output RO (R in pinout mapping) turns high. When V_{ID} is lower than the V_{IT-} (negative input threshold), the receiver output R turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When RE is logic high or left open, the receiver output is high-Z and the magnitude and polarity of VID are uncorrelated. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is in open state (disconnected from the bus), the bus lines are short (shorted to one another), or the bus is in idle (not actively driven). Please see details in below truth table.

Receiver Function Table of TPT482

Input	Input	Output	Description
V_{ID} = V_A – V_B	/RE	R	
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
Open	L	H	Fail-safe high output
Short	L	H	Fail-safe high output
Idle (Terminated)	L	H	Fail-safe high output

X = don't care

Z = high impedance

Device Functional Modes for TPT480 – driver function

Since there is no enable function pins, the driver and receiver are fully enabled, then the differential outputs Y and Z follow the logic states of input D at all times. A logic high at D causes Y to turn high and Z to turn low, then the differential output voltage defined as V_{OD} = V_Y – V_Z is positive. When D is low, the output states reverse: Z turns high and Y becomes low, then

V_{OD} is negative. The D pin has an internal pull-up resistor to VCC, when left open while the driver is enabled, output Y turns high and Z turns low. Please see details in below truth table.

Driver Function Table of TPT480

Input	Output	Output	Description
D	Y	Z	
H	H	L	Actively drives bus High
L	L	H	Actively drives bus Low
X	Z	Z	Driver disabled
Open	H	L	Actively drives bus High by default

X = don't care

Z = high impedance

Device Functional Modes for TPT480 – receiver function

When the differential input $V_{ID} = V_A – V_B$ is higher than the V_{IT+}, the receiver output R turns high. When V_{ID} is less than the V_{IT-}, the receiver output R turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is open, short, or idle state. Please see details in below truth table.

Receiver Function Table of TPT480

Input	Output	Description
$V_{ID} = V_A – V_B$	R	
$V_{ID} > V_{IT+}$	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	Receive valid bus Low
Open	H	Fail-safe high output
Short	H	Fail-safe high output
Idle (Terminated)	H	Fail-safe high output

X = don't care

Z = high impedance

Application and Implementation

Note
Information in the following application sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

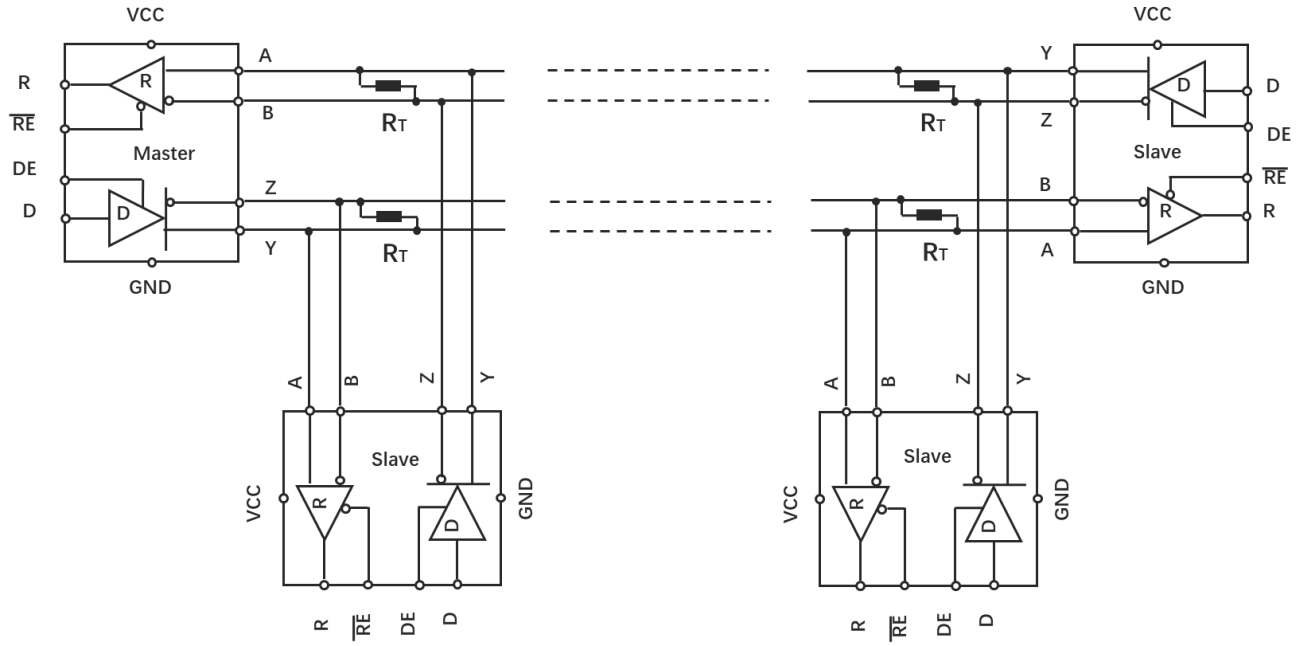


Figure 8. Typical RS485 communication network with enable function

The TPT482 and TPT480 (no DE, /RE pin) transceiver is designed for bidirectional RS485/422 data communications on multipoint bus transmission lines. Figures 8 shows typical network applications circuit to support up to 256 nodes. To minimize line reflections, terminate the line at both ends in its characteristic impedance, one 120ohm load in master side, and another 120ohm load in the end of slave side, and limit stub lengths off the main line as short as possible.

Layout

Layout Guideline

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in the width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This change in width upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, thus resulting in the reflection. Not all PCB traces can be straight, so they will have to turn corners. Figure 9 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

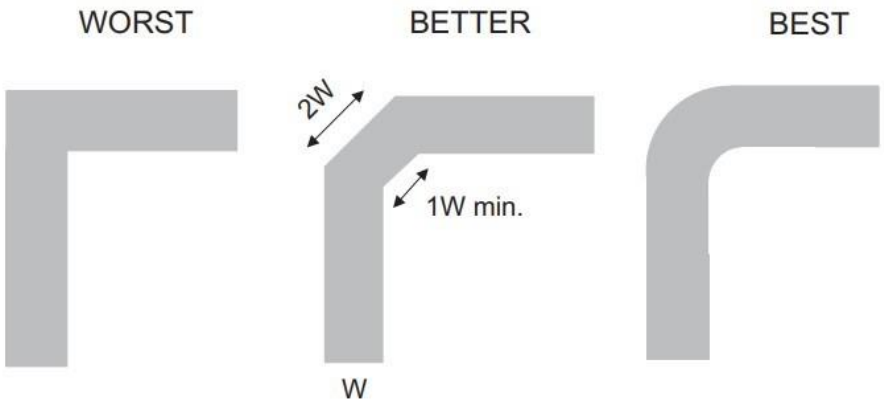
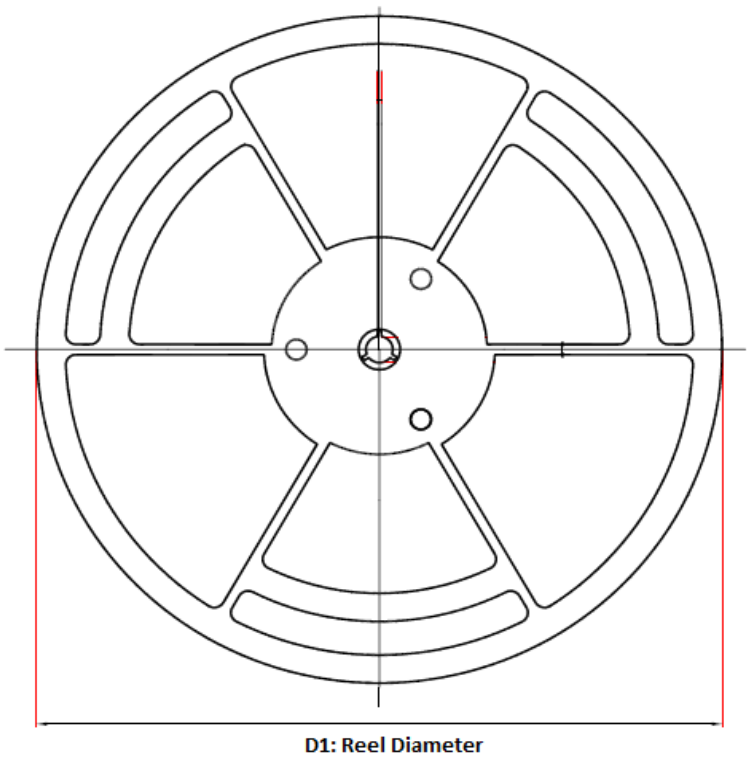


Figure 9. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Tape and Reel Information

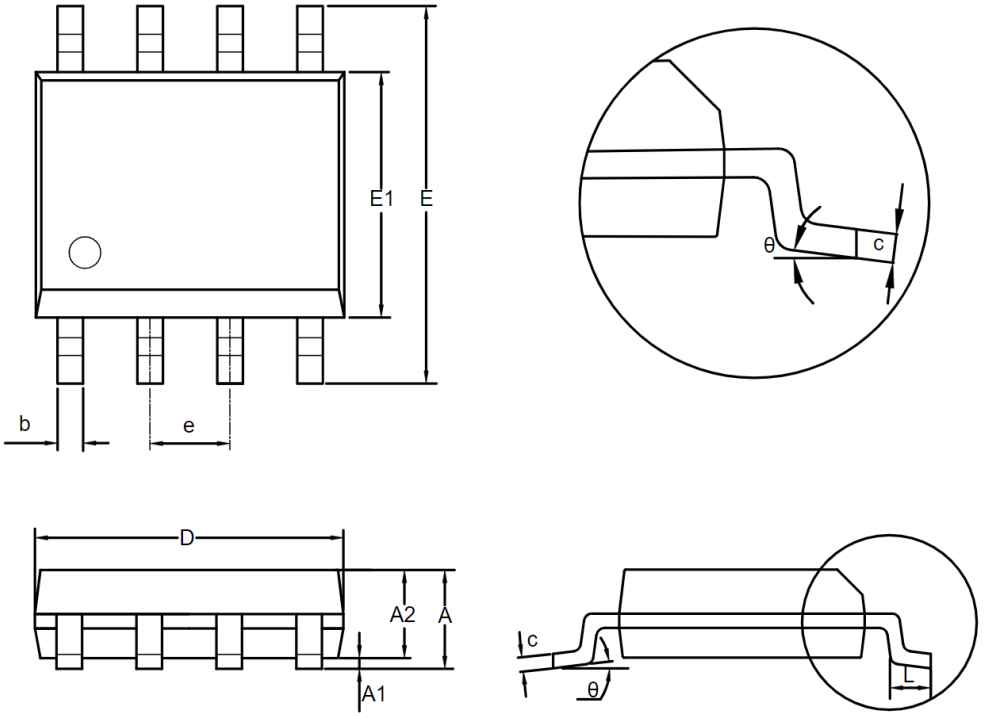


Order Number	Package	D1	A0	K0	W0	W1	B0	P0	Pin1 Quadrant
TPT480L1-SO1R	8-Pin SOP	330.0	6.5	2.0	12.0	17.6	5.4	8.0	Q1
TPT480-DF6R	DFN3X3-8L	330.0	3.3	1.1	12.0	17.6	3.3	8.0	Q1
TPT482-SO2R	14-Pin SOP	330.0	6.6	1.8	16.0	21.6	9.15	8.0	Q1
TPT482-VS2R	10-Pin MSOP	330.0	5.4	1.4	12.0	17.6	3.4	8.0	Q1

Package Outline Dimensions

SO1R (SOP-8)

Package Outline Dimensions SO1(SOP-8-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.550	0.049	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.000	0.016	0.039
θ	0	8°	0	8°

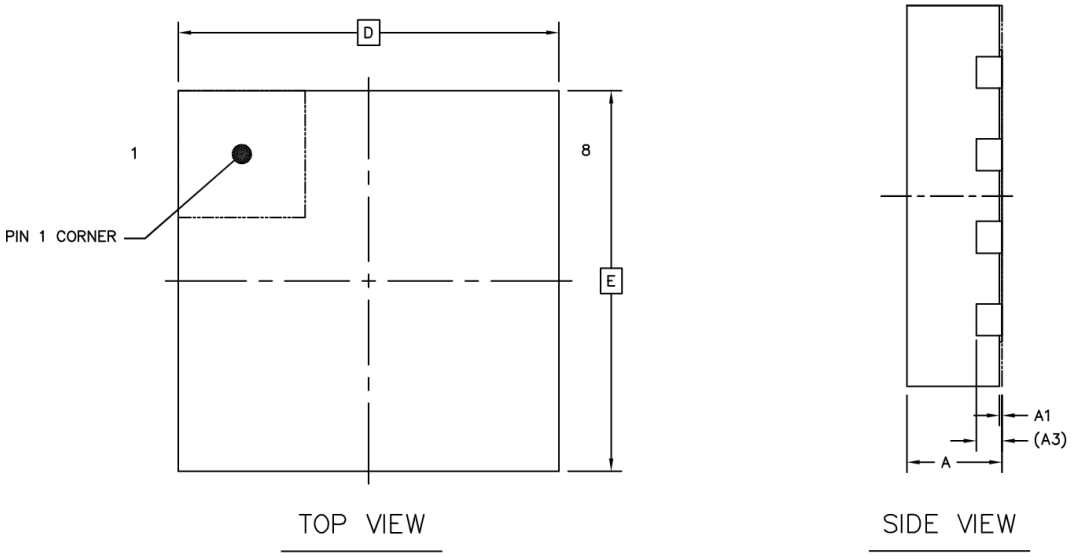
NOTES

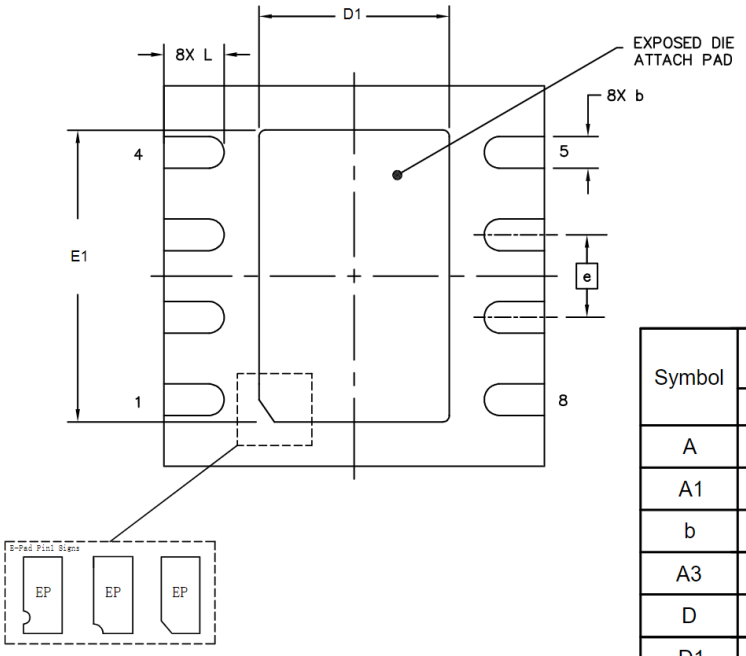
1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Package Outline Dimensions (Continued)

DF6R (DFN3x3-8L)

Package Outline Dimensions DF6(DFN3X3-8-B)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
b	0.250	0.350	0.010	0.014
A3	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D1	1.100	1.300	0.043	0.051
E	2.900	3.100	0.114	0.122
E1	2.050	2.250	0.081	0.089
e	0.650 BSC		0.026 BSC	
L	0.350	0.450	0.014	0.018

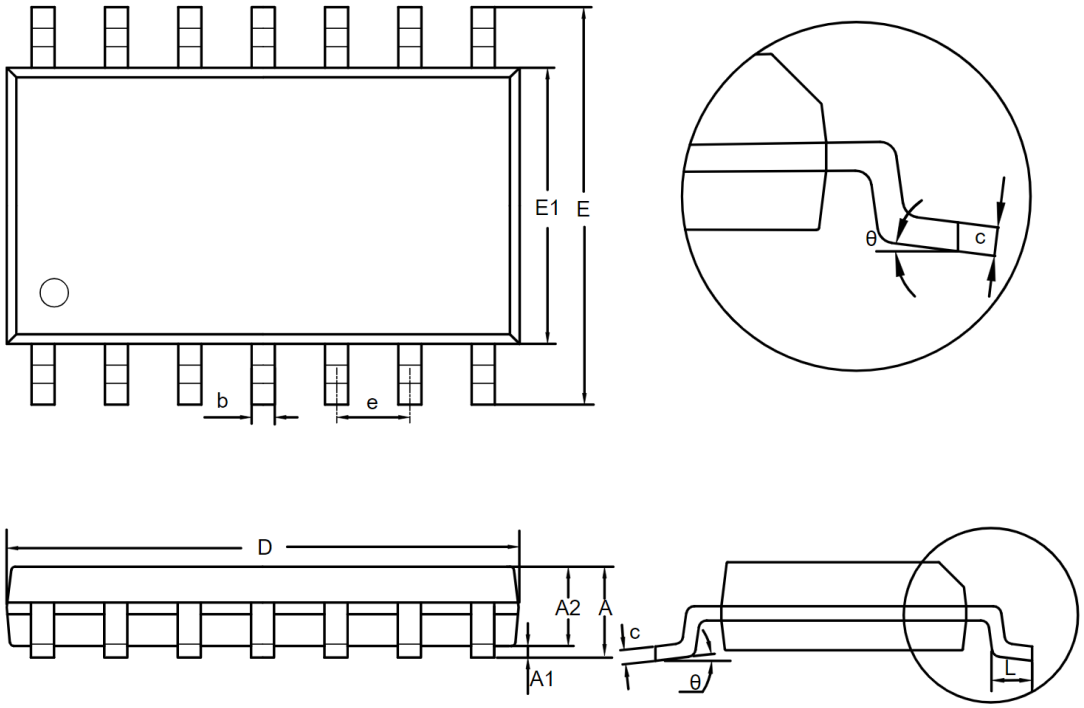
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.
3. The many types of E-pad Pin1 signs may appear in the product.

Package Outline Dimensions (Continued)

SO2R (SOP-14)

Package Outline Dimensions SO2(SOP-14-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.050	0.250	0.002	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0	8°	0	8°

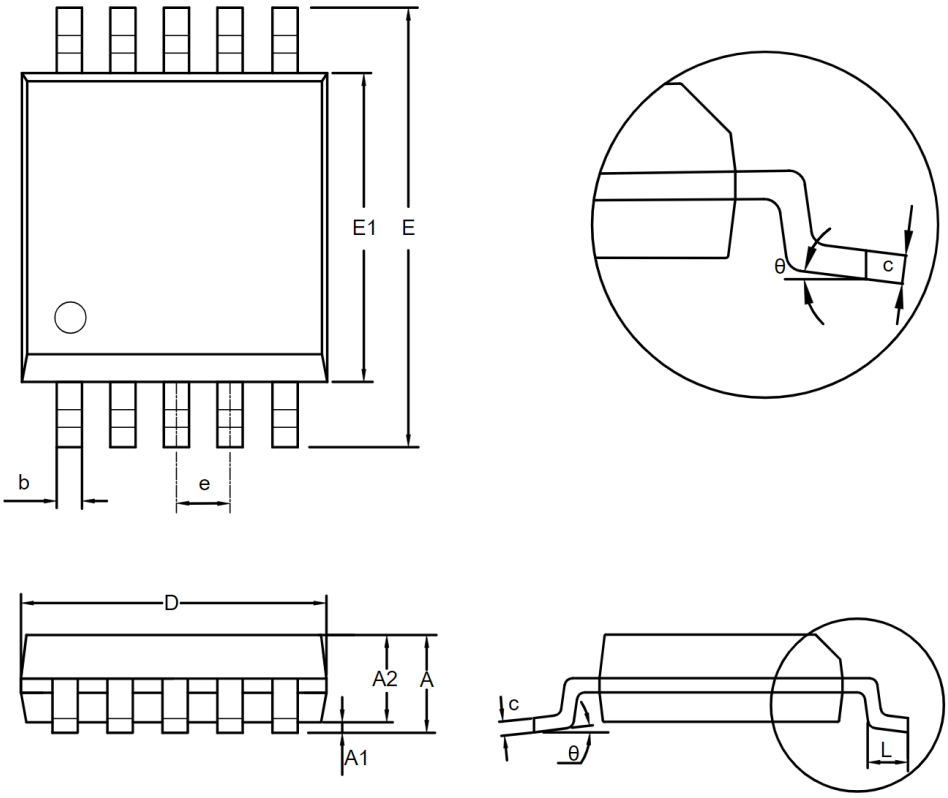
NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Package Outline Dimensions (Continued)

VS2R (MSOP-10)

Package Outline Dimensions VS2(MSOP-10-A)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	4.700	5.100	0.185	0.201
E1	2.900	3.100	0.114	0.122
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0	8°	0	8°

NOTES

1. Do not include mold flash or protrusion.
2. This drawing is subject to change without notice.

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT480L1-SO1R	-40 to 125°C	SOP8	T480	1	Tape and Reel, 4000	Green
TPT480-DF6R	-40 to 125°C	DFN3X3-8	T480	3	Tape and Reel, 4000	Green
TPT482-SO2R	-40 to 125°C	SOP14	T482	3	Tape and Reel, 2500	Green
TPT482-VS2R	-40 to 125°C	MSOP10	T482	3	Tape and Reel, 3000	Green

(1). Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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