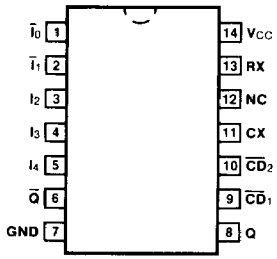
9600

RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

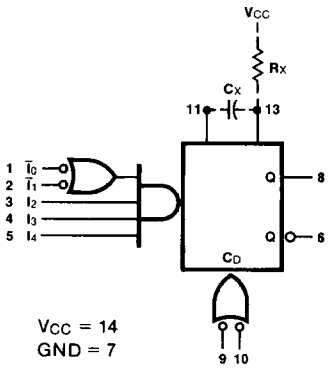
DESCRIPTION — The 9600 monostable, retriggerable, resettable multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9600 has excellent immunity to noise on the V_{CC} and ground lines. It uses TTL technology for high speed and high fan-out capability and is compatible with all members of the Fairchild TTL family.

- **74 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0% to 100% DUTY CYCLE**
- **RESETTABLE**
- **LEADING OR TRAILING-EDGE TRIGGERING**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



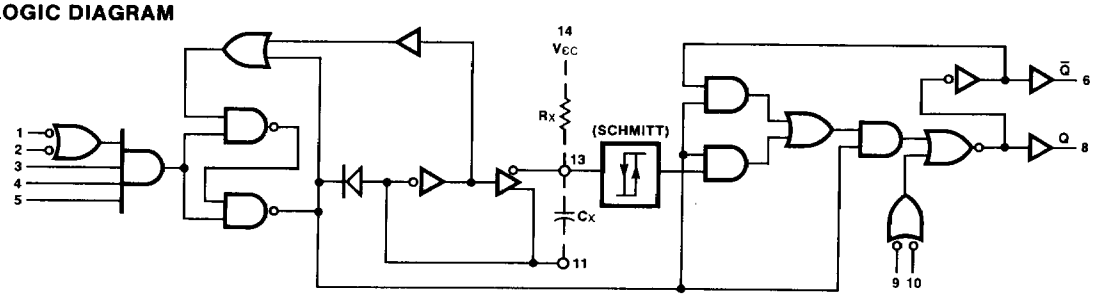
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +75°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9600PC		9A
Ceramic DIP (D)	A	9600DC	9600DM	6A
Flatpak (F)	A	9600FC	9600FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
$\overline{I}_0$, $\overline{I}_1$	Trigger Inputs (Active Falling Edge)	1.5/1.0
I_2 — I_4	Trigger Inputs (Active Rising Edge)	1.5/1.0
$\overline{C}_{D1}$ — $\overline{C}_{D2}$	Clear Inputs (Active LOW)	1.5/1.0
Q	Pulse Output	24/7.06 (6.2)
$\overline{Q}$	Complementary Pulse Output	24/7.06 (6.2)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 9600 monostable multivibrator has five inputs, three active HIGH and two active LOW. This allows leading-edge or trailing-edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9600 and result in a continuous true output (see Rule 8). Retriggering may be inhibited by tying the negation ($\overline{Q}$) output to an active LOW input. The output pulse may be terminated at any time by connecting either or both reset pins to a LOW logic level pin. Active pullups are provided on the outputs for good drive capability into capacitive loads.

Operating Notes

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the logic diagram. The value of R_X may vary from 5.0 kΩ to 50 kΩ for 0° C to +75° C operation and from 5.0 kΩ to 25 kΩ for -55° C to +125° C operation. C_X may vary from 0 to any necessary value available.
2. The following are recommended fixed values of R_X: R_X = 30 kΩ for 0° C to +75° C operation, R_X = 10 kΩ for -55° C to +125° C operation.
3. The output pulse width (t) is defined as follows:
   $t = 0.32\ R_X C_X (1 + 0.7/R_X)$ Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF. (see *Figure a*)
   The value of C_X may vary from 0 to any value necessary and obtainable. If however, C_X has leakage currents approaching 3.0 μA or if stray capacitance from either pin 11 or pin 13 to ground exceeds 50 pF, the timing equation may not represent the pulse width obtained.
4. If electrolytic type capacitors are to be used, the following three configurations are recommended.
   A. Use with low leakage electrolytic capacitors (see *Figure b*).
      The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 3.0 μA, and the inverse capacitor leakage at 1.0 V is less than 5.0 μA over the operational temperature range and Rule 3 above is satisfied.
   B. Use with high inverse leakage current electrolytic capacitors. (*Figure c*; this configuration is not recommended with retriggerable operation.)
      The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.
      $t \approx 0.3\ RC_X$
   C. Use to obtain extended pulse widths. (*Figure d*; this configuration is not recommended with retriggerable operation.)
      This configuration obtains extended pulse widths because of the larger timing resistor allowed by Beta multiplication. Electrolytics with high inverse leakage currents can be used. Q_1 is an npn silicon transistor such as 2N5961 or 2N5962, with h_{FE}, R and R_X related as in the inequality below.
      $R < R_X\ (0.7)\ (h_{FE}\ Q_1)$ or < 2.5 MΩ, whichever is less
      R_X (Min) < R_Y < R_X (Max) R_Y of 5.0 kΩ to 10 kΩ is recommended
      $t \approx 0.3\ RC_X$
5. This circuit is recommended to obtain variable pulse width by remote trimming *(Figure e)*.
6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules (see Triggering Truth Table *Figures f* and *g*).
   t_1, t_3 = Min. positive input pulse width > 40 ns.
   t_2, t_4 = Min. negative input pulse width > 40 ns.
8. The retrigger pulse width is equal to the pulse width t plus a delay time (see *Figure h*). For pulse widths greater than 500 ns, t_w can be approximated as t.
   $$t_w = t + t_{PLH} = 0.32\ R_X C_X\ (1 + 0.7/R_X) + t_{PLH}$$
9. Two overriding active LOW resets are provided (see *Figure i*). A LOW to either or both resets can terminate any timing cycle and/or inhibit any new cycle until both reset inputs are restored to a HIGH. Trigger inputs will not produce spikes in the output when either or both resets are held LOW.
10. Use of a 0.01 μF to 0.1 μF bypass capacitor located close to the 9600 is recommended.

TRIGGERING TRUTH TABLE*

INPUT PINS							RESPONSE
1	2	3	4	5	9	10	
X	X	X	X	X	L	X	No Trigger
↘	L	X	X	X	X	X	No Trigger
↘	X	L	X	X	X	X	No Trigger
↘	H	H	H	H	H	H	Trigger
H	H	↗	X	X	X	X	No Trigger
X	X	↗	L	X	X	X	No Trigger
L	X	↗	H	H	H	H	Trigger

*Pins 1 &2 are logically interchangeable, as are pins 3, 4, 5, and also 9 & 10.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

For $C_X \geq 10^3$ pF, $t = 0.32\ R_X C_X (1 + 0.7/R_X)$

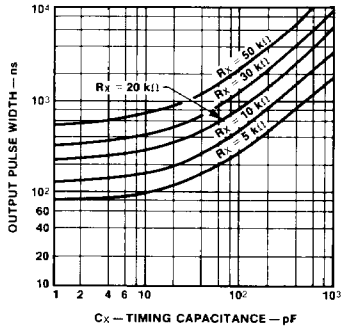


Fig. a

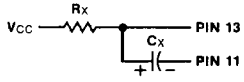


Fig. b

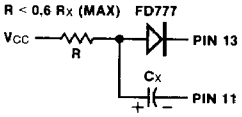


Fig. c

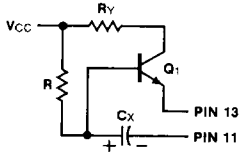


Fig. d

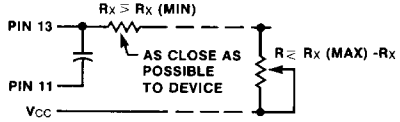


Fig. e Remote Trimming

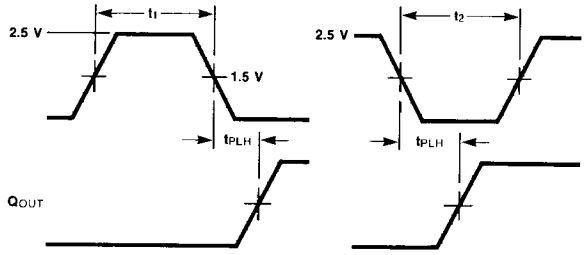


Fig. f Input on Pin 1 or 2

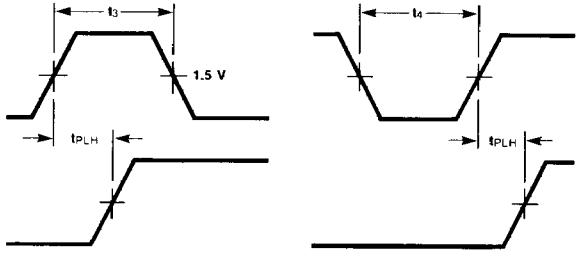


Fig. g Input on Pin 3, 4 or 5

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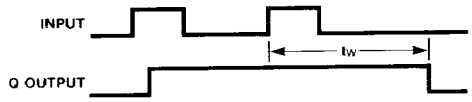


NOTE:
Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X ns after the initial trigger pulse (i.e., during the discharge cycle time).

Fig. h

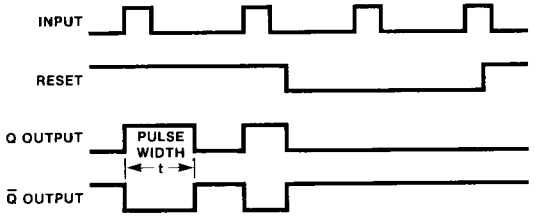
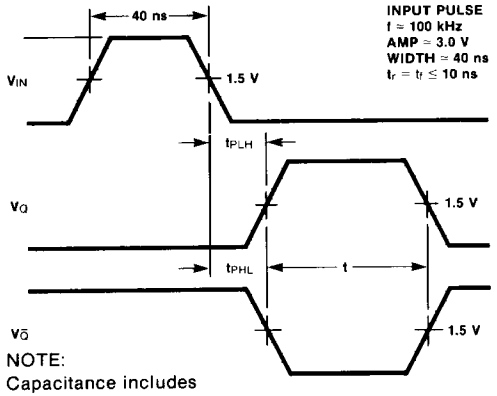


Fig. i



NOTE:
Capacitance includes Jig and Probe

Fig. j

NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

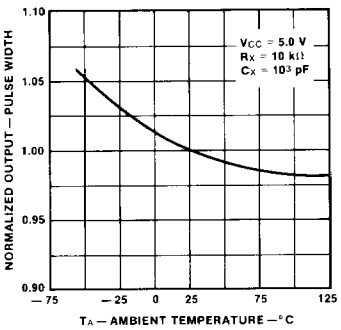


Fig. k

NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

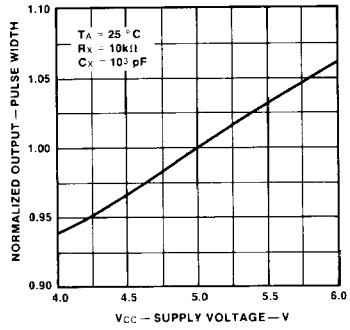


Fig. l

MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

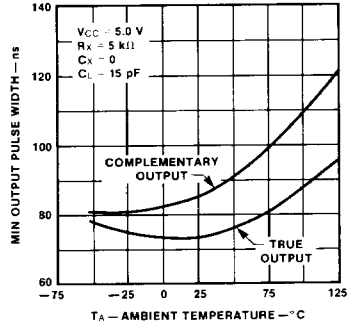


Fig. m

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96XX Min	96XX Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage	XM		0.4	V	I_{OL} = 9.92 mA* / I_{OL} = 11.3 mA; V_{CC} = Min
		XC		0.45		
V_{OL}	Output LOW Voltage	XM		0.4	V	I_{OL} = 12.8 mA, V_{CC} = Max
		XC		0.45		
V_{IH}	Input HIGH Voltage	XM	1.5		V	T_A = Max
		XC	1.65			
V_{IL}	Input LOW Voltage	XM		0.9	V	T_A = 25°C
		XC		0.85		
I_{IL}	Input LOW Current	XM		-1.6	mA	V_{IN} = 0.4 V / V_{IN} = 0.45 V; V_{CC} = Max
		XC		-1.6		
I_{OS}	Output Short Circuit Current	XM		-25	mA	V_{CC} = Max, V_{OUT} = 1.0 V* T_A = 25°C
		XC		-35		
I_{PD}	Quiescent Power Supply Drain	XM		24	mA	V_{CC} = 5.0 V, Pins 1, 2 = Gnd
		XC		26		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		96XX C_L = 15 pF Min	96XX C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay $\overline{I_n}$ to Q	XM		45	ns	R_X = 5.0 Ω, C_X = 0 pF Figs. 3-1, Fig. j
		XC		56		
t_{PHL}	Propagation Delay $\overline{I_n}$ to $\overline{Q}$	XM		40	ns	
		XC		47		
t_w (Min)	Minimum Q Pulse Width	XM		100	ns	R_X = 5.0 Ω, C_X = 0 pF
		XC		120		
t_w (Min)	Minimum $\overline{Q}$ Pulse Width	XM		112	ns	Fig. 3-1, Fig. j
		XC		130		
t_w	Pulse Width	XM	3.2	3.76	μs	R_X = 10 kΩ, C_X = 1000 pF Fig. 3-1, Fig. j
		XC	3.08	3.76		

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		96XX Min	96XX Max	UNITS	CONDITIONS
C_{STRAY}	Maximum Allowable Wiring Capacitance (Pin 13)			50	pF	Pin 13 to Gnd
R_X (Max)	Maximum Timing Resistor	XM	5.0	25	kΩ	Over Operating Temperature Range
		XC	5.0	50		

*Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{OS} Pin 8, open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{OS} Pin 6.

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