GLF71430 / GLF71431

7 A, VariRise™ Programmable Slew Rate Controlled Switch

Product Specification

DESCRIPTION

The GLF71430 / GLF71431 is an ultra-efficient, 7 A rated, integrated load switch with the VariRise™ technology which provides the programmable slew rate of variable output voltage rising times.

The GLF71430 / GLF71431 features the ultra-efficient I_QSmart™ technology that supports some of the lowest R_{ON}, quiescent currents (I_Q) and shutdown currents (I_{SD}) in the industry. Low R_{ON} reduces conduction losses, while low I_Q and I_{SD} solutions help designers to reduce parasitic leakage currents, improve system efficiency, and increase battery lifetimes.

The PGM input pin allows the user to add an external resistor to set the slew rate of the switch output voltage to a specific value for a given output capacitance. It limits inrush currents during turn-on, helping to minimize voltage droop.

The GLF71430 / GLF71431 offers best in class size and on-resistance (R_{ON}) performance. It uses chip scale packaging which utilizes 12 bumps, in a 1.27 mm x 1.67 mm die size with 0.4 mm pitch.

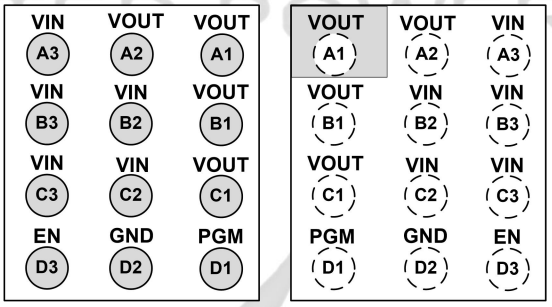
APPLICATIONS

- Low Power Subsystems
- Communication / Network System
- Smart Mobile Devices
- Storage Devices

FEATURES

- Supply Voltage Range: 1.5 V to 5.5 V
- Low R_{ON}: 10 mΩ Typ. at 5.5 V_{IN}
- VariRise™ Programmable V_{OUT} Rising Time
- 7 A Continuous Output Current
- Ultra-Low Quiescent Current
  - I_Q: 10 nA Typ. at 5.5 V_{IN}
- Ultra-Low Stand-by Current
  - I_{SD}: GLF71430, 10 nA Typ. at 5.5 V_{IN}
  - I_{SD}: GLF71431, 55 nA Typ. at 5.5 V_{IN}
- Output Discharge Switch: GLF71431
- Wide Operating Temperature Range:
  - 40 °C to 105 °C
- 1.27 mm x 1.67 mm x 0.55 mm Wafer Level Chip Scale Packaging (WLCSP)

PACKAGE



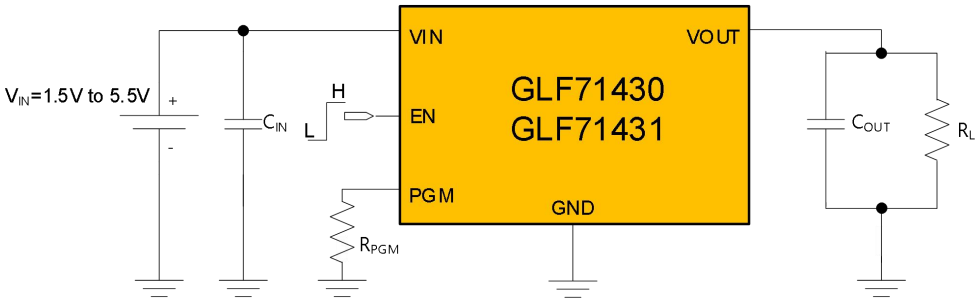
BOTTOM VIEW **TOP VIEW**

1.27 mm x 1.67 mm x 0.55 mm, 0.4 mm Pitch

ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V	Output Discharge	EN Activity	Package
GLF71430	DA	10 mΩ	NA	High	WLCSP
GLF71431	AI		85 Ω	High	WLCSP

APPLICATION DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

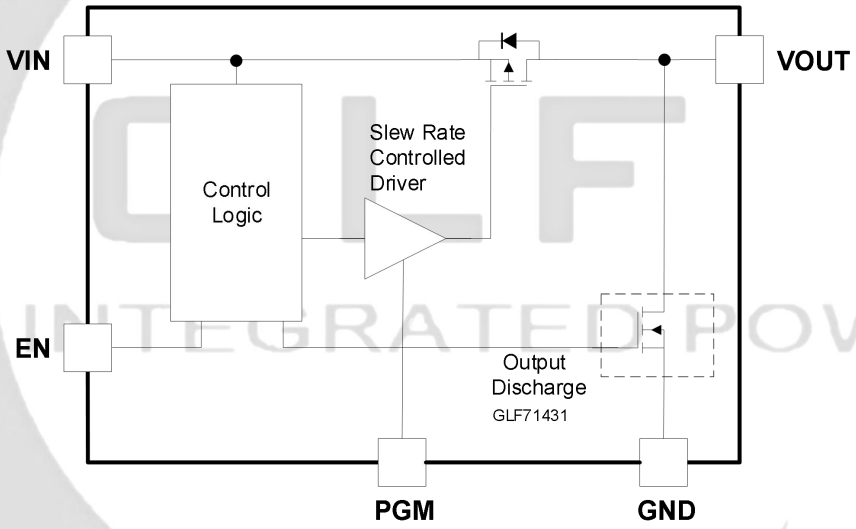
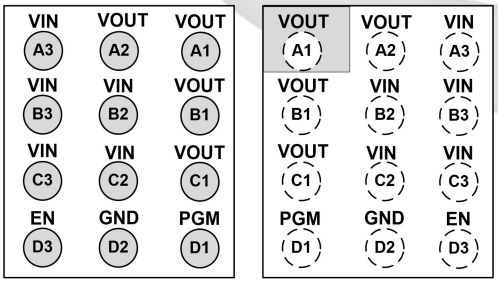


Figure 1. Functional Block Diagram

PIN CONFIGURATION



BOTTOM VIEW TOP VIEW

Figure 2. 1.27 mm x 1.67 mm x 0.55 mm WLCSP

PIN DEFINITION

Pin No.	Name	Description
A1, A2 B1, C1	VOUT	Switch Output
A3, B2, B3 C2, C3	VIN	Switch Input. Supply Voltage for IC
D1	PGM	Program pin to set the VOUT rising time with an external resistor.
D3	EN	Active high signal to enable the switch
D2	GND	Ground

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			7	A
P_D	Power Dissipation at T_A = 25°C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	105	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	+105	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 1.5 V to 5.5 V, typical values are at V_{IN} = 3.3 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Basic Operation						
V_{IN}	Supply Voltage		1.5		5.5	V
I_Q	Quiescent Current (1)	V_{IN} = V_{EN} = 5.5 V, I_{OUT}=0 mA,		10	50	nA
		V_{IN} = V_{EN} = 5.5 V, I_{OUT}=0 mA, T_A =85 °C (4)		25		
		V_{IN} = V_{EN} = 5.5 V, I_{OUT}=0 mA, T_A =105 °C (4)		92		
I_{SD}	Shutdown Current GLF71430	EN = GND, I_{OUT}=0 mA, V_{IN}=1.5 V		4		nA
		EN = GND, I_{OUT}=0 mA, V_{IN}=2.5 V		5		
		EN = GND, I_{OUT}=0 mA, V_{IN}=3.3 V		6		
		EN = GND, I_{OUT}=0 mA, V_{IN}=4.5 V		7		
		EN = GND, I_{OUT}=0 mA, V_{IN}=5.5 V		10	60	
		EN = GND, I_{OUT}=0 mA, V_{IN}=5.5 V, T_A = 85 °C (4)		45		
		EN = GND, I_{OUT}=0 mA, V_{IN}=5.5 V, T_A = 105 °C (4)		170		
	Shutdown Current GLF71431	EN = GND, I_{OUT}=0 mA, V_{IN}=1.5 V		7		nA
		EN = GND, I_{OUT}=0 mA, V_{IN}=2.5 V		10		
		EN = GND, I_{OUT}=0 mA, V_{IN}=3.3 V		12		
		EN = GND, I_{OUT}=0 mA, V_{IN}=4.5 V		25		
		EN = GND, I_{OUT}=0 mA, V_{IN}=5.5 V		55	80	
		EN = GND, I_{OUT}=0 mA, V_{IN}=5.5 V, T_A = 85 °C (4)		1.6		µA
		EN = GND, I_{OUT}=0 mA, V_{IN}=5.5 V, T_A = 105 °C (4)		4.6		

R_{ON}	On-Resistance	V_{IN}=5.5 V I_{OUT}= 500 mA	T_A = 25 °C		10	13	mΩ
			T_A = 85 °C (4)		12		
			T_A = 105 °C (4)		13		
		V_{IN}=3.3 V, I_{OUT}= 500 mA	T_A = 25 °C		13	16	
			T_A = 85 °C (4)		15		
			T_A = 105 °C (4)		16		
		V_{IN}=2.5 V, I_{OUT}= 300 mA	T_A =25 °C		15		mΩ
		V_{IN}=1.8 V, I_{OUT}= 300 mA	T_A =25 °C		20		
		V_{IN}=1.5 V, I_{OUT}= 100 mA	T_A =25 °C		25		
R_{DSC}	Output Discharge Resistance (2)	V_{EN} < V_{IL}, I_{FORCE}= 10 mA, GLF71431			85		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.5 V to 1.8 V		0.9			V
		V_{IN}=1.8 V to 5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.5 V to 1.8 V				0.3	V
		V_{IN}=1.8 V to 5.5 V				0.4	V
R_{EN}	EN pull down resistance	V_{EN}=5.5 V V_{EN}=V_{IN}		7	10.8	13	MΩ
Switching Characteristics (2,3)							
t_{dON}	Turn-On Delay	R_{OUT}=150 Ω, C_{OUT}=1.0 µF, R_{PGM} = 100 kΩ			2		ms
t_R	V_{OUT} Rise Time				5		
t_{dON}	Turn-On Delay	R_{OUT}=150 Ω, C_{OUT}=1.0 µF, R_{PGM} = 1 MΩ			7		
t_R	V_{OUT} Rise Time				27		
t_{dOFF}	Turn-Off Delay (4)	R_{OUT}=150 Ω, C_{OUT}=1.0 µF, GLF71430			20		µs
t_F	V_{OUT} Fall Time (4)				345		
t_{dOFF}	Turn-Off Delay (4)	R_{OUT}=150 Ω, C_{OUT}=1.0 µF, GLF71431			10		
t_F	V_{OUT} Fall Time (4)				110		

Notes:
1. I_Q does not include Enable pull down current through the pull-down resistor R_{EN}.
2. Output discharge path is enabled during off.
3. t_{ON} = t_{dON} + t_R , t_{OFF} = t_{dOFF} + t_F
4. By design; characterized, not production tested

TIMING DIAGRAM

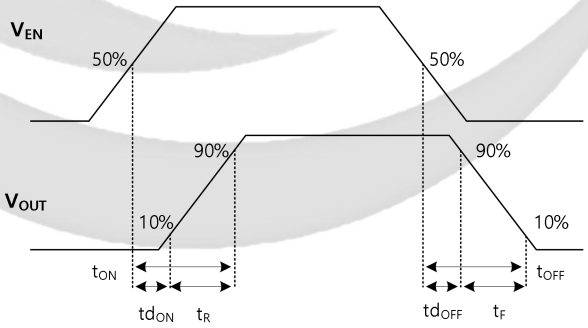


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

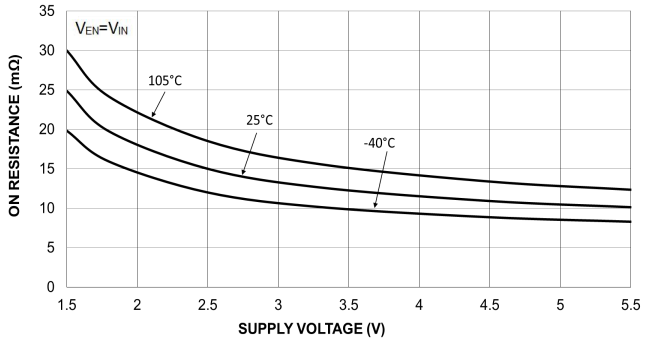


Figure 4. On-Resistance vs. Supply Voltage

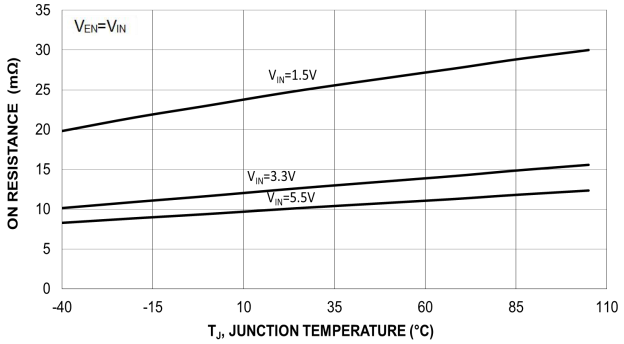


Figure 5. On-Resistance vs. Temperature

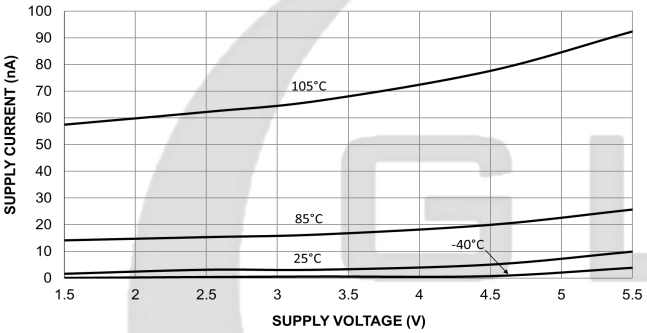


Figure 6. Quiescent Current vs. Supply Voltage

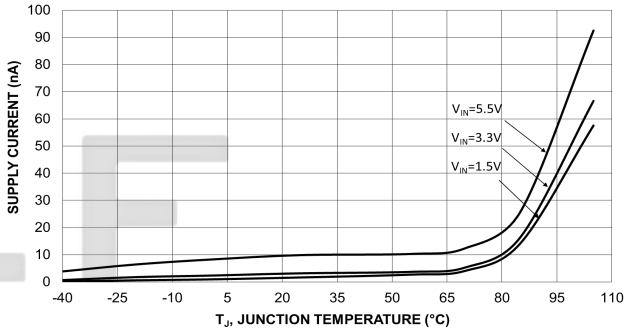


Figure 7. Quiescent Current vs. Temperature

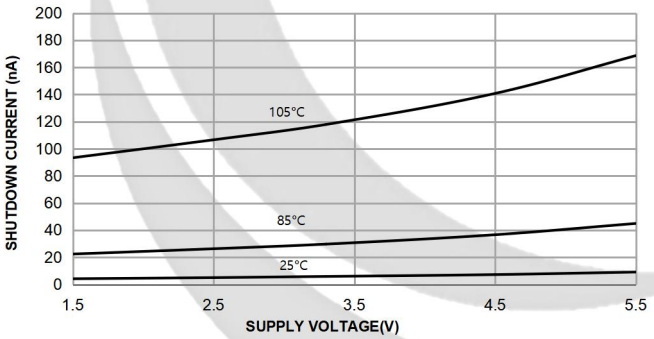


Figure 8. Shutdown Current vs. Supply Voltage, GLF71430

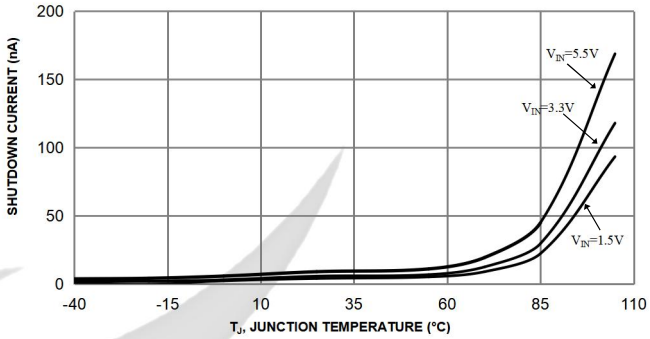


Figure 9. Shutdown Current vs. Temperature, GLF71430

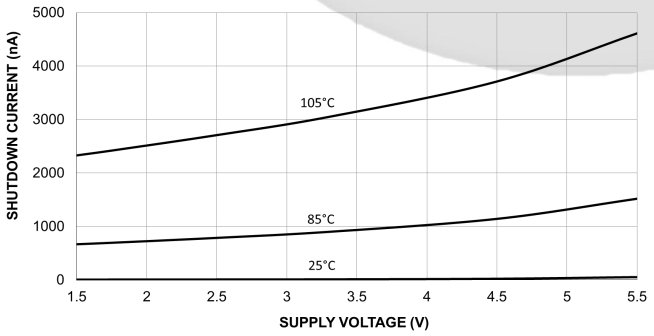


Figure 10. Shutdown Current vs. Supply Voltage, GLF71431

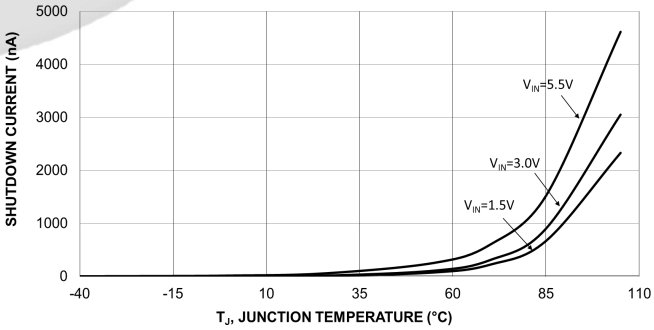


Figure 11. Shutdown Current vs. Temperature, GLF71431

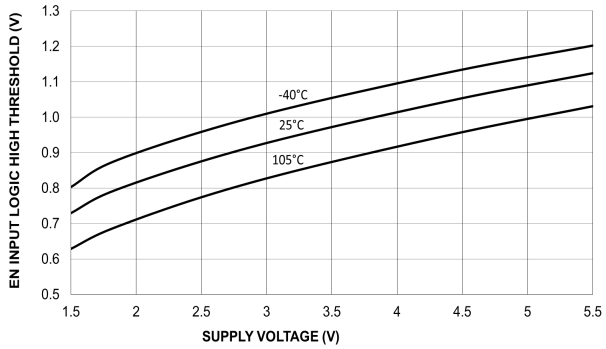


Figure 12. EN Input Logic High Threshold

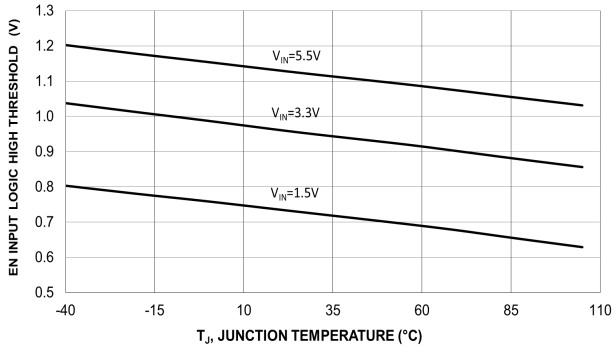


Figure 13. EN Input Logic High Threshold vs. Temperature

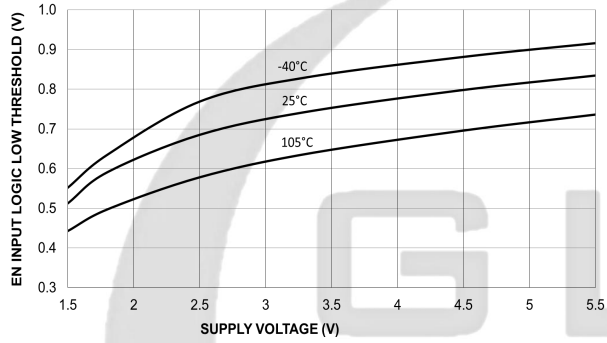


Figure 14. EN Input Logic Low Threshold

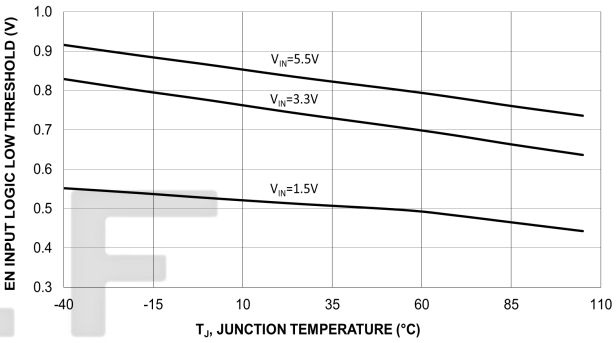


Figure 15. EN Input Logic Low Threshold vs. Temperature

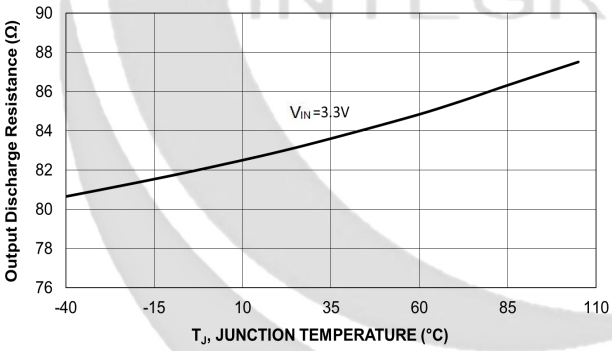


Figure 16. Output Discharge Resistance vs. Temperature

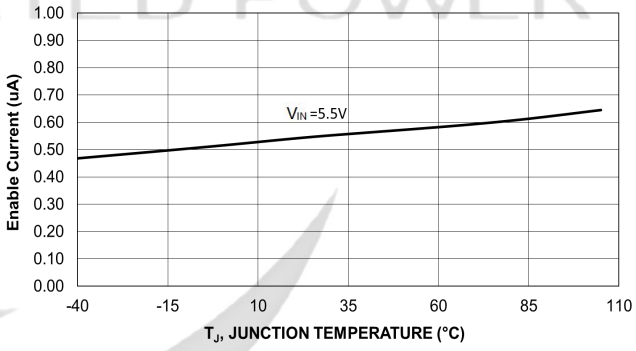


Figure 17. Enable Pulldown Current vs. Temperature

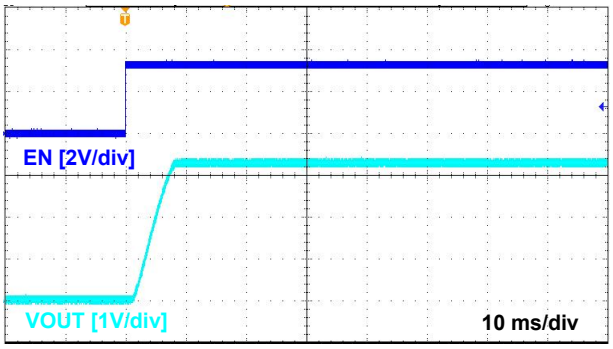


Figure 22. Turn-On Response, GLF71430 V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=100 kΩ, R_L=150 Ω

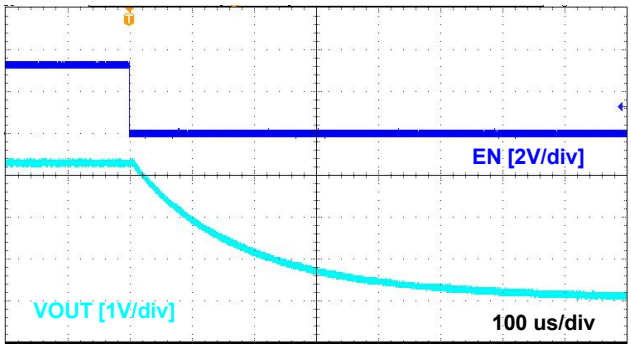


Figure 23. Turn-Off Response, GLF71430 V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=100 kΩ, R_L=150 Ω

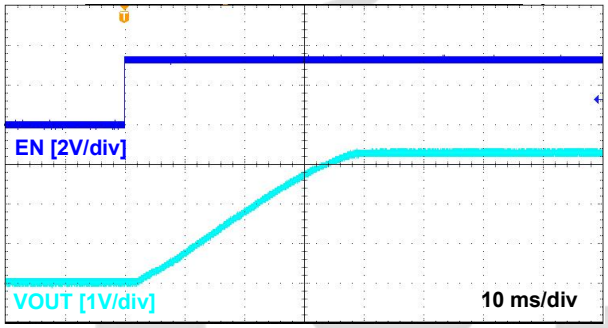


Figure 24. Turn-On Response, GLF71430 V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=1 MΩ, R_L=150 Ω

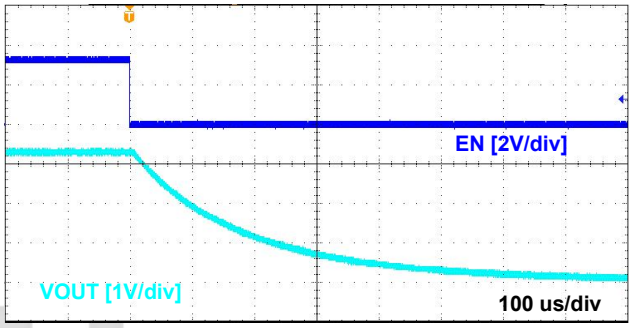


Figure 25. Turn-Off Response,GLF71430, V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=1 MΩ, R_L=150 Ω

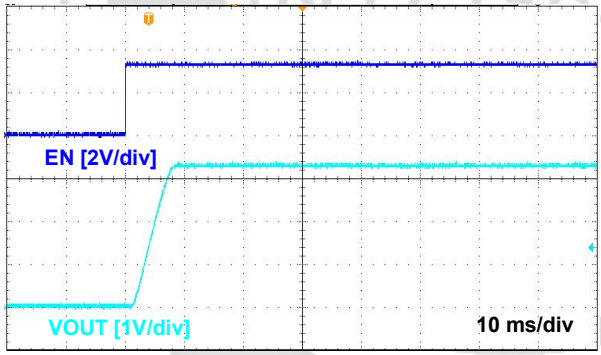


Figure 18. Turn-On Response, GLF71431 V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=100 kΩ, R_L=150 Ω

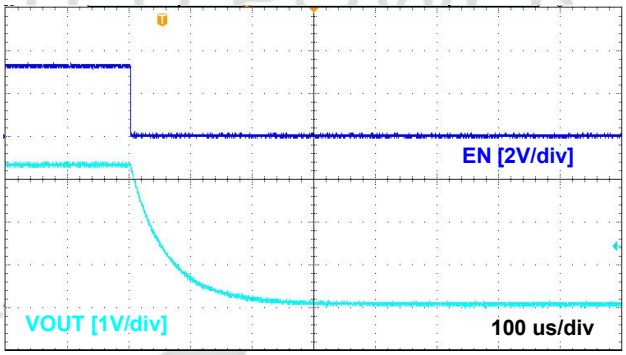


Figure 19. Turn-Off Response, GLF71431 V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=100 kΩ, R_L=150 Ω

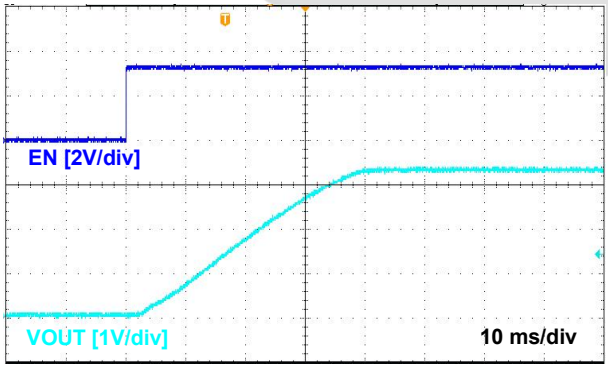


Figure 20. Turn-On Response, GLF71431 V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=1 MΩ, R_L=150 Ω

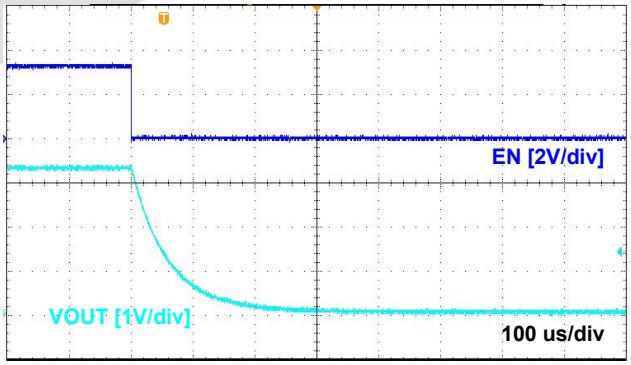


Figure 21. Turn-Off Response,GLF71431 V_{IN}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_{PGM}=1 MΩ, R_L=150 Ω

APPLICATION INFORMATION

The GLF71430 / GLF71431 is a 7 A fully integrated load switch with the VariRise™ programmable slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.5 V to 5.5 V with very low on-resistance to reduce conduction loss. At off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power supply. The package is a 1.27 mm x 1.67 mm wafer level chip scale package, saving space in compact applications. It is constructed using 12 bumps, with a 0.4 mm pitch for manufacturability.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to mitigate voltage undershoot on the output pin the moment when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

EN pin

The GLF71430 / GLF71431 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.

Output Discharge Function

When the EN signal of the GLF71431 turns into an off state, the N-channel switch turns on to discharge an output capacitor quickly.

VariRise™ Programmable Slew Rate

An external resistor between the PGM and GND pin sets the output voltage slew rate. The R_{PGM} pin is not recommended to be open. The table 1 can also be used to choose R_{PGM} value quickly.

R_{PGM} [kΩ]	5.0 V_{IN}		3.3 V_{IN}		2.5 V_{IN}		1.8 V_{IN}		1.5 V_{IN}	
	t_R [ms]	t_{dON} [ms]	t_R [ms]	t_{dON} [ms]	t_R [ms]	t_{dON} [ms]	t_R [ms]	t_{dON} [ms]	t_R [ms]	t_{dON} [ms]
20	1.37	0.68	1.19	0.69	0.98	0.73	0.79	0.71	0.57	0.64
33	2.13	1.10	1.90	1.06	1.56	1.09	1.22	1.04	0.89	0.91
51	3.22	1.30	2.71	1.50	2.25	1.51	1.78	1.42	1.32	1.24
82	4.91	1.98	4.20	2.11	3.44	2.12	2.64	1.95	1.95	1.70
100	5.93	2.36	5.02	2.40	4.01	2.39	3.14	2.27	2.27	1.92
150	8.36	3.15	7.09	3.17	5.77	3.01	4.47	2.85	2.97	2.47
220	11.69	3.89	10.00	3.89	7.99	3.74	6.11	3.46	4.13	3.09
300	14.88	4.56	12.69	4.56	10.21	4.29	7.53	3.97	5.34	3.52
390	18.57	5.25	15.56	5.16	12.46	4.73	9.22	4.35	6.46	3.88
510	22.45	5.92	18.95	5.78	15.20	5.19	11.35	4.71	7.71	4.22
680	27.20	6.67	22.91	6.44	18.60	5.66	13.39	5.07	8.92	4.55
1000	34.11	7.57	27.84	7.36	22.44	6.31	16.00	5.71	11.50	4.81

Note. Condition: C_{IN}=0.1 μF, C_{OUT}=0.1 μF, R_L=10 Ω, Rise Time from 10 % to 90 % of VOUT

Table 1. V_{OUT} Rise Time (ms) vs. R_{PGM}

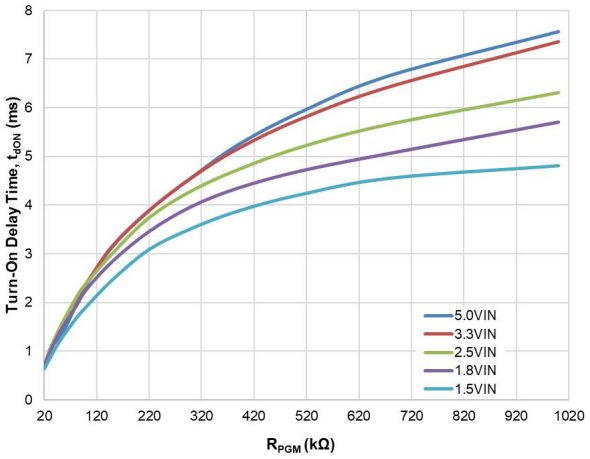


Figure 26. Turn-On Delay Time vs. R_{PGM}

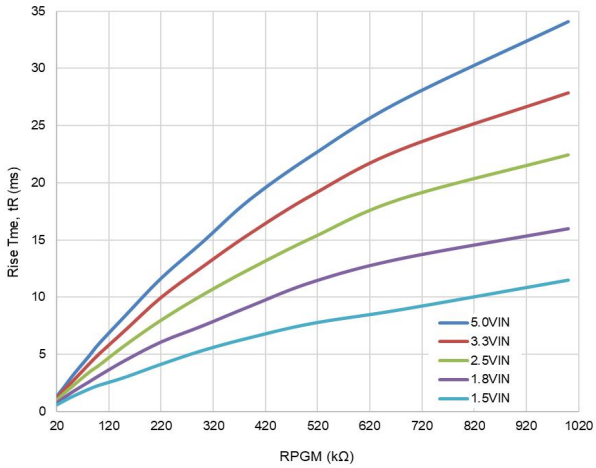
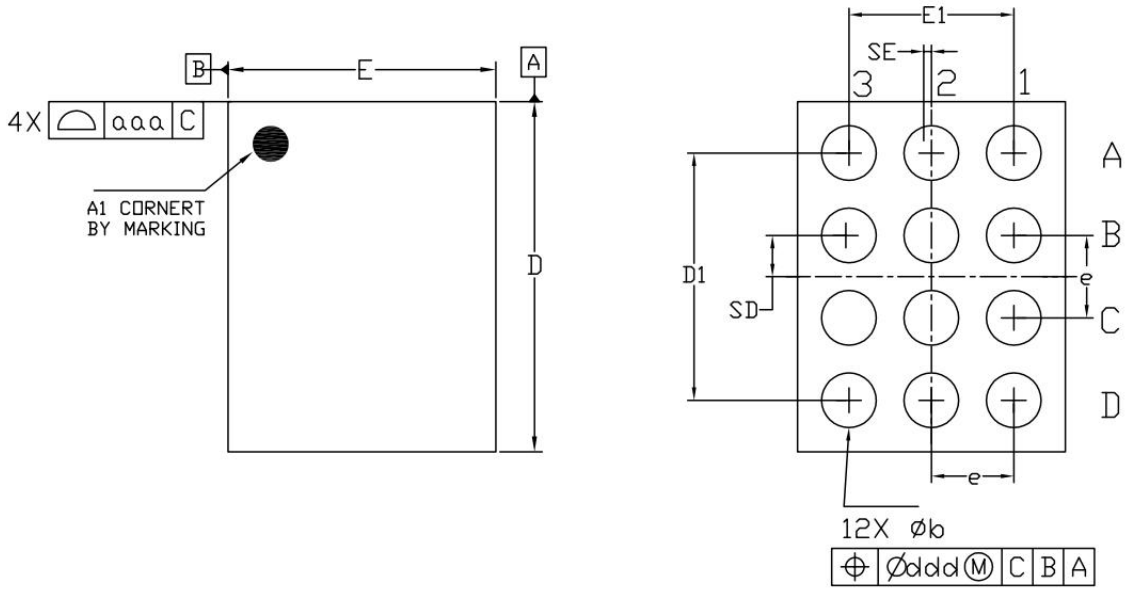


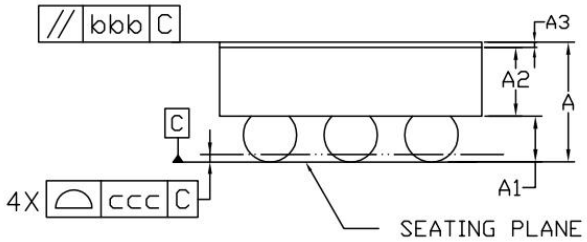
Figure 27. V_{OUT} Rise Time vs. R_{PGM}

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will be better to reduce parasitic effects at dynamic operations and improve thermal performance at high load current.

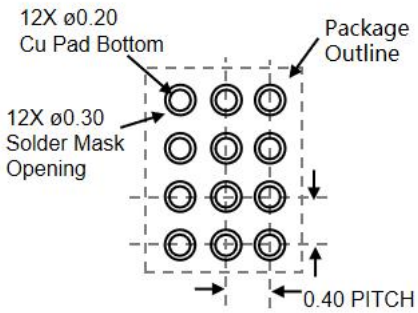
PACKAGE OUTLINE





Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.175	0.200	0.225
A2	0.300	0.325	0.350
A3	0.020	0.025	0.030
D	1.655	1.670	1.685
E	1.255	1.270	1.285
D1	1.150	1.200	1.250
E1	0.750	0.800	0.850
b	0.215	0.265	0.315
e	0.400 BSC		
SD	0.200 BSC		
SE	0.000 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint

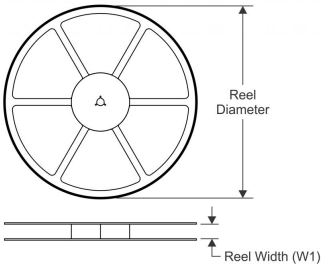


Notes

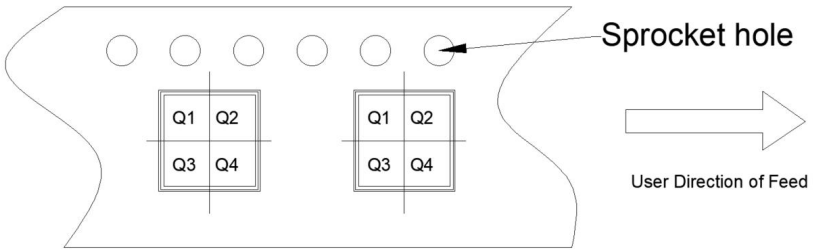
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

TAPE AND REEL INFORMATION

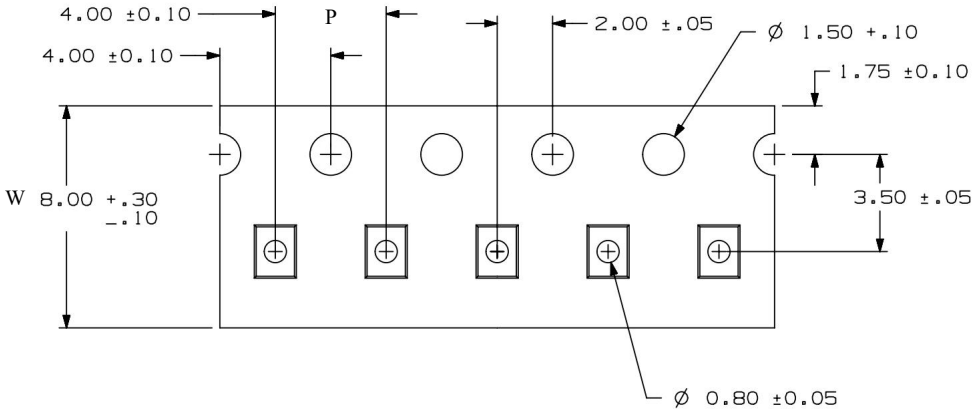
REEL DIMENSIONS

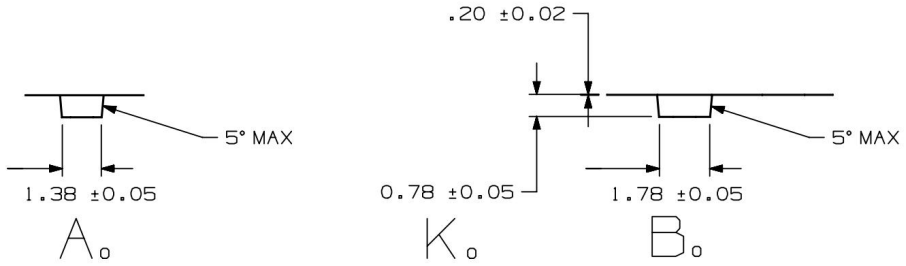


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71430	WLCSP	12	3000	180	9	1.38	1.78	0.78	4	8	Q1
GLF71431	WLCSP	12	3000	180	9	1.38	1.78	0.78	4	8	Q1

Notes:
A0: Dimension designed to accommodate the component width
B0: Dimension designed to accommodate the component length
C0: Dimension designed to accommodate the component thickness
W: Overall width of the carrier tape
P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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