HDL6M05543

QUAD ±100V 2A TRUE 5-LEVEL ULTRASOUND PULSER

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Rev.2.2_00

The ABLIC Inc. HDL6M05543 is a quad, true 5-level RTZ, high-voltage, high-speed ultrasound pulser.
The HDL6M05543 comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

Functions

- Quad true 5-level pulser with active T/R switch with 3-input per channel

Features

- 0 to ±100V output voltage
- ±2A source and sink peak current for the 1st high-voltage (HV) pulses ($V_{PP}1/V_{NN}1$)
- ±2A source and sink peak current with ±1A active clamp for the 2nd HV pulses ($V_{PP}2/V_{NN}2$)
- ±2A source and sink peak current for active ground clamp
- 250Ω (±0.1A) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock with 2-bit edge control (transparent mode available)
- 10Ω active T/R switch with 2-bit turn-on timing control
- 20MHz output frequency @±60V output, 220pF load
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each HV output
- 4-mode output current control for the 2nd HV rail
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 64-lead 9x9mm QFN package (RoHS compliant)

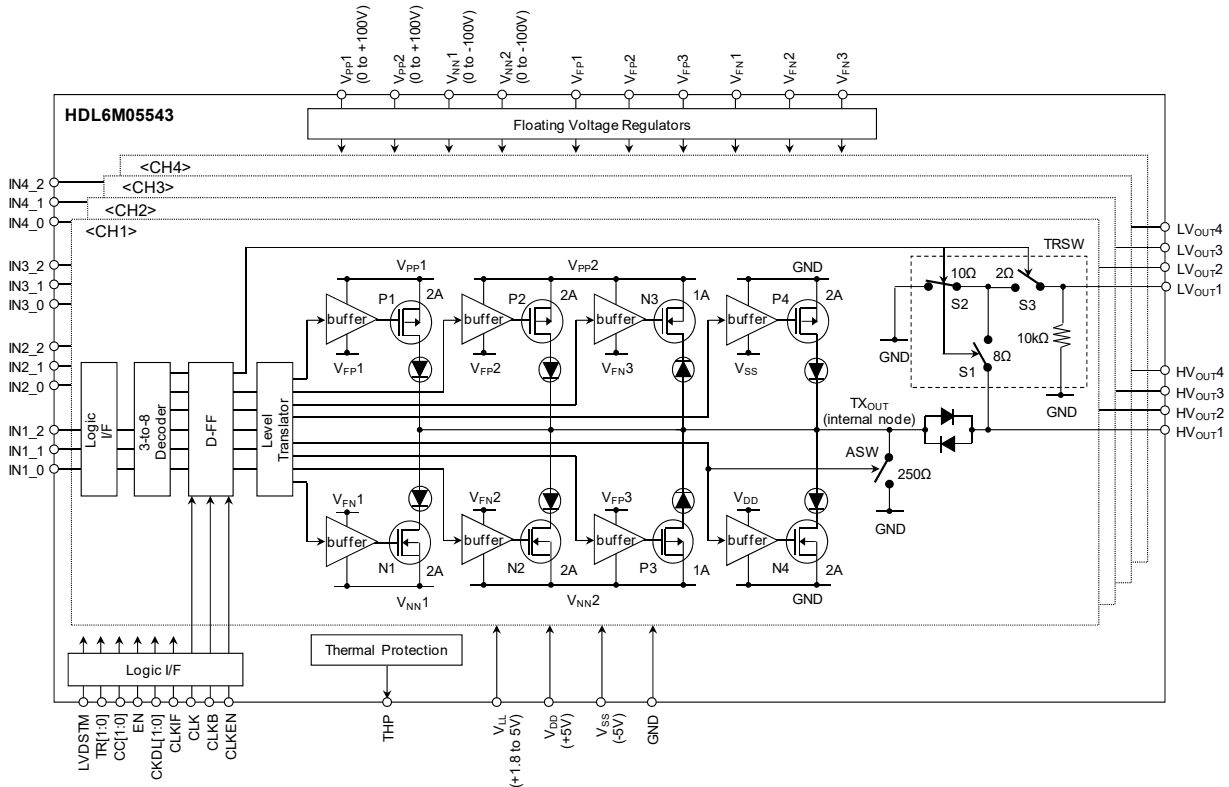


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Negative supply voltage	V_{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	$V_{PP}1$, $V_{PP}2$	-0.5 to +105	V	
5	Negative high-voltage supplies	$V_{NN}1$, $V_{NN}2$	-105 to +0.5	V	
6	Positive high-voltage difference	($V_{PP}1$-$V_{PP}2$)	-105 to +105	V	
7	Negative high-voltage difference	($V_{NN}1$-$V_{NN}2$)	-105 to +105	V	
8	High-voltage outputs (x=1~4)	$HV_{OUT}x$	-105 to +105	V	
9	Low-voltage outputs (x=1~4)	$LV_{OUT}x$	-1 to +1	V	
10	THP (Thermal Protection) output	THP	-0.4 to +7	V	
11	All Logic input voltages (x=1~4)	INx_[2:0], EN, CLKEN, CLK, CLKB, CLKIF, CKDL[1:0], CC[1:0], TR[1:0], LVDSTM	-0.4 to +7	V	
12	Operating junction temperature	T_{Jop}	-20 to +150	°C	
13	Operating free-air Temperature	T_A	0 to +75	°C	
14	Storage temperature	T_{STG}	-55 to +150	°C	
15	Maximum power dissipation	P_{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Power sequencing

2.1 Operating Supply Voltages

Table 2 Operating Supply Voltages

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	2.4	2.5 to 3.3	3.6	V	Clock mode
			1.7	1.8 to 5	V_{DD}	V	Transparent mode
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V_{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	$V_{PP}1$, $V_{PP}2$	0	-	100	V	
5	Negative high-voltage supplies	$V_{NN}1$, $V_{NN}2$	-100	-	0	V	
6	Positive high-voltage difference	($V_{PP}1$-$V_{PP}2$)	-100	-	100	V	
7	Negative high-voltage difference	($V_{NN}1$-$V_{NN}2$)	-100	-	100	V	
8	IC substrate voltage *	V_{SUB}	-	0	-	V	
9	$V_{PP}x$, $V_{NN}x$ slew rate (x=1,2)	SR_{MAX}	-	-	25	V/ms	

NOTE: * The package exposed pad internally connected to the IC substrate must be soldered to the ground.

2.2 Logic Inputs

Clock (CLK) mode synchronizes data inputs INx_[2:0] (x=1~4) with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. INx_[2:0] are decoded, clocked, level-translated, then sent to high-voltage output stage.

Differential clock input has two modes as shown below.

- LVDS CLK mode: set CLKIF=0. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: set CLKIF=1. See Table 3 for all the logic inputs.

TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. INx_[2:0] are decoded, level-translated, then sent to high-voltage output stage. See Table 3 for all the logic inputs.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition	
1	High-level logic input voltage	V_{IH}	$0.8V_{LL}$	-	V_{LL}	V		
2	Low-level logic input voltage	V_{IL}	0	-	$0.2V_{LL}$	V		
3	Logic input capacitance	C_{IN}	-	3	-	pF		
4	Logic input high current *1	I_{IH}	-10	-	10	μA		
5	Logic input low current *2	I_{IL}	-10	-	10	μA		
6	Input rise/fall time	t_r, t_f	-	-	800	ps	CLK≥100MHz	CMOS CLK mode 10~90% CLK, CLKB, INx_[2:0]
			-	-	2.0	ns	CLK<100MHz	
7	Input clock frequency	f_{CLK}	-	-	200	MHz	CMOS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T, See Fig.3	
8	Duty cycle	D_{CLK}	40	50	60	%		
9	Data Setup time	t_{SU}	1.4	-	-	ns	CLK mode, CKDL[1:0]='00' INx_[2:0] to CLK/CLKB, See Fig.3	
10	Data Hold time	t_{HLD}	1.4	-	-	ns		

NOTE:

*1) TR[1:0], CKDL[1:0], and LVDSTM have 50μA leak at V_{LL}=2.5V due to 50kΩ internal pull-down resistor.

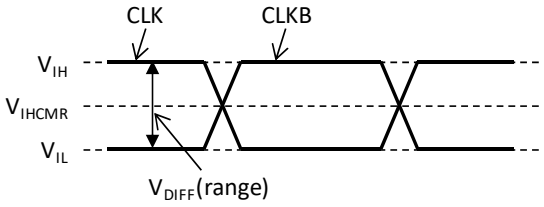
*2) EN, CC[1:0], CLKEN, and CLKIF have 50μA leak at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V_{IH}	1.265	-	-	V	V_{IHCMR}(Typ)+V_{DIFF}(Min)/2
2	Low-level input voltage	V_{IL}	-	-	1.135	V	V_{IHCMR}(Typ)-V_{DIFF}(Min)/2
3	Differential input voltage range	$V_{DIFF(range)}$	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	$V_{DIFF(p-p)}$	0.26	0.7	0.98	V_{pp}	|CLK-CLKB| differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V_{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R_{IN}	85	100	115	Ω	LVDSTM=1
7	High-level input current	I_{IH}	-	-	5.8	mA	
8	Low-level input current	I_{IL}	-	-	5.8	mA	
9	Input rise/fall time	t_r, t_f	-	-	600	ps	20% to 80% of V_{DIFF}
10	Input clock frequency	f_{CLK}	-	-	200	MHz	LVDS CLK mode, CLK, CLKB, f_{CLK}=1/T, D_{CLK}=τ/T, See Fig.3
11	Duty cycle	D_{CLK}	40	50	60	%	

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range (V_{DIFF}(range))



Differential input voltage peak to peak swing (V_{DIFF}(p-p))

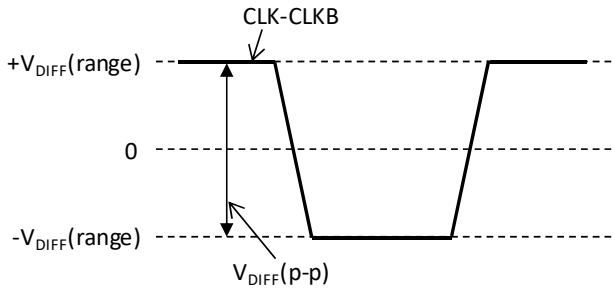


Fig.2 LVDS clock inputs

LVDS/CMOS CLK mode (CLKEN=0)

TP mode (CLKEN=1)

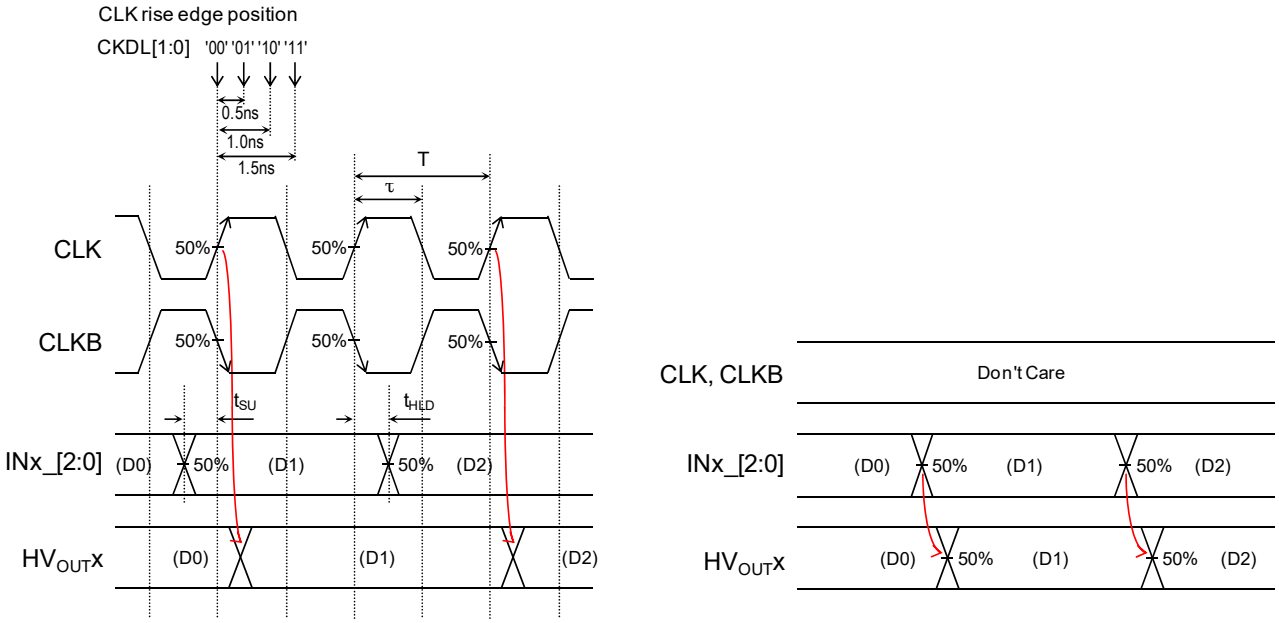


Fig.3 Setup/Hold Time

2.3 Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.

When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outpus will be enabled.

3. Typical Application Circuit

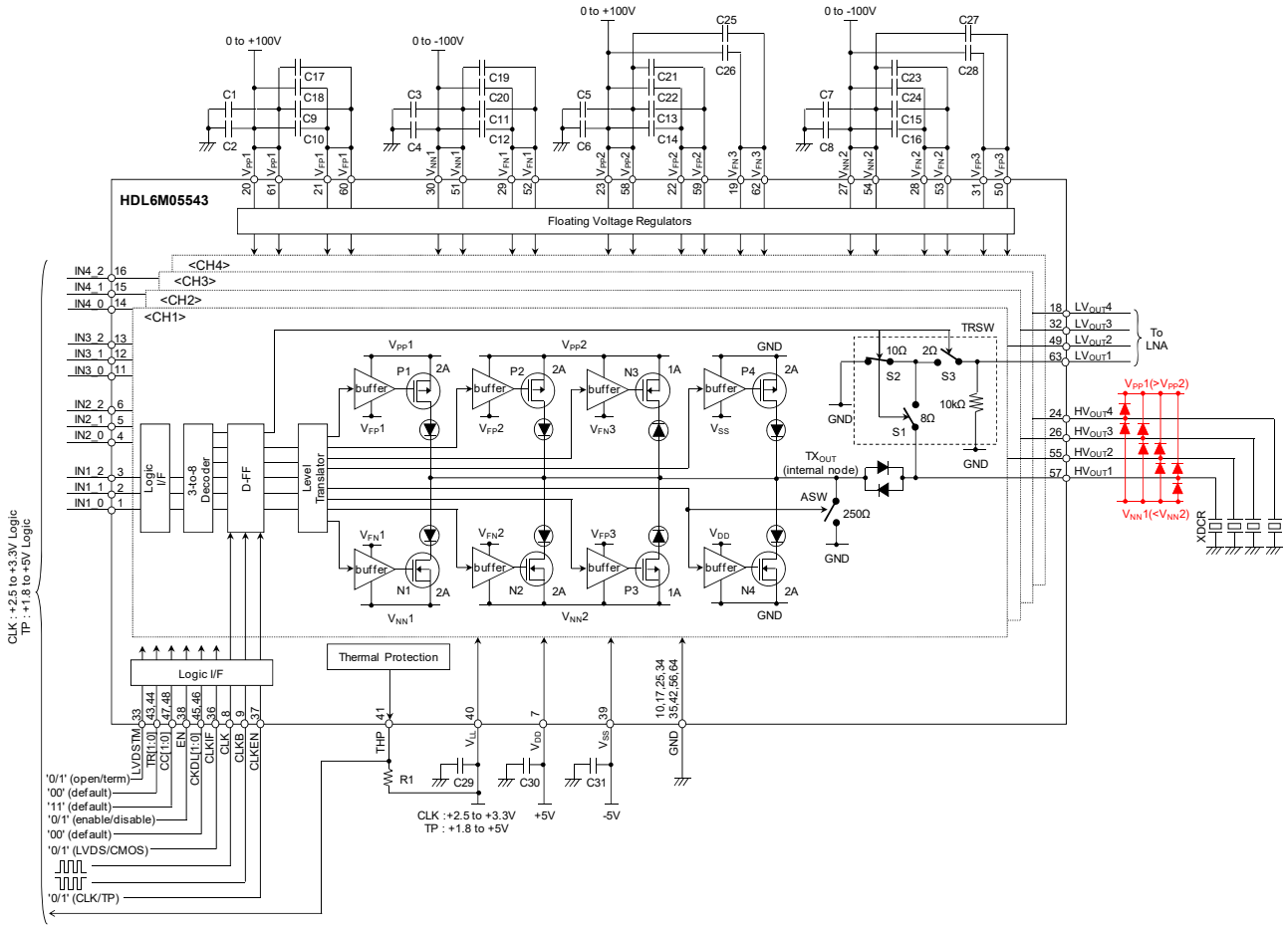


Fig.4 Typical Application Circuit

Note:

1. High-voltage power supply pins, $V_{PP}x/V_{NN}x$ (x=1,2), can draw fast transient currents up to ±2.0A. Therefore, ceramic capacitors of ≥200V 0.1μF to 1μF (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of ≥16V 10μF (C9~16), ≥16V 100nF (C17~28), and ≥16V 0.1μF to 1μF (C29~31) should also be connected between high-voltage power supply pins and corresponding floating voltage pins $V_{FP}x/V_{FN}x$, and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. Please refer to Mode Control Tables for detailed CC[1:0], TR[1:0], and CKDL[1:0] setting.
6. High-voltage diodes (e.g. BAV23S) between $HV_{OUT}x$ and $V_{PP}1/V_{NN}1$ (highest voltage) are recommended to clamp excessive voltage overshoot caused by reverberation.

4. Electrical Characteristics

4.1 Operating Supply Currents

Table 5 Operating Supply Currents

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25ºC, CLK=CLKB=100MHz/0(CLKEN=0/1), TR[1:0]=CKDL[1:0]='00',
HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	V_{LL} current	TP	I_{LLQD}	-	0.0	-	mA	Quiescent current-1 EN=1(Disable) INx_[2:0]='000' Current mode 3 (CC[1:0]='11') $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V
		LVDS CLK		-	0.1	-	mA	
		CMOS CLK		-	0.05	-	mA	
2	V_{DD} current	TP	I_{DDQD}	-	2.4	-	mA	
		LVDS CLK		-	2.4	-	mA	
		CMOS CLK		-	2.4	-	mA	
3	V_{SS} current		I_{SSQD}	-	0.62	-	mA	
4	$V_{PP}1$ current		I_{PP1QD}	-	0.04	-	mA	
5	$V_{NN}1$ current		I_{NN1QD}	-	0.04	-	mA	
6	$V_{PP}2$ current		I_{PP2QD}	-	0.04	-	mA	
7	$V_{NN}2$ current		I_{NN2QD}	-	0.04	-	mA	
8	V_{LL} current	TP	I_{LLQE}	-	0.05	-	mA	Quiescent current-2 EN=0(Enable) INx_[2:0]='000' Current mode 3 (CC[1:0]='11') $V_{PP}1/V_{NN}1$=+/-100V $V_{PP}2/V_{NN}2$=+/-100V
		LVDS CLK		-	0.15	-	mA	
		CMOS CLK		-	0.1	-	mA	
9	V_{DD} current	TP	I_{DDQE}	-	3	-	mA	
		LVDS CLK		-	15	-	mA	
		CMOS CLK		-	13	-	mA	
10	V_{SS} current		I_{SSQE}	-	0.9	-	mA	
11	$V_{PP}1$ current		I_{PP1QE}	-	0.16	-	mA	
12	$V_{NN}1$ current		I_{NN1QE}	-	0.16	-	mA	
13	$V_{PP}2$ current		I_{PP2QE}	-	0.16	-	mA	
14	$V_{NN}2$ current		I_{NN2QE}	-	0.16	-	mA	
15	V_{LL} current	TP	I_{LLPW}	-	0.05	-	mA	PW operating current EN=0 Current mode 3 (CC[1:0]='11') 4-channel active Bipolar 3-level 2-cycle P1/N1-drive f=5MHz, PRT=200µs $V_{PP}1/V_{NN}1$=+/-60V $V_{PP}2/V_{NN}2$=+/-60V
		LVDS CLK		-	0.15	-	mA	
		CMOS CLK		-	0.1	-	mA	
16	V_{DD} current	TP	I_{DDPW}	-	6.5	-	mA	
		LVDS CLK		-	22	-	mA	
		CMOS CLK		-	20	-	mA	
17	V_{SS} current		I_{SSPW}	-	5.5	-	mA	
18	$V_{PP}1$ current		I_{PP1PW}	-	2.2	-	mA	
19	$V_{NN}1$ current		I_{NN1PW}	-	2.4	-	mA	
20	$V_{PP}2$ current		I_{PP2PW}	-	0.16	-	mA	
21	$V_{NN}2$ current		I_{NN2PW}	-	0.16	-	mA	

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
22	V_{LL} current	TP	I_{LLCW3}	-	0.18	-	mA	CW operating current-1 EN=0 Current mode 3 (CC[1:0]='11') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V
		LVDS CLK		-	0.26	-	mA	
		CMOS CLK		-	0.21	-	mA	
23	V_{DD} current	TP	I_{DDCW3}	-	20	-	mA	
		LVDS CLK		-	35	-	mA	
		CMOS CLK		-	33	-	mA	
24	V_{SS} current		I_{SSCW3}	-	15	-	mA	
25	$V_{PP}1$ current		I_{PP1CW3}	-	0.16	-	mA	
26	$V_{NN}1$ current		I_{NN1CW3}	-	0.16	-	mA	
27	$V_{PP}2$ current		I_{PP2CW3}	-	84	-	mA	
28	$V_{NN}2$ current		I_{NN2CW3}	-	86	-	mA	
29	V_{LL} current	TP	I_{LLCW2}	-	0.27	-	mA	CW operating current-2 EN=0 Current mode 2 (CC[1:0]='10') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V
		LVDS CLK		-	0.3	-	mA	
		CMOS CLK		-	0.26	-	mA	
30	V_{DD} current	TP	I_{DDCW2}	-	19	-	mA	
		LVDS CLK		-	35	-	mA	
		CMOS CLK		-	33	-	mA	
31	V_{SS} current		I_{SSCW2}	-	13	-	mA	
32	$V_{PP}1$ current		I_{PP1CW2}	-	0.16	-	mA	
33	$V_{NN}1$ current		I_{NN1CW2}	-	0.16	-	mA	
34	$V_{PP}2$ current		I_{PP2CW2}	-	80	-	mA	
35	$V_{NN}2$ current		I_{NN2CW2}	-	83	-	mA	
36	V_{LL} current	TP	I_{LLCW1}	-	0.22	-	mA	CW operating current-3 EN=0 Current mode 1 (CC[1:0]='01') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V
		LVDS CLK		-	0.30	-	mA	
		CMOS CLK		-	0.26	-	mA	
37	V_{DD} current	TP	I_{DDCW1}	-	15	-	mA	
		LVDS CLK		-	31	-	mA	
		CMOS CLK		-	29	-	mA	
38	V_{SS} current		I_{SSCW1}	-	10	-	mA	
39	$V_{PP}1$ current		I_{PP1CW1}	-	0.16	-	mA	
40	$V_{NN}1$ current		I_{NN1CW1}	-	0.16	-	mA	
41	$V_{PP}2$ current		I_{PP2CW1}	-	77	-	mA	
42	$V_{NN}2$ current		I_{NN2CW1}	-	80	-	mA	
43	V_{LL} current	TP	I_{LLCW0}	-	0.31	-	mA	CW operating current-4 EN=0 Current mode 0 (CC[1:0]='00') 4-channel active Bipolar 3-level Continuous P2/N2-drive f=5MHz $V_{PP}1/V_{NN}1$=+/-5V $V_{PP}2/V_{NN}2$=+/-5V
		LVDS CLK		-	0.35	-	mA	
		CMOS CLK		-	0.31	-	mA	
44	V_{DD} current	TP	I_{DDCW0}	-	12	-	mA	
		LVDS CLK		-	28	-	mA	
		CMOS CLK		-	26	-	mA	
45	V_{SS} current		I_{SSCW0}	-	7.9	-	mA	
46	$V_{PP}1$ current		I_{PP1CW0}	-	0.16	-	mA	
47	$V_{NN}1$ current		I_{NN1CW0}	-	0.16	-	mA	
48	$V_{PP}2$ current		I_{PP2CW0}	-	67	-	mA	
49	$V_{NN}2$ current		I_{NN2CW0}	-	70	-	mA	

4.2 Static Characteristics

Table 6 Static Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25°C, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	$HV_{OUT}x$ output voltage range	$HV_{OUT}x$	-100	-	+100	V	
2	$HV_{OUT}x$ high-side peak current	I_{OH}	-	2.0	-	A	P1 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
			-	2.0	-	A	P2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	P2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	P2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	P2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 0 (CC[1:0]='00')
			-	1.0	-	A	N3 active, $V_{PP}1/V_{NN}1$=+/-80V, $V_{PP}2/V_{NN}2$=+/-20V, Current mode 3
3	$HV_{OUT}x$ high-side GND clamp peak current	I_{OHCL}	-	2.0	-	A	N4 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
4	$HV_{OUT}x$ low-side peak current	I_{OL}	-	2.0	-	A	N1 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
			-	2.0	-	A	N2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	N2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	N2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	N2 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V Current mode 0 (CC[1:0]='00')
			-	1.0	-	A	P3 active, $V_{PP}1/V_{NN}1$=+/-80V, $V_{PP}2/V_{NN}2$=+/-20V, Current mode 3
5	$HV_{OUT}x$ low-side GND clamp peak current	I_{OLCL}	-	2.0	-	A	P4 active, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V
6	$HV_{OUT}x$ high-side on-resistance	R_{ONH}	-	11	-	Ω	P1 active, I_{OH}=100mA
			-	11	-	Ω	P2/N3 active, I_{OH}=100mA Current mode 3 (CC[1:0]='11')
			-	13	-	Ω	P2 active, I_{OH}=100mA Current mode 2 (CC[1:0]='10')
			-	19	-	Ω	P2 active, I_{OH}=100mA Current mode 1 (CC[1:0]='01')
			-	32	-	Ω	P2 active, I_{OH}=100mA Current mode 0 (CC[1:0]='00')
7	$HV_{OUT}x$ high-side GND clamp on-resistance	R_{ONHCL}	-	10	-	Ω	N4 active, I_{OHCL}=100mA
8	$HV_{OUT}x$ low-side on-resistance	R_{ONL}	-	10	-	Ω	N1 active, I_{OL}=100mA
			-	10	-	Ω	N2/P3 active, I_{OL}=100mA Current mode 3 (CC[1:0]='11')
			-	12	-	Ω	N2 active, I_{OL}=100mA Current mode 2 (CC[1:0]='10')
			-	18	-	Ω	N2 active, I_{OL}=100mA Current mode 1 (CC[1:0]='01')
			-	30	-	Ω	N2 active, I_{OL}=100mA Current mode 0 (CC[1:0]='00')
9	$HV_{OUT}x$ low-side GND clamp on-resistance	R_{ONLCL}	-	11	-	Ω	P4 active, I_{OLCL}=100mA
10	$HV_{OUT}x$ off-capacitance	C_{HVOFF}	-	40	-	pF	$TX_{OUT}x$=HiZ, TRSW=off

4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V, T_A=25ºC, TR[1:0]=CKDL[1:0]='00', CC[1:0]='11', CLK=CLKB=100MHz/0(CLKEN=0/1), HV_{OUT} load=220pF//200Ω, LV_{OUT} load=47pF//200Ω, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions	
				Min	Typ	Max			
1	Output frequency		f_{OUT}	-	20	-	MHz		
2	Output rise propagation delay	TP mode	t_{dr}	-	31	-	ns	See Fig.5	
		CLK mode		-	39	-	ns		
3	Output fall propagation delay	TP mode	t_{df}	-	31	-	ns		
		CLK mode		-	39	-	ns		
4	Output rise propagation delay clamp	TP mode	t_{drCL}	-	31	-	ns		
		CLK mode		-	39	-	ns		
5	Output fall propagation delay clamp	TP mode	t_{dfCL}	-	31	-	ns		
		CLK mode		-	39	-	ns		
6	Propagation delay matching		Δt_d	-	±1	±3	ns		
7	Output rise time		t_r	-	16	-	ns	P1 active	See Fig.5
				-	16	-	ns	P2 active, CC[1:0]='11'	
				-	19	-	ns	P2 active, CC[1:0]='10'	
				-	27	-	ns	P2 active, CC[1:0]='01'	
				-	52	-	ns	P2 active, CC[1:0]='00'	
			t_{rCL}	-	10	-	ns	P4 active	
8	Output fall time		t_f	-	16	-	ns	N1 active	
				-	16	-	ns	N2 active, CC[1:0]='11'	
				-	19	-	ns	N2 active, CC[1:0]='10'	
				-	27	-	ns	N2 active, CC[1:0]='01'	
				-	52	-	ns	N2 active, CC[1:0]='00'	
			t_{fCL}	-	10	-	ns	N4 active	
9	2nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, f_{OUT}=5MHz See Fig.6	
10	Pulse cancellation		HDPC	-	-40	-	dBc		
			HDPC2	-	-40	-	dBc		
11	RMS output jitter		t_J	-	10	-	ps	Bipolar CW, f_{OUT}=5MHz $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-5V	
12	Crosstalk between channels		X_{TLK}	-	-70	-	dB	f_{OUT}=5MHz, $10V_{p-p}$, HV_{OUT} load=50Ω	
13	Output enable time	TP	t_{EN}	-	28	-	ns	See Fig.7	
		LVDS CLK		-	600	-	ns		
		CMOS CLK		-	600	-	ns		
14	Output disable time		t_{DS}	-	36	-	ns		
15	Clock mode enable time		t_{CLKEN}	-	600	-	ns		
16	Clock mode disable time		t_{CLKDS}	-	36	-	ns		

4.4 Integrated Peripheral Circuits Characteristics

T/R Switch

Table 8 T/R Switch Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, $V_{PP}1/V_{NN}1=V_{PP}2/V_{NN}2$=+/-60V, T_A=25ºC, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	$LV_{OUT}x$ output voltage range		$LV_{OUT}x$	-0.85	-	+0.85	V	
2	TRSW on-resistance		R_{ONTR}	-	10	-	Ω	$HV_{OUT}x$=100mV, $LV_{OUT}x$=0V
3	TRSW on-capacitance		C_{ONTR}	-	15	-	pF	
4	TRSW off-resistance on HVOUTx		$R_{OFFTRHV}$	1	-	-	MΩ	
5	TRSW off-resistance on LVOUTx		$R_{OFFTRLV}$	8	10	12	kΩ	
6	Spike voltage on $HV_{OUT}x$ and $LV_{OUT}x$		V_{TRN}	-	-	50	mV_{PP}	50pF//200Ω load on $HV_{OUT}x$ 20pF//200Ω load on $LV_{OUT}x$
7	TRSW turn-on time	TR[1:0]='00'	t_{dTRON}	-	400	-	ns	Logic input-to-ready for Rx signal See Fig.8
		TR[1:0]='01'		-	500	-	ns	
		TR[1:0]='10'		-	600	-	ns	
		TR[1:0]='11'		-	700	-	ns	
8	TRSW turn-off time		t_{dTROFF}	-	50	100	ns	See Fig.8
9	Tx setup time		t_{TXSU}	100	-	-	ns	INx_[2:0]='100'(GND) for at least 100ns before Tx burst. See Fig.8

Analog Switch

Table 9 Analog Switch Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R_{ONASW}	-	250	-	Ω	

HV Blocking Diode

Table 10 Output HV Blocking Diode Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FHVD}	-	1.0	-	V	I_F=100mA
			-	1.2	-	V	I_F=200mA
2	Reverse voltage	V_{RHVD}	200	-	-	V	I_R=1μA

LV Noise-cut Diode

Table 11 Output LV Noise-cut Diode Characteristics

T_A=25ºC

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V_{FLVD}	-	1.1	-	V	I_F=100mA
			-	1.25	-	V	I_F=200mA

Thermal Protection

Table 12 Thermal Protection Characteristics

V_{LL}=2.5V, V_{DD}/V_{SS}=+/-5V, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, V_{LL}=2.5V, I_{THP}=1mA
4	THP temperature threshold	T_{THP}	100	110	120	ºC	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	ºC	

5. Switching Time Diagram

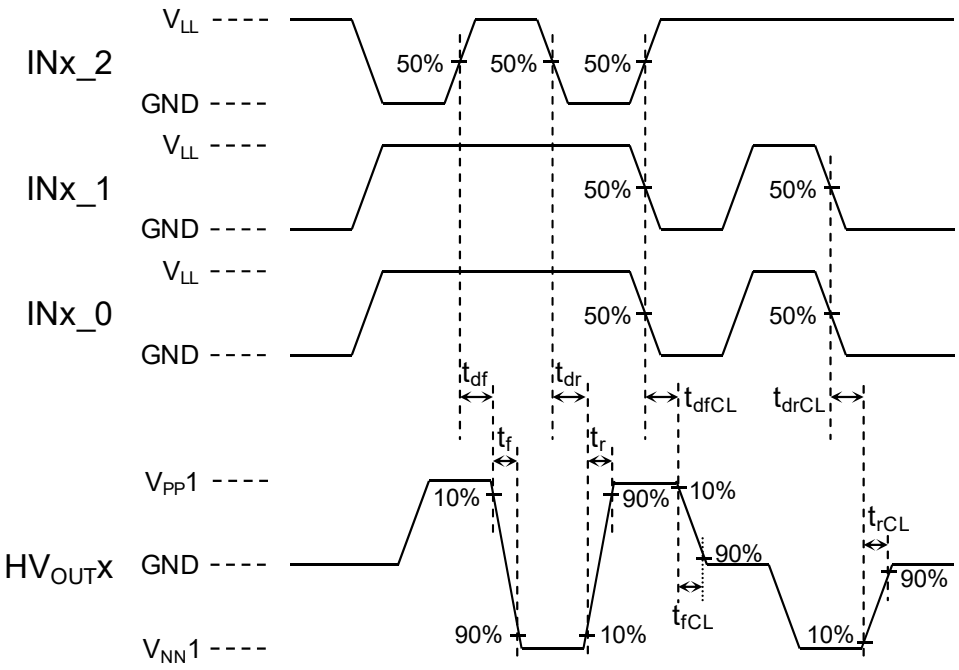
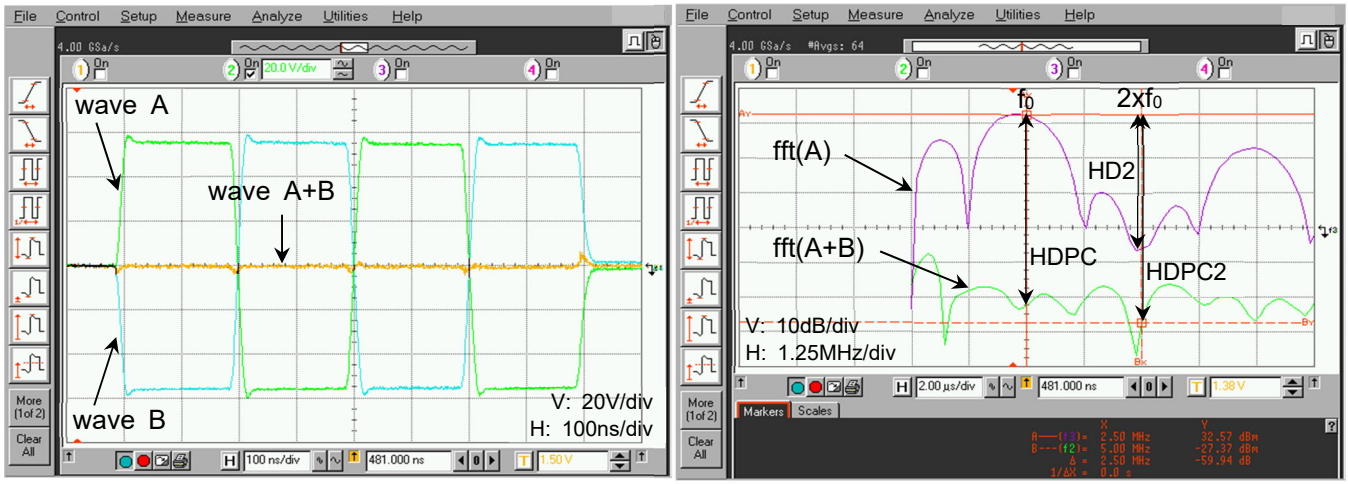


Fig.5 Propagation delay and Output rise/fall time



Example waveforms: VPP/VNN=+/-60V, f_0=2.5MHz, 2-cycle, HV_{OUT} load=220pF//200Ω

Fig.6 2nd harmonic distortion and Pulse cancellation

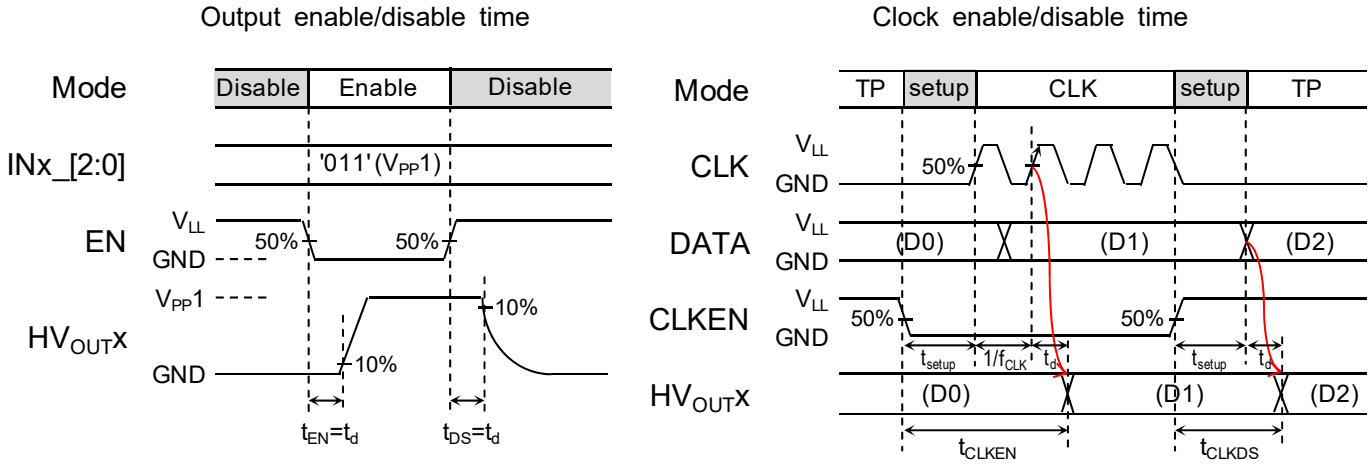


Fig.7 Output enable/disable and Clock enable/disable time

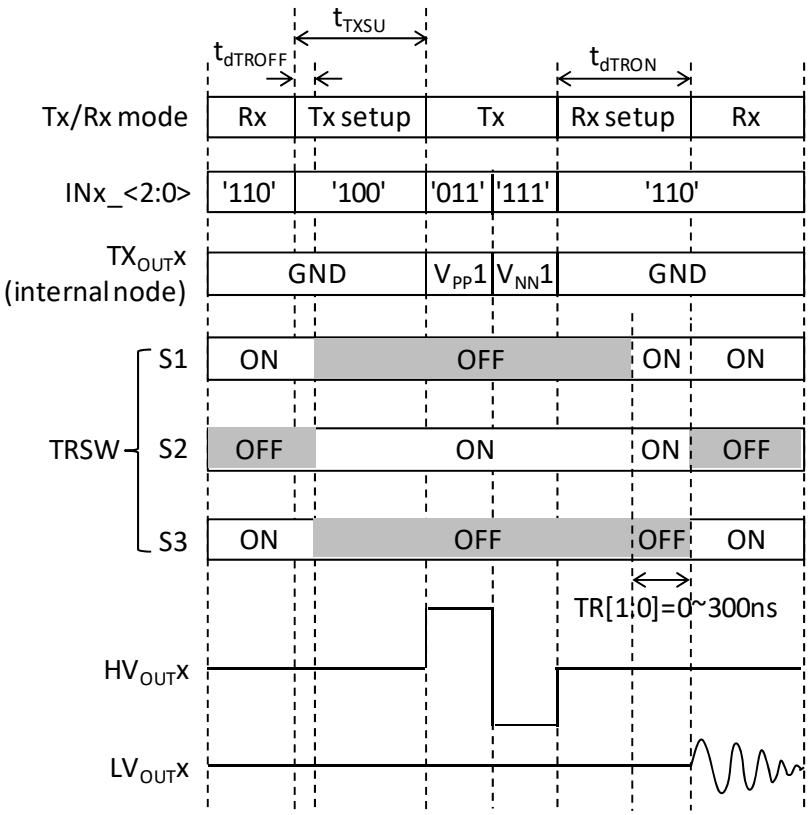


Fig.8 T/R Switch turn-on/off time

6. Truth Table and Mode Control tables

Table 13 Truth table

Logic Inputs				Internal MOSFET state												Output state	
EN	INx_2	INx_1	INx_0	P1	N1	P2	N2	P3	N3	P4	N4	ASW	TRSW			$TX_{OUT}x$	$LV_{OUT}x$
				+HV1	-HV1	+HV2	-HV2	-HV2	+HV2	GND	GND	GND	S1	S2	S3	(internal node)	
0	0	0	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	HiZ	10kΩ
0	0	0	1	OFF	OFF	**ON**	OFF	OFF	**ON** *	OFF	OFF	OFF	OFF	**ON**	OFF	+HV2	10kΩ
0	0	1	0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	**ON**	HiZ	$HV_{OUT}x$
0	0	1	1	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	+HV1	10kΩ
0	1	0	0	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	OFF	**ON**	OFF	GND	10kΩ
0	1	0	1	OFF	OFF	OFF	**ON**	**ON** *	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	-HV2	10kΩ
0	1	1	0	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	**ON**	**ON**	**ON**	OFF	**ON**	GND	$HV_{OUT}x$
0	1	1	1	OFF	**ON**	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	-HV1	10kΩ
1	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	**ON**	OFF	HiZ	10kΩ

Note: $V_{PP}1$/ $V_{NN}1$=+/-HV1, $V_{PP}2$/ $V_{NN}2$=+/-HV2, x=1~4

Note: When the current mode is other than 3 (CC[1:0]≠'11'), both P3 and N3 are always in off-state.

Table 14 P2/N2 drive current mode

			Iout [A]	
Current Mode	CC1	CC0	P2	N2
0	0	0	0.5	0.5
1	0	1	1	1
2	1	0	1.5	1.5
3	1	1	2	2

Note:

Recommended mode is as follows:

- Current mode 2 or 3 for high amplitude short cycle pulse waveforms, or for driving heavy load
- Current mode 0 or 1 for low amplitude long pulse train waveforms (e.g. CW), or for driving light load

Table 15 TRSW S1-S2 turn-on overlap time control mode

			S1-S2 ON
TRSW Control Mode	TR1	TR0	overlap time [ns]
0	0	0	0 (default)
1	0	1	100
2	1	0	200
3	1	1	300

Note: Detailed switching time diagram is shown in Fig.8.

Table 16 Clock edge timing control mode

			CLK
CLK Edge Control Mode	CKDL1	CKDL0	edge [ns]
0	0	0	0 (default)
1	0	1	0.5
2	1	0	1
3	1	1	1.5

Note: Detailed switching time diagram is shown in Fig.3.

7. Pin Configuration

Table 17 Pin Configuration

Pin#	Pin Name	I/O	Function
1	IN1_0	I	The least significant bit of logic input of channel 1
2	IN1_1	I	The 2nd significant bit of logic input of channel 1
3	IN1_2	I	The most significant bit of logic input of channel 1
4	IN2_0	I	The least significant bit of logic input of channel 2
5	IN2_1	I	The 2nd significant bit of logic input of channel 2
6	IN2_2	I	The most significant bit of logic input of channel 2
7	V_{DD}	-	Positive low voltage power supply (+5V)
8	CLK	I	Positive clock input (up to 200MHz)
9	CLKB	I	Negative clock Input (up to 200MHz)
10	GND	-	Drive power ground (0V)
11	IN3_0	I	The least significant bit of logic input of channel 3
12	IN3_1	I	The 2nd significant bit of logic input of channel 3
13	IN3_2	I	The most significant bit of logic input of channel 3
14	IN4_0	I	The least significant bit of logic input of channel 4
15	IN4_1	I	The 2nd significant bit of logic input of channel 4
16	IN4_2	I	The most significant bit of logic input of channel 4
17	GND	-	Drive power ground (0V)
18	$LV_{OUT}4$	O	Low voltage output of channel 4
19	$V_{FN}3$	-	Built-in power supply for N-MOS (N3) gate drive
20	$V_{PP}1$	-	Positive high voltage power supply 1 (0 to +100V)
21	$V_{FP}1$	-	Built-in power supply for P-MOS (P1) gate drive
22	$V_{FP}2$	-	Built-in power supply for P-MOS (P2) gate drive
23	$V_{PP}2$	-	Positive high voltage power supply 2 (0 to +100V)
24	$HV_{OUT}4$	O	High voltage output of channel 4
25	GND	-	Drive power ground (0V)
26	$HV_{OUT}3$	O	High voltage output of channel 3
27	$V_{NN}2$	-	Negative high voltage power supply 2 (0 to -100V)
28	$V_{FN}2$	-	Built-in power supply for N-MOS (N2) gate drive
29	$V_{FN}1$	-	Built-in power supply for N-MOS (N1) gate drive
30	$V_{NN}1$	-	Negative high voltage power supply 1 (0 to -100V)
31	$V_{FP}3$	-	Built-in power supply for P-MOS (P3) gate drive
32	$LV_{OUT}3$	O	Low voltage output of channel 3

Table 17 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
33	LVDSTM	-	Control of LVDS termination between CLK and CLKB, Hi=embedded 100Ω, Low=open (50kΩ internal pull-down resistor)
34	GND	-	Drive power ground (0V)
35	GND	-	Drive power ground (0V)
36	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50kΩ internal pull-up resistor)
37	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50kΩ internal pull-up resistor)
38	EN	I	Control of drive output enable, Hi=off, Low=on (50kΩ internal pull-up resistor)
39	V_{SS}	-	Negative low voltage power supply (-5V)
40	V_{LL}	-	Positive voltage supply of logic input interface (1.8 to 5V)
41	THP	O	Thermal protection output flag, open N-MOS drain
42	GND	-	Drive power ground (0V)
43	TR0	I	Lower bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
44	TR1	I	Upper bit of control of T/R switch S1 and S2 turn-on overlap time (50kΩ internal pull-down resistor)
45	CKDL0	I	Lower bit of control of clock edge timing (50kΩ internal pull-down resistor)
46	CKDL1	I	Upper bit of control of clock edge timing (50kΩ internal pull-down resistor)
47	CC0	I	Lower bit of control of P2/N2 drive current (50kΩ internal pull-up resistor)
48	CC1	I	Upper bit of control of P2/N2 drive current (50kΩ internal pull-up resistor)
49	$LV_{OUT}2$	O	Low voltage output of channel 2
50	$V_{FP}3$	-	Built-in power supply for P-MOS (P3) gate drive
51	$V_{NN}1$	-	Negative high voltage power supply 1 (0 to -100V)
52	$V_{FN}1$	-	Built-in power supply for N-MOS (N1) gate drive
53	$V_{FN}2$	-	Built-in power supply for N-MOS (N2) gate drive
54	$V_{NN}2$	-	Negative high voltage power supply 2 (0 to -100V)
55	$HV_{OUT}2$	O	High voltage output of channel 2
56	GND	-	Drive power ground (0V)
57	$HV_{OUT}1$	O	High voltage output of channel 1
58	$V_{PP}2$	-	Positive high voltage power supply 2 (0 to +100V)
59	$V_{FP}2$	-	Built-in power supply for P-MOS (P2) gate drive
60	$V_{FP}1$	-	Built-in power supply for P-MOS (P1) gate drive
61	$V_{PP}1$	-	Positive high voltage power supply 1 (0 to +100V)
62	$V_{FN}3$	-	Built-in power supply for N-MOS (N3) gate drive
63	$LV_{OUT}1$	O	Low voltage output of channel 1
64	GND	-	Drive power ground (0V)

■ Package

Table 18 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-64(0909)B	QN064-B-P-SD	QFN9x9-B-T-SD	QN064-B-M-S2	QN064-B-L-SD	QN064-B-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Fig. 9 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

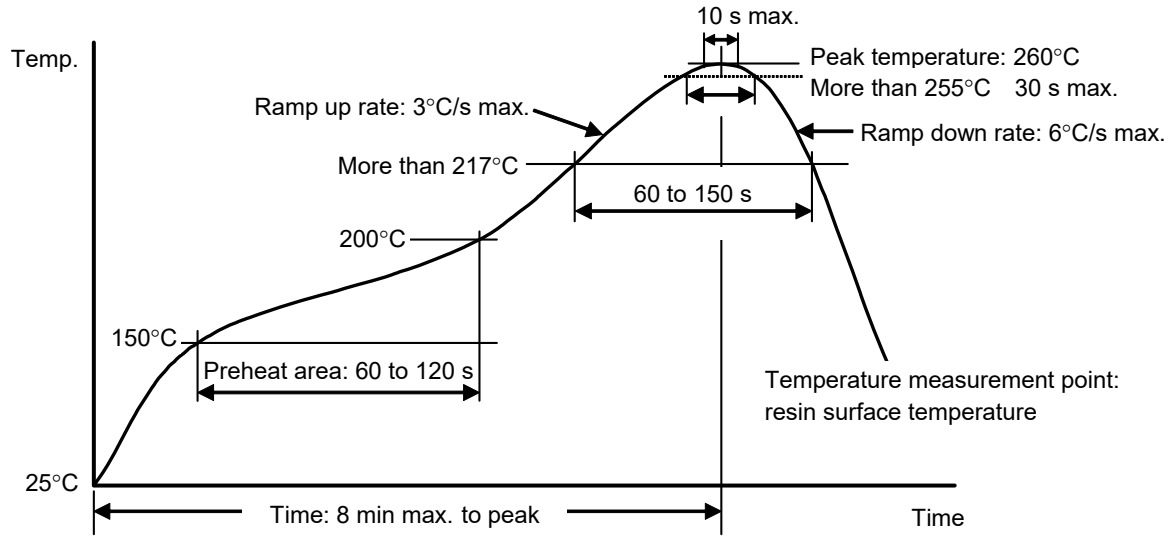


Fig.9 Resistance to Soldering Heat Condition for Package (Reflow Method)

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3. ABLIC Inc. assumes no obligation or any way of compensation should any fault about customer products and applications using ABLIC Inc. products be found in marketplace. Only in such a case fault of ABLIC Inc. is evident and products concerned do not meet the Product Specification, compensation shall be conducted if claimed within one year of product delivery up to in the way of product replacement or payment of equivalent amount.

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■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

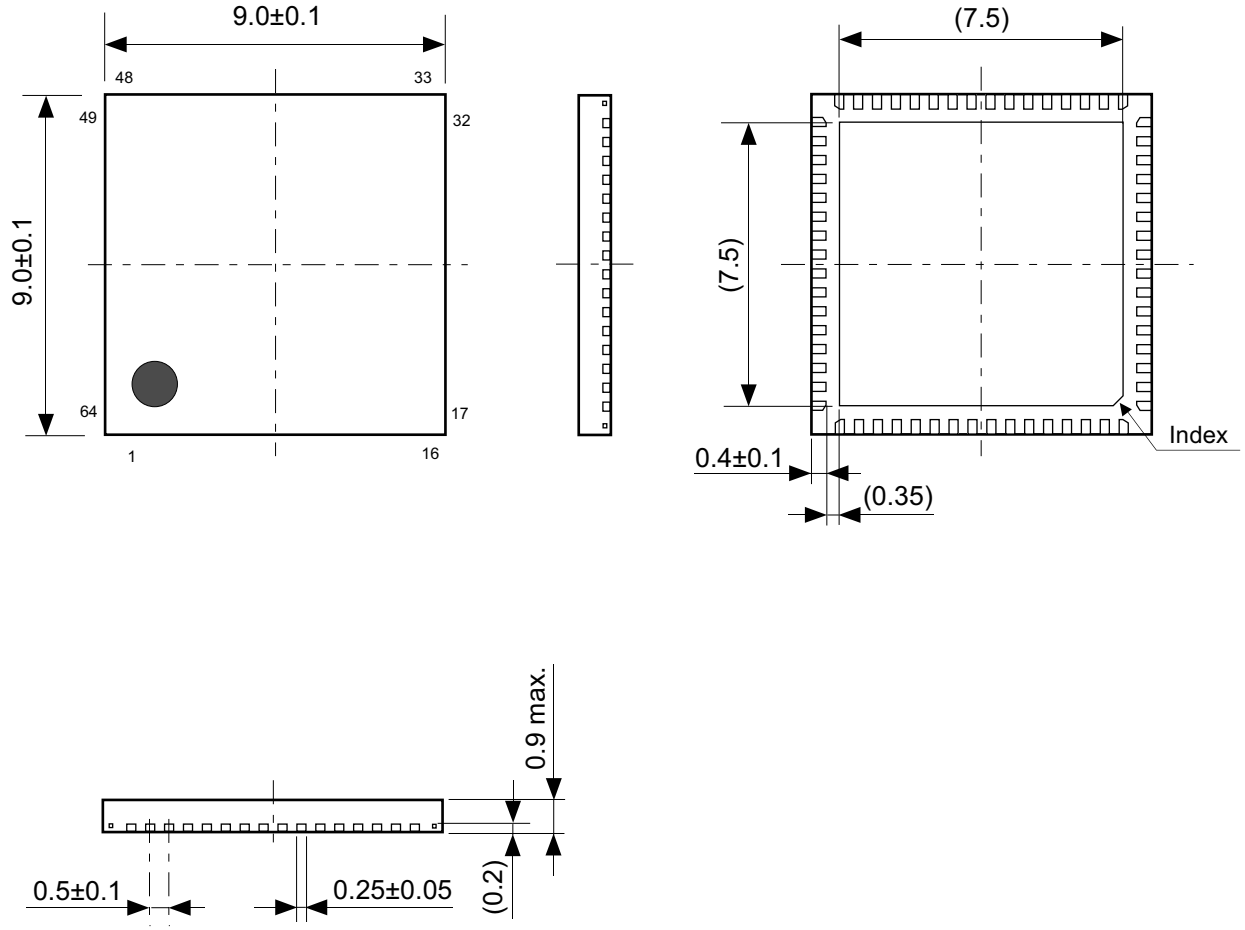
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

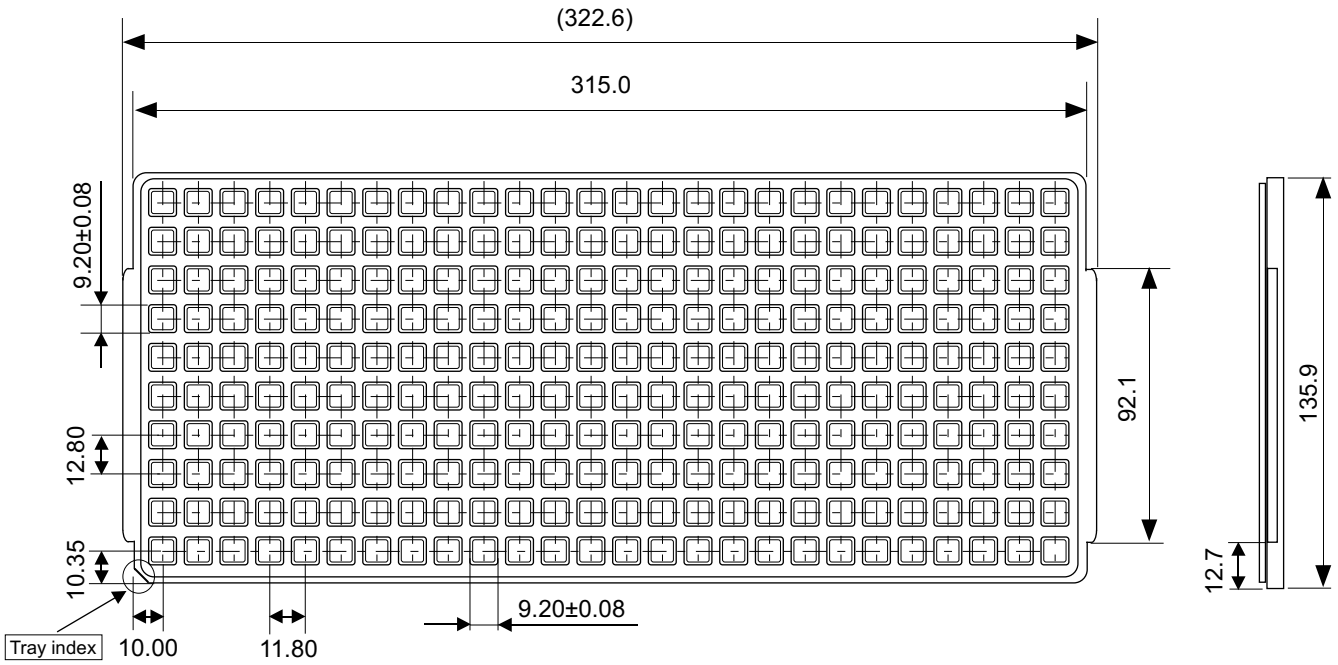
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

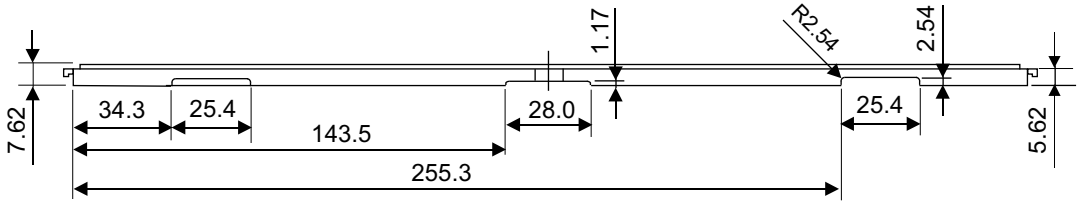
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.



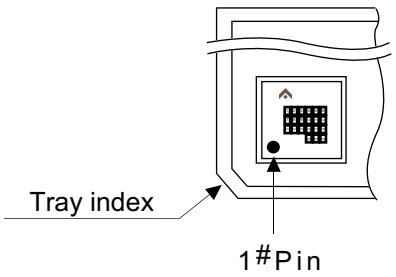
No. QN064-B-P-SD-2.0

TITLE	QFN64-B-PKG Dimensions
No.	QN064-B-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



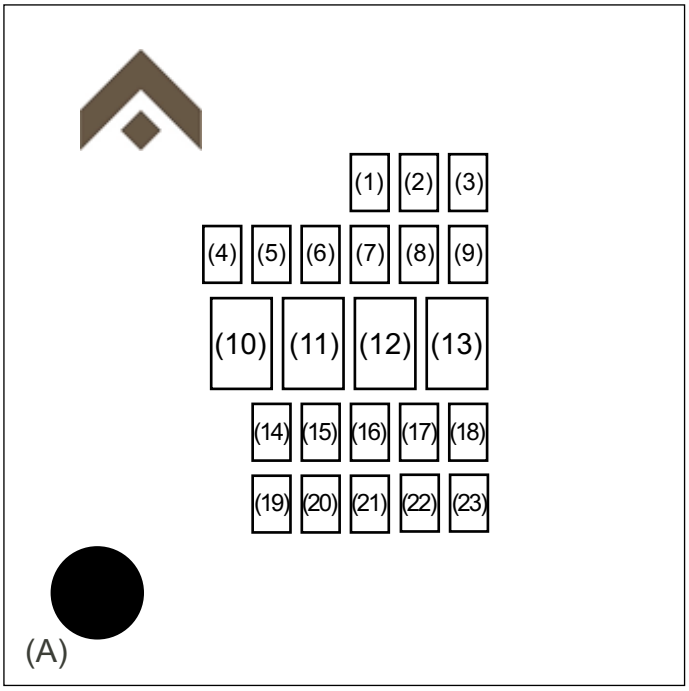


(Direction of IC in tray)



No. QFN9x9-B-T-SD-1.0

TITLE	QFN9x9-B-Tray		
No.	QFN9x9-B-T-SD-1.0		
ANGLE		QTY.	260
UNIT	mm		
ABLIC Inc.			



(1) : Year of assembly

(2) : Month of assembly

(3) : Week of assembly

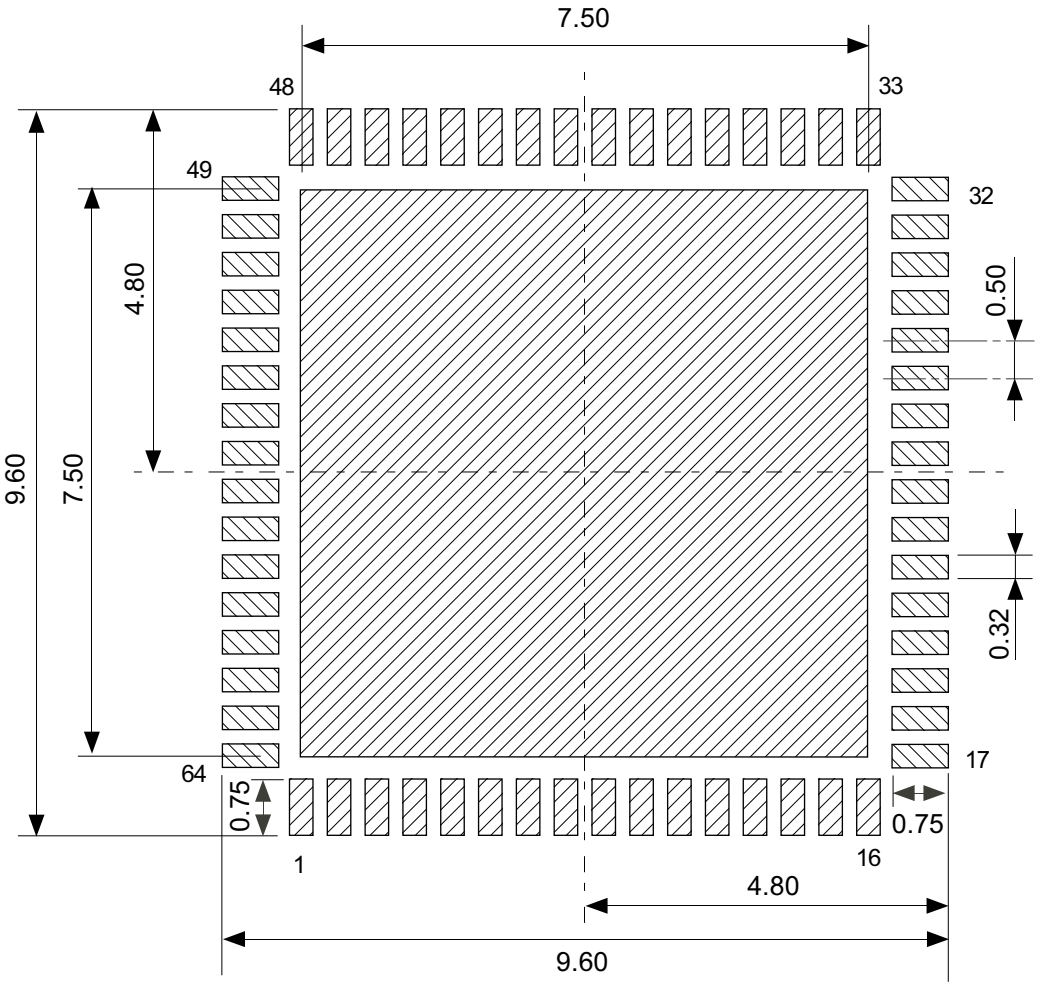
(4) to (13) : Product code

(14) to (23) : Quality control code

(A) : 1-pin mark

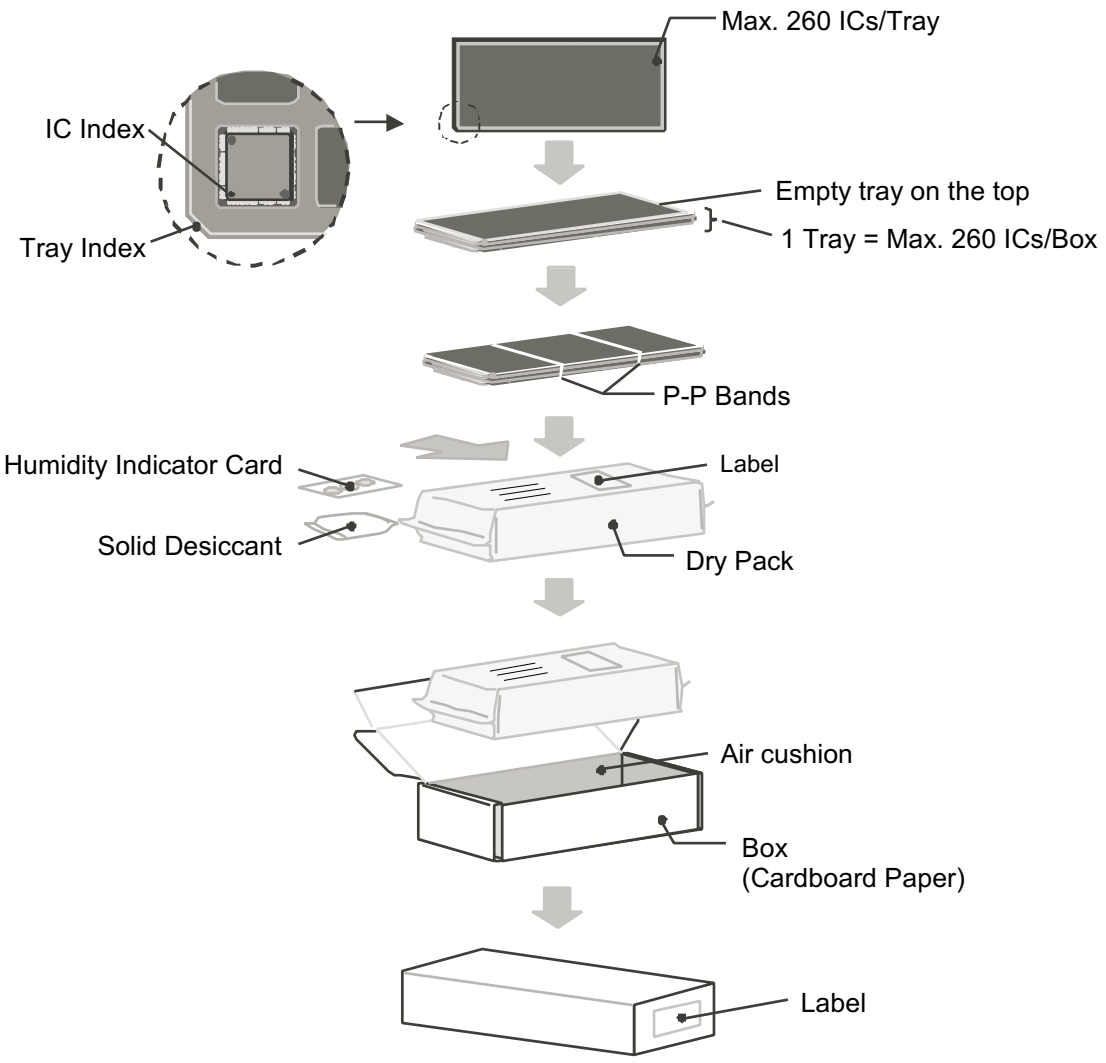
No. QN064-B-M-S2-1.0

TITLE	QFN64-B-Markings (S-UM5543 / S-UM5584)		
No.	QN064-B-M-S2-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN064-B-L-SD-2.0

TITLE	QFN64-B -Land Recommendation
No.	QN064-B-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN064-B-K-SD-2.0

TITLE	QFN64-B -Packing Procedure
No.	QN064-B-K-SD-2.0
ANGLE	
UNIT	
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