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16-CHANNEL (4 BANKS OF 4-CHANNEL) HIGH-VOLTAGE ANALOG SWITCH

The ABLIC Inc. HDL6M06502B is 16-channel high-voltage analog switch IC operated only by a single 5V for ultrasound imaging applications.
The HDL6M06502B consists of 4 sets of 4 single-pole, single-throw (SPST) analog switches controlled by 4 logic inputs. The HDL6M06502B has a unique pin-out which makes PCB traces easier.

Functions

- 16-channel (4 banks of 4-channel) high-voltage SPST analog switch with active ground clamp

Features

- 0V to ±100V analog signal voltage range (10kHz to 20MHz signal frequency range)
- 2A peak analog signal current per channel
- 8Ω main switch on-resistance
- 40kΩ bleed resistor on probe side
- Low on/off-capacitance
- -52dB off-isolation at 5MHz (load-independent)
- -60dB switch crosstalk
- 20Ω ground clamp switch on probe side alternately turned on/off with main switch
- DS_ASW to disable 20Ω ground clamp switch
- 1.8V to 5V CMOS logic interface
- Single +5V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- Low power dissipation (static 1mW)
- Unique pin configuration for easy PCB traces (SPs on one side and STs on opposite side)
- 52-lead 8x8mm QFN package (RoHS compliant)

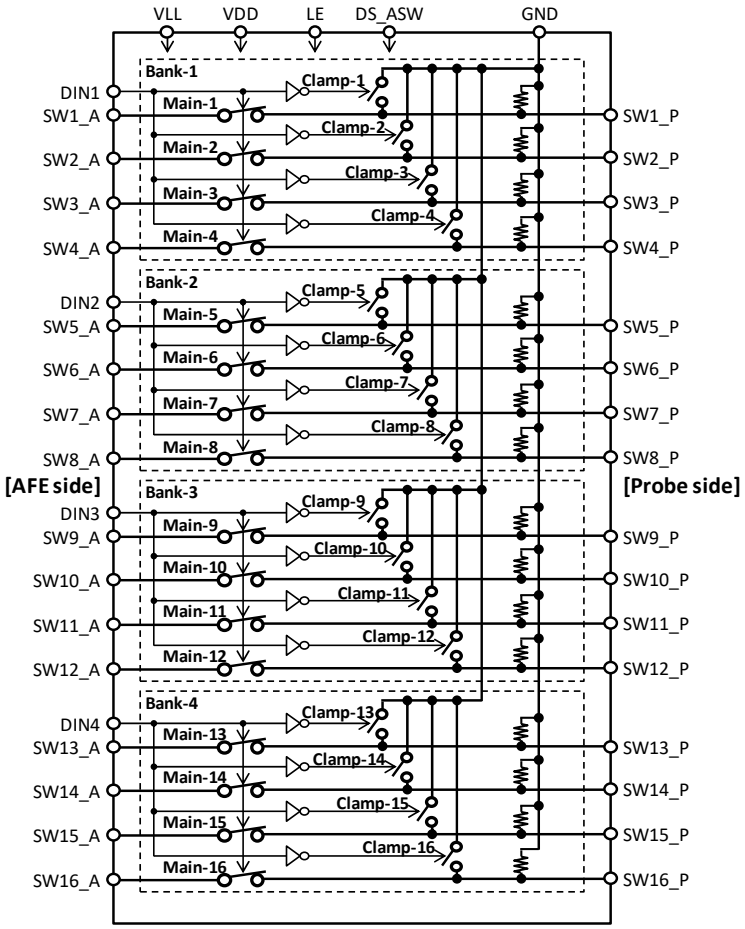

Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply voltage	V_{LL}	-0.4 to +7	V	
2	Positive supply voltage	V_{DD}	-0.4 to +7	V	
3	Logic input voltage (x=1~4)	DINx, LE, DS_ASW	-0.4 to +7	V	
4	Analog signal range	V_{SIG}	-105 to +105	V	
5	Peak analog signal current per channel	I_{SW}	-105 to +105	V	SW_A
			-105 to +105	V	SW_P when Switch ON
			-2 to +2	V	SW_P when Switch OFF, DS_ASW=0
			-105 to +105	V	SW_P when Switch OFF, DS_ASW=1
6	Operating junction temperature	T_{Jop}	-20 to +150	°C	
7	Storage temperature	T_{STG}	-55 to +150	°C	
8	Maximum power dissipation	P_{Dmax}	4	W	

NOTE: * Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Application Circuits

2.1 Operating Supply Voltages, Temperature, and Logic Inputs

Table 2 Operating Supply Voltages and Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V_{LL}	1.7	1.8 to 5	V_{DD}	V	
2	Positive supply voltage	V_{DD}	4.75	5	5.25	V	
3	IC substrate voltage *1	V_{SUB}	-	0	-	V	
4	Operating free-air temperature	T_A	0		75	°C	
5	High-level logic input voltage	V_{IH}	0.8V_{LL}	-	V_{LL}	V	
6	Low-level logic input voltage	V_{IL}	0	-	0.2V_{LL}	V	
7	Logic input high current *2	I_{IH}	-10	-	10	µA	DINx (x=1~4), LE, DS_ASW
8	Logic input low current	I_{IL}	-10	-	10	µA	
9	Logic input capacitance	C_{IN}	-	2	-	pF	
10	Setup time	t_{SU}	20	-	-	ns	
11	Hold time	t_{HLD}	20	-	-	ns	
12	LE time width	t_{LEW}	20	-	-	ns	

NOTE:
*1) Thermal pad on the bottom of the package must be soldered to the ground.
*2) DS_ASW has 100µA leakage at V_{LL}=5V due to 50kΩ internal pull-down resistor.

2.2 Power Supply Sequencing

No power supply sequencing is required even if V_{LL} is different from V_{DD}.
Please apply the V_{DD} voltage to the V_{LL} when operating with a single 5V.

2.3 Application Circuits

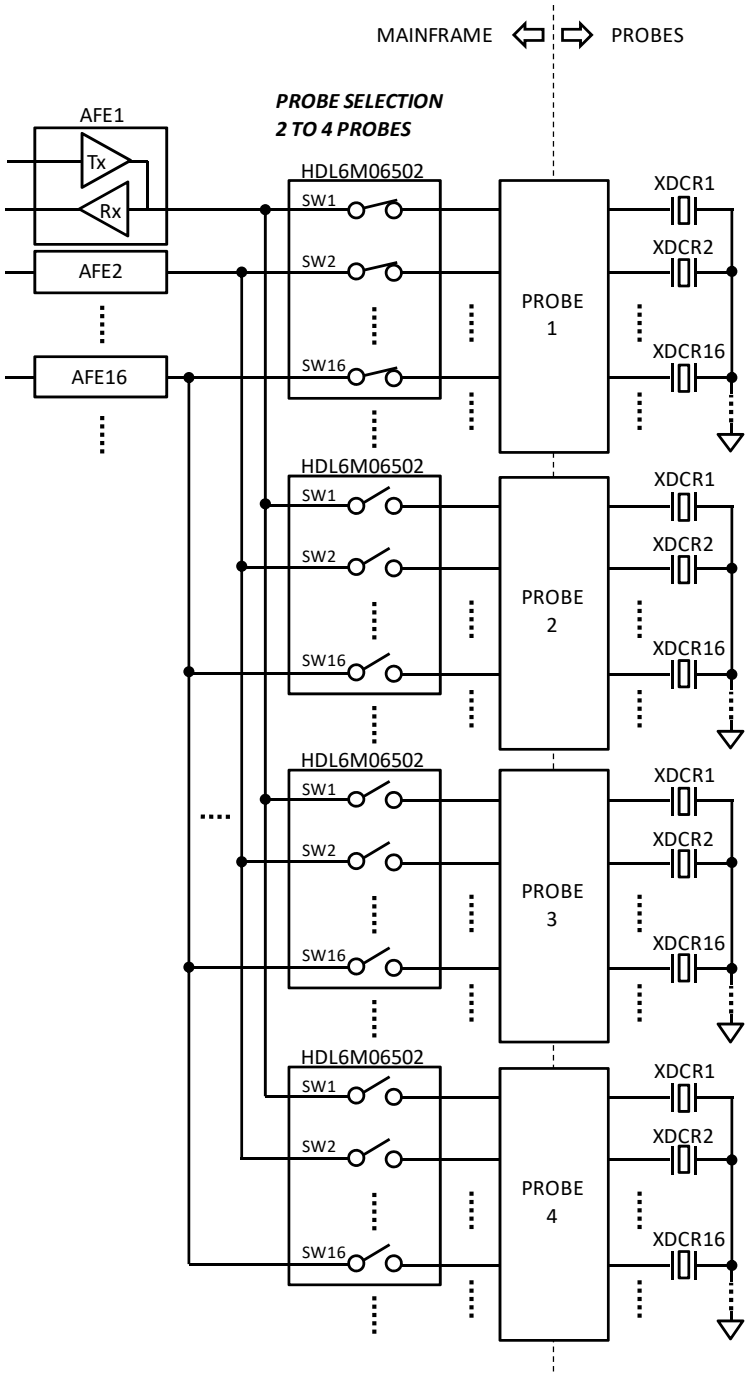

Fig.2 Probe selection (2 to 4 probes) in ultrasound imaging application

3. Electrical Characteristics

DC Characteristics

Table 3 DC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LE=0, DS_ASW=0, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range	V_{SIG}	-100	-	+100	V	
2	V_{LL} quiescent current	I_{LLQ}	-	0.1	-	μA	Quiescent current-1 All main switches off
3	V_{DD} quiescent current	I_{DDQ}	-	250	-	μA	
4	V_{LL} quiescent current	I_{LLQ}	-	0.1	-	μA	Quiescent current-2 All main switches on
5	V_{DD} quiescent current	I_{DDQ}	-	250	-	μA	
6	V_{LL} dynamic current	I_{LL}	-	0.4	1	μA	Dynamic current All channels switching simultaneously at f_{SW}=50kHz
7	V_{DD} dynamic current	I_{DD}	-	1.6	2	mA	
8	DC offset main switch off	V_{OS}	-	0	-	mV	
9	Small signal main switch on-resistance	R_{ONS}	-	8	10	Ω	V_{SIG}=0.1Vpp to 5Vpp @5MHz, R_S=10Ω
10	Small signal main switch on-resistance matching	ΔR_{ONS}	-	2	5	%	V_{SIG}=0V, I_{SIG}=5mA
11	Large signal main switch on-resistance	R_{ONL}	-	8	-	Ω	V_{SIG}=20Vpp@5MHz, R_S=10Ω
12	GND clamp on-resistance	R_{ONCL}	-	20	-	Ω	Main switches off, probe side
13	Shunt resistance	R_{BLD}	30	40	50	kΩ	Probe side
14	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

AC Characteristics

Table 4 AC Characteristics

V_{LL}=3.3V, V_{DD}=5V, LE=0, DS_ASW=0, T_A=25ºC, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Turn-on time	t_{ON}	-	2	5	μs	
		t_{ON_ASW}	-	2	5	μs	
2	Turn-off time	t_{OFF}	-	2	5	μs	
		t_{OFF_ASW}	-	2	5	μs	
3	Output switching frequency	f_{SW}	-	-	50	kHz	Duty cycle=50%
4	Small signal frequency	f_{SIG}	0.01	-	20	MHz	C_L=220pF
5	Off isolation	V_{ISO}	-	-49	-	dB	f_{SIG}=5MHz, R_L//C_L=1kΩ//15pF
			-	-52	-	dB	f_{SIG}=5MHz, R_L=50Ω
6	Crosstalk	V_{CT}	-	-60	-	dB	f_{SIG}=5MHz, R_L=50Ω
7	Off capacitance to GND	C_{OFF}	-	30	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
8	On capacitance to GND	C_{ON}	-	15	-	pF	V_{SIG}=0V, f_{SIG}=1MHz
9	Output spike voltage	V_{SPK}	-10	90	150	mV	50Ω load

4. Logic Timing

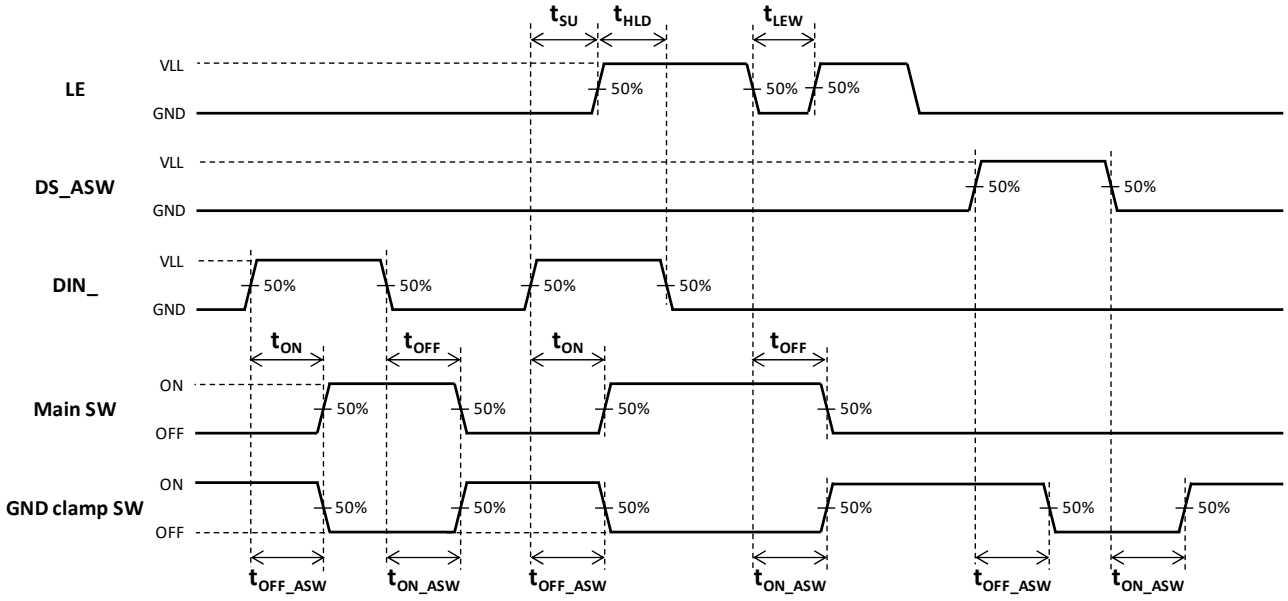

Fig.3 Logic Timing

5. Test Circuits

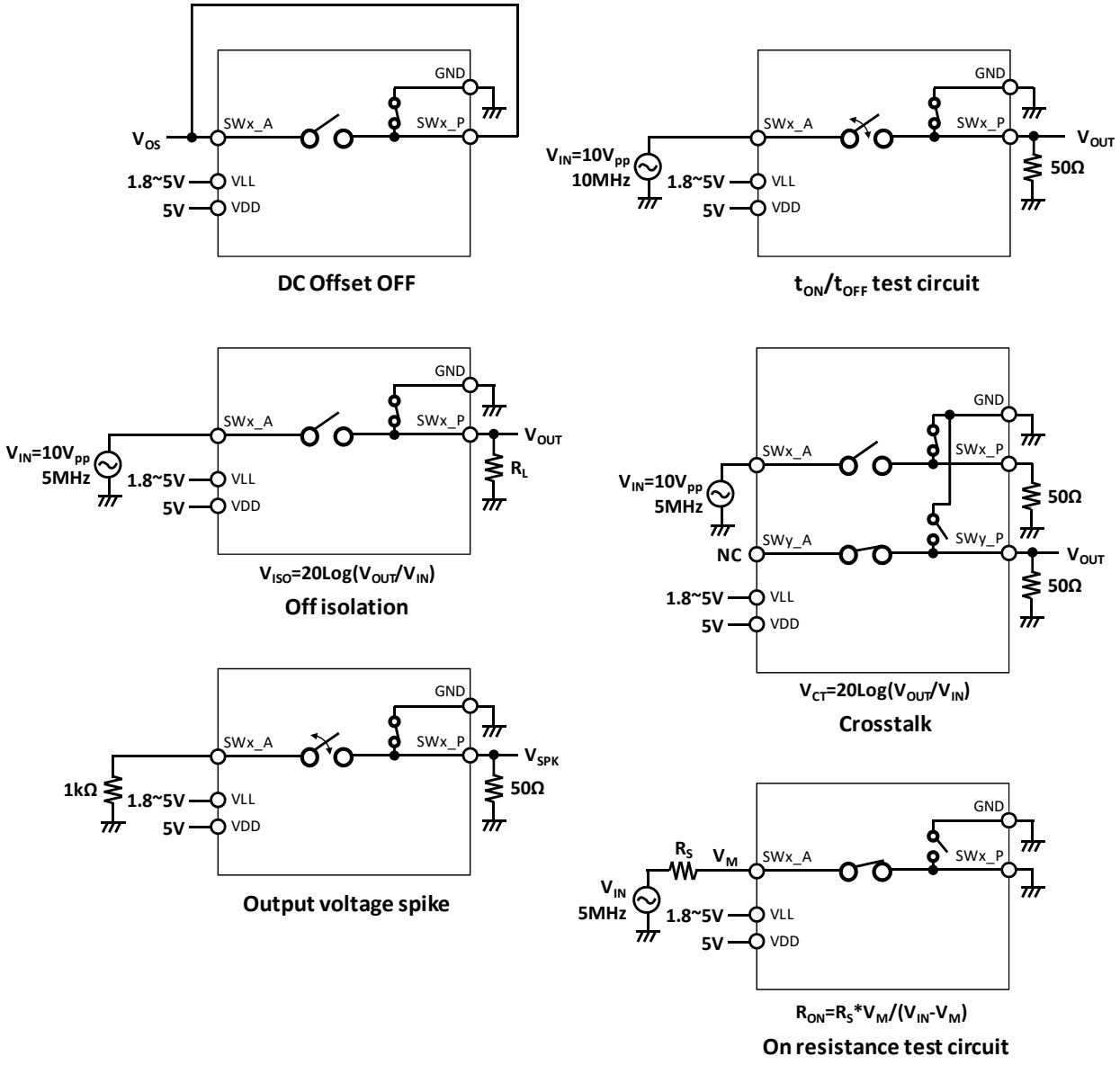

Fig.4 Test Circuits

6. Truth Table

Table 5 Truth table

Logic Inputs						Analog Switch State							
LE	DS_ASW	DIN4	DIN3	DIN2	DIN1	SW13 to SW16		SW9 to SW12		SW5 to SW8		SW1 to SW4	
						Main SW	Clamp SW	Main SW	Clamp SW	Main SW	Clamp SW	Main SW	Clamp SW
0	0	0	0	0	0	OFF	**ON**	OFF	**ON**	OFF	**ON**	OFF	**ON**
0	0	0	0	0	1	OFF	**ON**	OFF	**ON**	OFF	**ON**	**ON**	OFF
0	0	0	0	1	0	OFF	**ON**	OFF	**ON**	**ON**	OFF	OFF	**ON**
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0	0	0	1	0	1	OFF	**ON**	**ON**	OFF	OFF	**ON**	**ON**	OFF
0	0	0	1	1	0	OFF	**ON**	**ON**	OFF	**ON**	OFF	OFF	**ON**
0	0	0	1	1	1	OFF	**ON**	**ON**	OFF	**ON**	OFF	**ON**	OFF
0	0	1	0	0	0	**ON**	OFF	OFF	**ON**	OFF	**ON**	OFF	**ON**
0	0	1	0	0	1	**ON**	OFF	OFF	**ON**	OFF	**ON**	**ON**	OFF
0	0	1	0	1	0	**ON**	OFF	OFF	**ON**	**ON**	OFF	OFF	**ON**
0	0	1	0	1	1	**ON**	OFF	OFF	**ON**	**ON**	OFF	**ON**	OFF
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0	1	1	1	0	1	**ON**	OFF	**ON**	OFF	OFF	OFF	**ON**	OFF
0	1	1	1	1	0	**ON**	OFF	**ON**	OFF	**ON**	OFF	OFF	OFF
0	1	1	1	1	1	**ON**	OFF	**ON**	OFF	**ON**	OFF	**ON**	OFF
1	X	X	X	X	X	Hold Previous State							

7. Pin Configuration

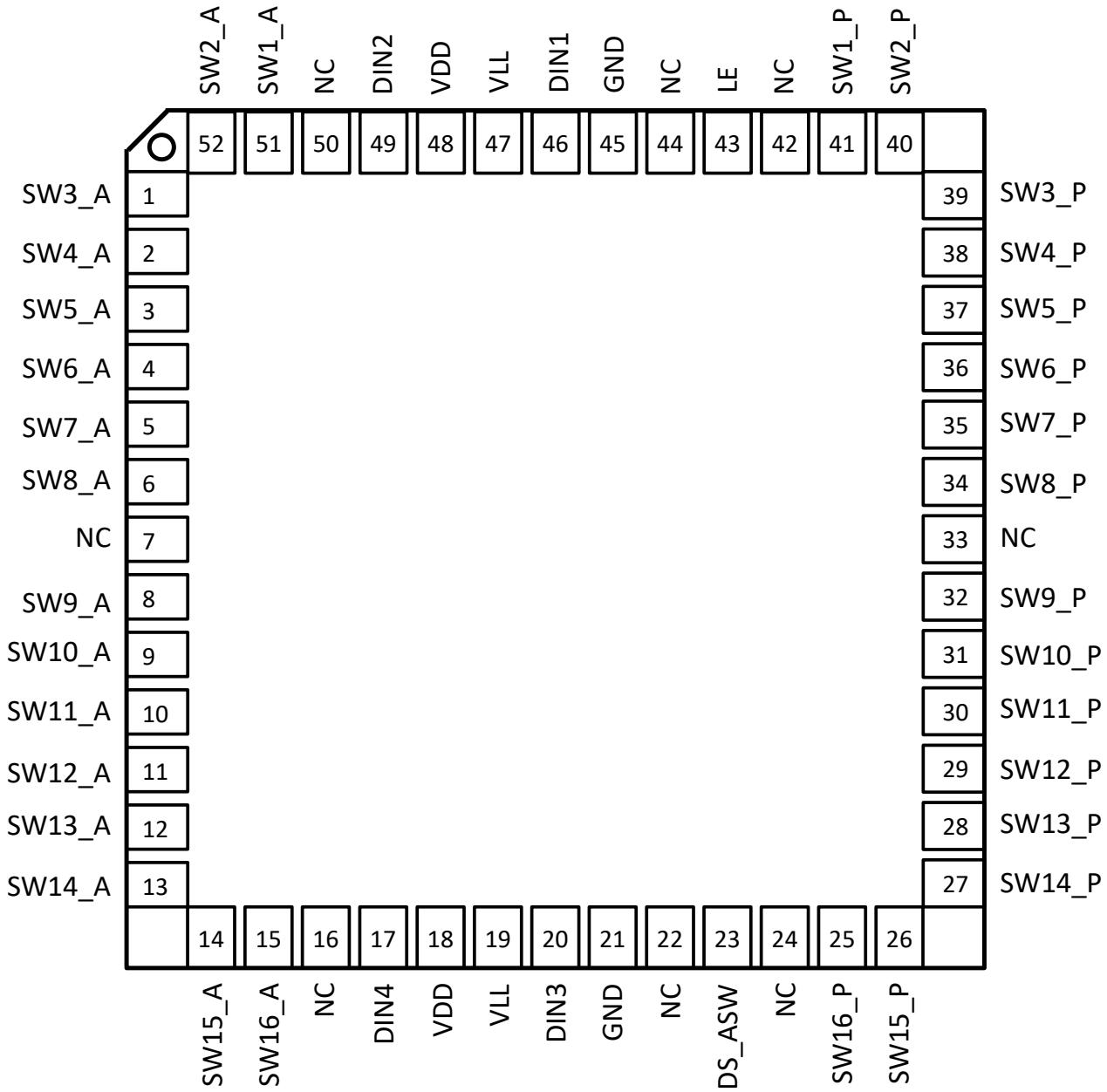

Fig.5 Pin Configuration

Table 6 Pin Configuration

Pin#	Pin Name	I/O	Function
1	SW3_A	I/O	Analog switch terminal 3 (AFE side)
2	SW4_A	I/O	Analog switch terminal 4 (AFE side)
3	SW5_A	I/O	Analog switch terminal 5 (AFE side)
4	SW6_A	I/O	Analog switch terminal 6 (AFE side)
5	SW7_A	I/O	Analog switch terminal 7 (AFE side)
6	SW8_A	I/O	Analog switch terminal 8 (AFE side)
7	NC	-	No connection (Not internally connected)
8	SW9_A	I/O	Analog switch terminal 9 (AFE side)
9	SW10_A	I/O	Analog switch terminal 10 (AFE side)
10	SW11_A	I/O	Analog switch terminal 11 (AFE side)
11	SW12_A	I/O	Analog switch terminal 12 (AFE side)
12	SW13_A	I/O	Analog switch terminal 13 (AFE side)
13	SW14_A	I/O	Analog switch terminal 14 (AFE side)
14	SW15_A	I/O	Analog switch terminal 15 (AFE side)
15	SW16_A	I/O	Analog switch terminal 16 (AFE side)
16	NC	-	No connection (Not internally connected)
17	DIN4	I	Data input 4 for SW13 to SW16, Hi=ON, Low=OFF
18	VDD	-	Positive low voltage power supply (+5V)
19	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
20	DIN3	I	Data input 3 for SW9 to SW12, Hi=ON, Low=OFF
21	GND	-	Drive power ground (0V)
22	NC	-	No connection (Not internally connected)
23	DS_ASW	I	GND clamp control, Hi=always disabled, Low=main switches and GND clamp switches are alternately turned on and off
24	NC	-	No connection (Not internally connected)
25	SW16_P	I/O	Analog switch terminal 16 (Probe side)
26	SW15_P	I/O	Analog switch terminal 15 (Probe side)

Table 6 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
27	SW14_P	I/O	Analog switch terminal 14 (Probe side)
28	SW13_P	I/O	Analog switch terminal 13 (Probe side)
29	SW12_P	I/O	Analog switch terminal 12 (Probe side)
30	SW11_P	I/O	Analog switch terminal 11 (Probe side)
31	SW10_P	I/O	Analog switch terminal 10 (Probe side)
32	SW9_P	I/O	Analog switch terminal 9 (Probe side)
33	NC	-	No connection (Not internally connected)
34	SW8_P	I/O	Analog switch terminal 8 (Probe side)
35	SW7_P	I/O	Analog switch terminal 7 (Probe side)
36	SW6_P	I/O	Analog switch terminal 6 (Probe side)
37	SW5_P	I/O	Analog switch terminal 5 (Probe side)
38	SW4_P	I/O	Analog switch terminal 4 (Probe side)
39	SW3_P	I/O	Analog switch terminal 3 (Probe side)
40	SW2_P	I/O	Analog switch terminal 2 (Probe side)
41	SW1_P	I/O	Analog switch terminal 1 (Probe side)
42	NC	-	No connection (Not internally connected)
43	LE	I	Latch enable input, Hi=Hold data, Low=Latch data input
44	NC	-	No connection (Not internally connected)
45	GND	-	Drive power ground (0V)
46	DIN1	I	Data input 1 for SW1 to SW4, Hi=ON, Low=OFF
47	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
48	VDD	-	Positive low voltage power supply (+5V)
49	DIN2	I	Data input 2 for SW5 to SW8, Hi=ON, Low=OFF
50	NC	-	No connection (Not internally connected)
51	SW1_A	I/O	Analog switch terminal 1 (AFE side)
52	SW2_A	I/O	Analog switch terminal 2 (AFE side)

■ Package

Table 7 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-52(0808)B	QN052-B-P-SD	QFN8x8-B-T-SD	QN052-B-M-S3	QN052-B-L-SD	QN052-B-K-SD

■ Storage, Mounting

1. Storage conditions

1. 1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.

1. 2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering.
It is necessary to check the package surface temperature (resin) before setting the temperature profile.
Figure 6 shows the resistance to soldering heat condition for package (Reflow method).
Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

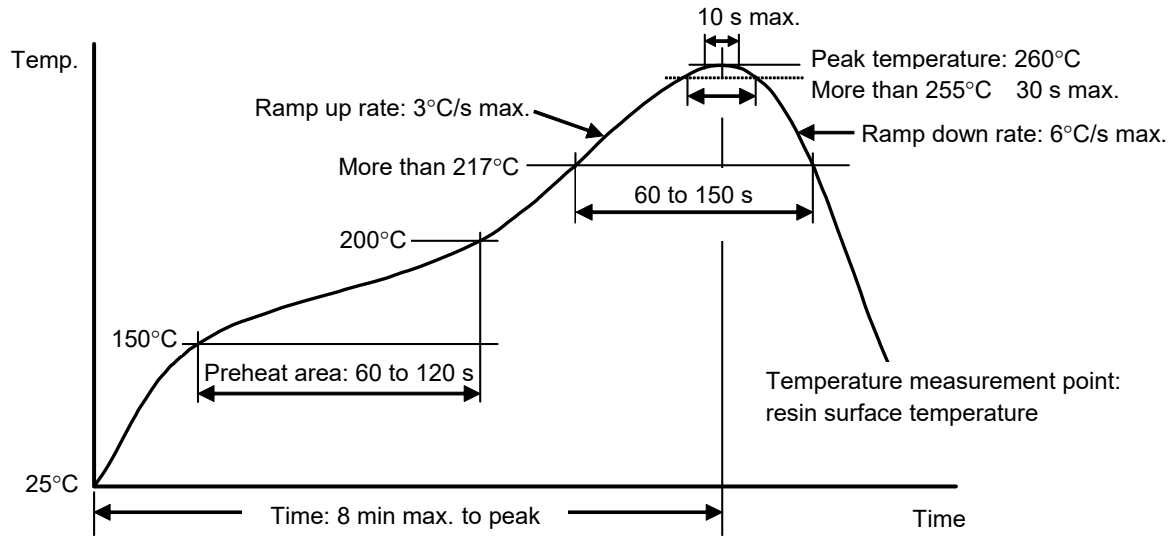

Figure 6 Resistance to Soldering Heat Condition for Package (Reflow Method)

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2. Should any claim be made within one month of product delivery about products’ failure to meet performance described in the Product Specification, all the products in relevant lot(s) shall be re-tested and re-delivered. Products delivered more than one month before such claim shall not be counted for such response.

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■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).

1. 1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.

1. 2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.

1. 3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.

1. 4 Prevent friction with other materials made with high polymer.

1. 5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.

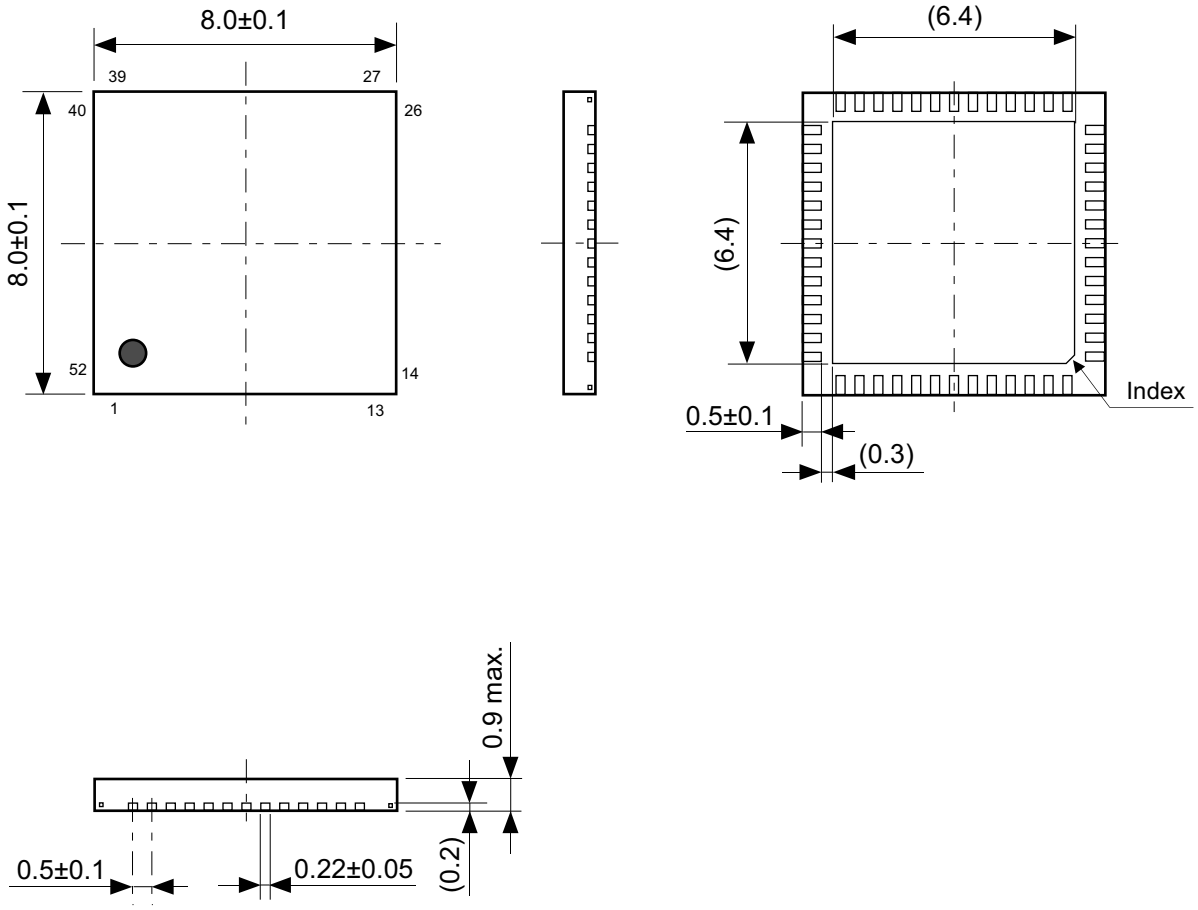
1. 6 Avoid dealing with or storing products in an extremely arid environment.

2. “Absolute maximum ratings” should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.

3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)

4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.

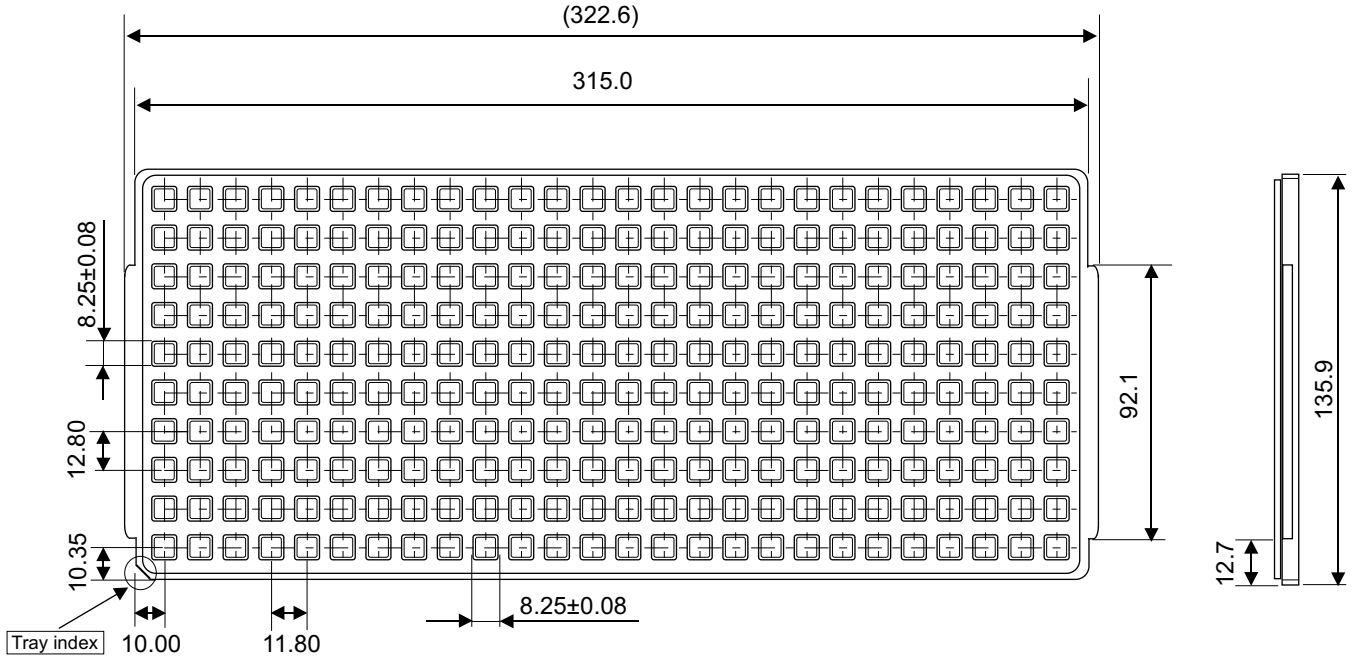
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

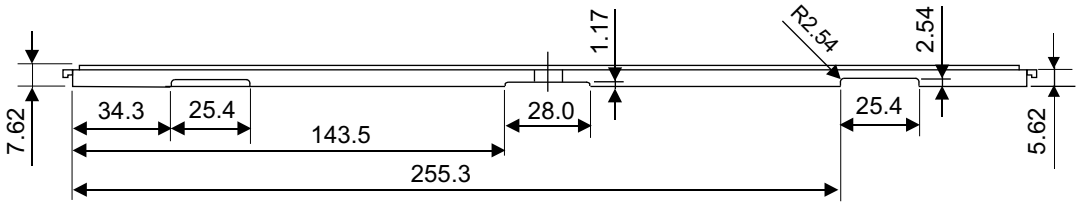


No. QN052-B-P-SD-1.0

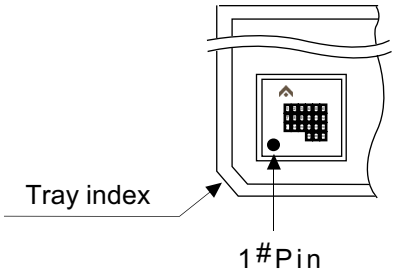
TITLE	QFN52-B-PKG Dimensions
No.	QN052-B-P-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



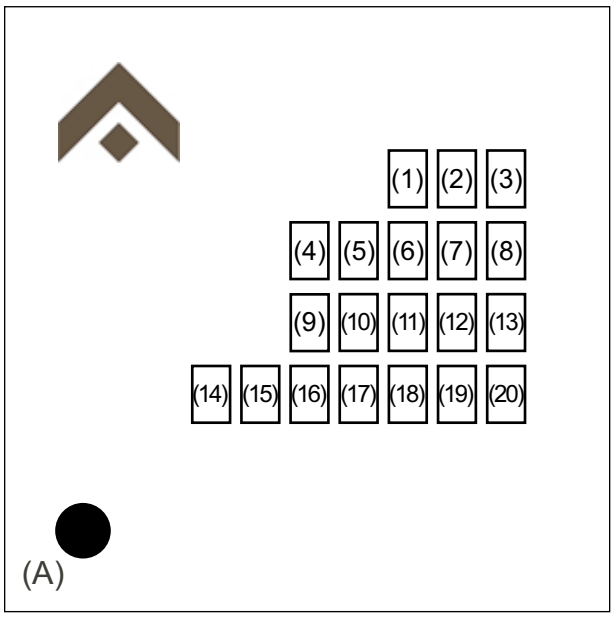


(Direction of IC in tray)



No. QFN8x8-B-T-SD-1.0

TITLE	QFN8x8-B-Tray		
No.	QFN8x8-B-T-SD-1.0		
ANGLE		QTY.	260
UNIT	mm		
	ABLIC Inc.		



(1) : Year of assembly

(2) : Month of assembly

(3) : Week of assembly

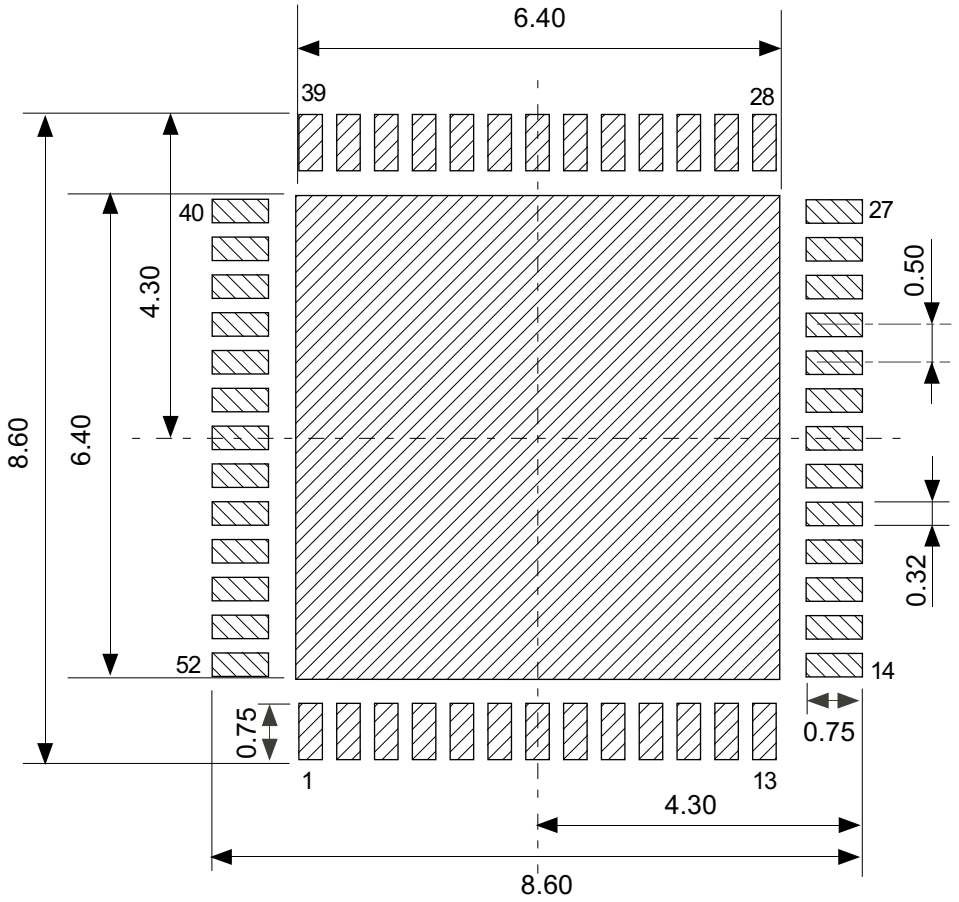
(4) to (13) : Product code

(14) to (20) : Quality control code

(A) : 1-pin mark

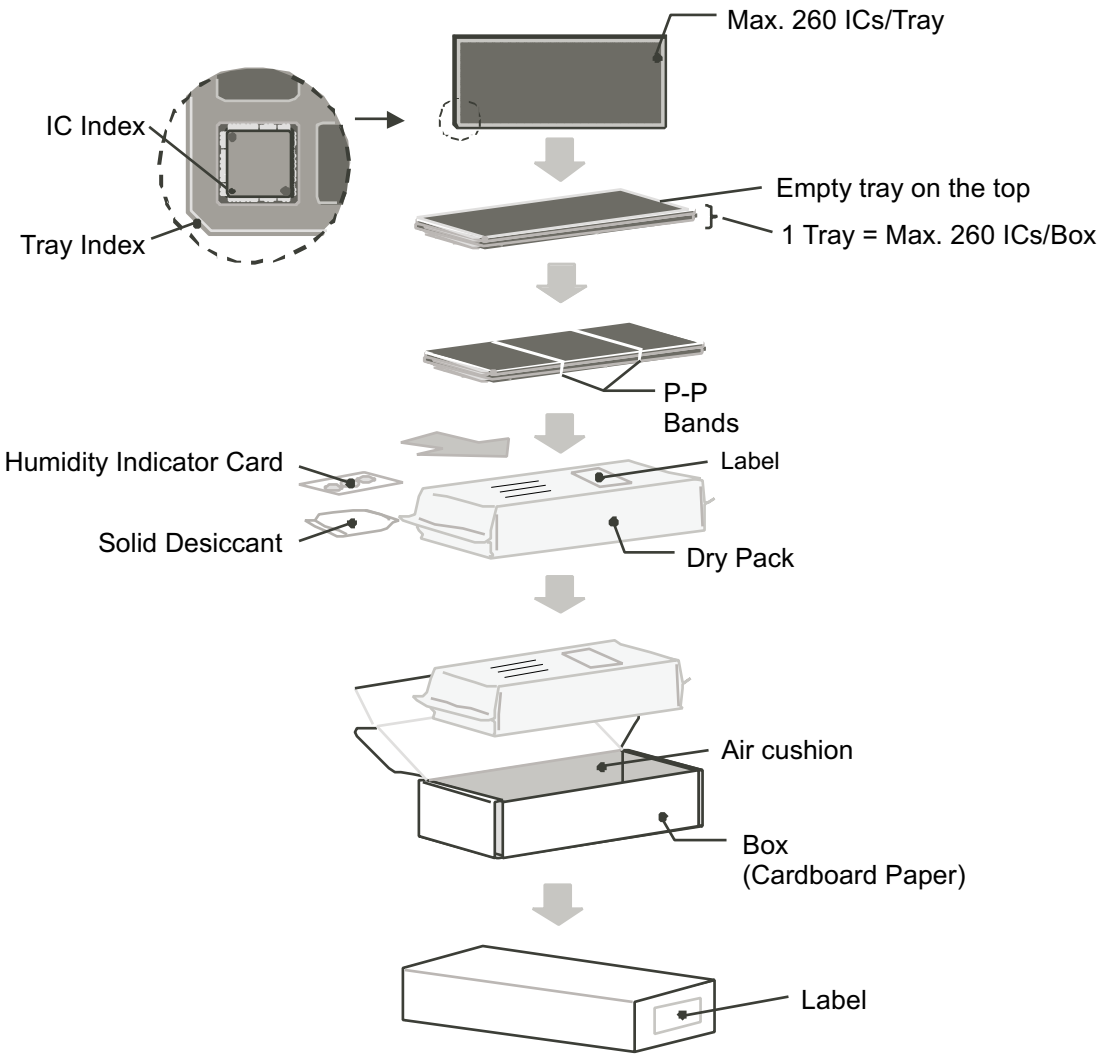
No. QN052-B-M-S3-1.0

TITLE	QFN52-B-Markings (S-UM6502B)		
No.	QN052-B-M-S3-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



No. QN052-B-L-SD-1.0

TITLE	QFN52-B -Land Recommendation
No.	QN052-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN052-B-K-SD-1.0

TITLE	QFN52-B -Packing Procedure
No.	QN052-B-K-SD-1.0
ANGLE	
UNIT	
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