

The ABLIC Inc. HDL6M06522BN is low charge injection 32-channel high-voltage analog switch IC operated only by a single 5V for ultrasound imaging applications.

The HDL6M06522BN consists of single-pole, single-throw (SPST) analog switches controlled by Serial Digital Interface (SDI). The HDL6M06522BN does not require any high-voltage power supply and has a unique pin-out for easy PCB traces. Two different packages are available.

Functions

- 32-channel high-voltage SPST analog switch with active ground clamp

Features

- 0V to $\pm 100\text{V}$ analog signal voltage range (10kHz to 20MHz signal frequency range)
- 2A peak analog signal current per channel
- 8Ω main switch on-resistance
- 40kΩ bleed resistor on probe side
- 32-bit shift registers
- Low on/off-capacitance
- 10pC charge injection to 1000pF
- -52dB off-isolation at 5MHz (load-independent)
- -60dB switch crosstalk
- 35Ω ground clamp switch on probe side alternately turned on/off with main switch
- DS_ASW to disable 35Ω ground clamp switch
- 1.8V to 5V CMOS logic interface
- Single +5V power supply (NO HIGH-VOLTAGE POWER SUPPLY required)
- Low power dissipation (static 5mW)
- Embedded thermal protection flag indicator
- Unique pin configuration for easy PCB traces
- RoHS compliant 84-lead 10x10mm QFN

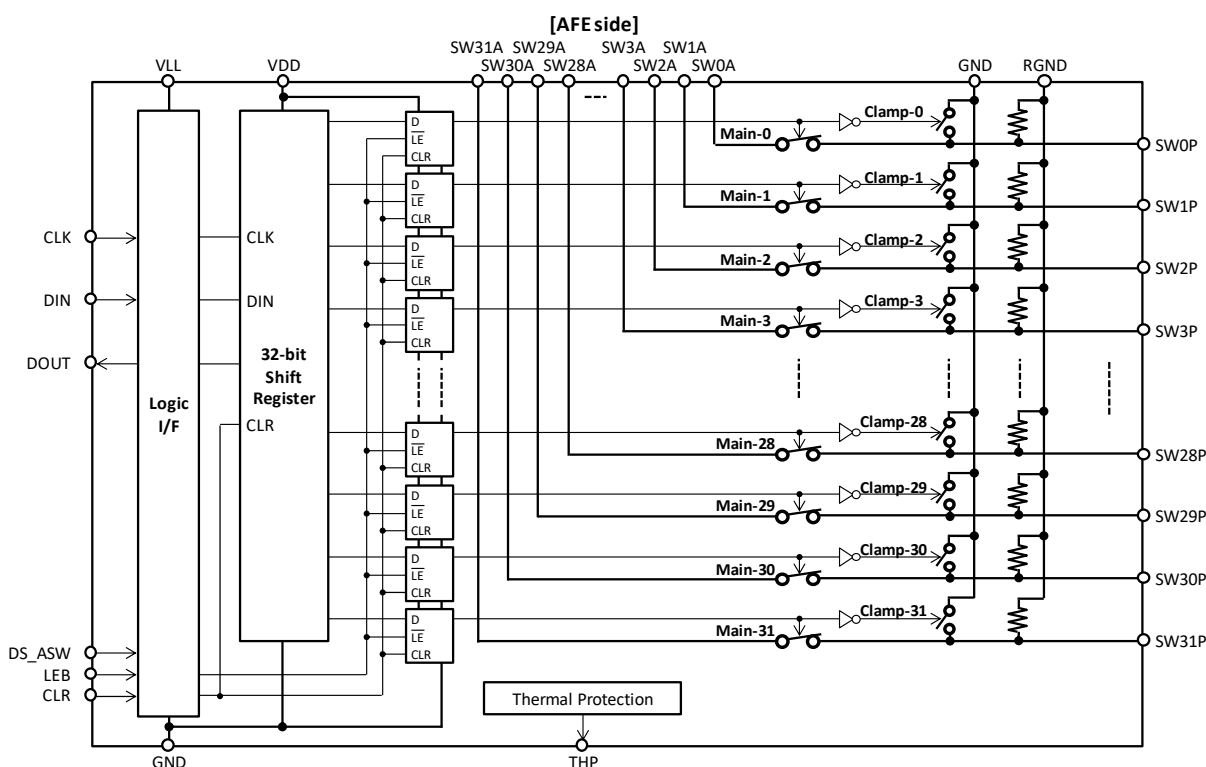


Fig.1 Block Diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Positive logic supply voltage	V _{LL}	-0.4 to +7	V	
2	Positive supply voltage	V _{DD}	-0.4 to +7	V	
3	Logic input voltage	DIN, LEB, CLK, CLR, DS_ASW	-0.4 to +7	V	
4	Logic output voltage	DOUT, THP	-0.4 to +7	V	
5	Analog signal range	V _{SIG}	-105 to +105	V	SW_A
			-105 to +105	V	SW_P when Switch ON
			-2 to +2	V	SW_P when Switch OFF, DS_ASW=0
			-105 to +105	V	SW_P when Switch OFF, DS_ASW=1
6	Peak analog signal current per channel	I _{SW}	2.5	A	
7	Operating junction temperature	T _{Jop}	-20 to +150	°C	
8	Storage temperature	T _{STG}	-55 to +150	°C	
9	Maximum power dissipation	P _{Dmax}	4	W	

NOTE: * Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Application Circuits

2.1 Operating Supply Voltages, Temperature, and Logic Inputs

Table 2 Operating Supply Voltages and Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V _{LL}	1.7	1.8 to 5	V _{DD}	V	
2	Positive supply voltage	V _{DD}	4.75	5	5.25	V	
3	IC substrate voltage *1	V _{SUB}	-	0	-	V	
4	Operating free-air temperature	T _A	0	-	75	°C	
5	High-level logic input voltage	V _{IH}	0.8V _{LL}	-	V _{LL}	V	
6	Low-level logic input voltage	V _{IL}	0	-	0.2V _{LL}	V	
7	Logic input high current *2	I _{IH}	-10	-	10	μA	DIN, LEB, CLK, CLR, DS_ASW
8	Logic input low current	I _{IL}	-10	-	10	μA	
9	Logic input capacitance	C _{IN}	-	2	-	pF	
10	Set up time before LEB rises	t _{SD}	25	-	-	ns	
11	Time width of LEB	t _{WLEB}	12	-	-	ns	
12	Clock delay time to data out	t _{DO}	7	10	-	ns	
13	Time width of CLR	t _{OLR}	55	-	-	ns	
14	Clock frequency	f _{CLK}	-	-	20	MHz	
15	Clock rise and fall times	t _R , t _F	-	-	50	ns	
16	Setup time data to clock	t _{SU}	7	-	-	ns	
17	Hold time data from clock	t _{HLD}	7	-	-	ns	
18	Time width of DS_ASW	t _{WDS_ASW}	10	-	-	μs	

NOTE: *1) Thermal pad on the bottom of the package must be soldered to the ground.

*2) DS_ASW has 100μA leakage at V_{LL}=5V due to 50kΩ internal pull-down resistor.

2.2 Power Supply Sequencing

No power supply sequencing is required even if V_{LL} is different from V_{DD}.

Please apply the V_{DD} voltage to the V_{LL} when operating with a single 5V.

3. Electrical Characteristics

DC Characteristics

Table 3 DC Characteristics

$V_{LL}=3.3V$, $V_{DD}=5V$, $LEB=0$, $DS_ASW=0/1$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Analog signal range	V_{SIG}	-100	-	+100	V	
2	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-1 All main switches off
3	V_{DD} quiescent current	I_{DDQ}	-	1	-	mA	
4	V_{LL} quiescent current	I_{LLQ}	-	0.2	-	μA	Quiescent current-2 All main switches on
5	V_{DD} quiescent current	I_{DDQ}	-	1	-	mA	
6	V_{LL} dynamic current	I_{LL}	-	5	15	μA	Dynamic current All channels switching simultaneously at $f_{sw}=50kHz$
7	V_{DD} dynamic current	I_{DD}	-	2.8	3.8	mA	
8	DC offset main switch off	V_{OS}	-	0	-	mV	$DS_ASW=0$
				0.8	10	mV	$DS_ASW=1$
9	Small signal main switch on-resistance	R_{ONS}	-	8	10	Ω	$V_{SIG}=0.1V_{pp}$ to $5V_{pp}$ @5MHz, $R_S=10\Omega$
10	Small signal main switch on-resistance matching	ΔR_{ONS}	-	2	5	%	$V_{SIG}=0V$, $I_{SIG}=5mA$
11	Large signal main switch on-resistance	R_{ONL}	-	8	-	Ω	$V_{SIG}=20V_{pp}$ @5MHz, $R_S=10\Omega$
12	GND clamp on-resistance	R_{ONCL}	-	35	-	Ω	Main switches off, probe side
13	Shunt resistance	R_{BLD}	30	40	50	k Ω	Probe side
14	Switch output peak current	I_{SW}	-	2	-	A	100ns pulse, 0.1% duty cycle

Thermal Protection

Table 4 Thermal Protection Characteristics

$V_{LL}=3.3V$, $V_{DD}=5V$, $LEB=0$, $DS_ASW=0/1$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, $V_{LL}=3.3V$, $I_{THP}=1mA$
4	THP temperature threshold	T_{THP}	90	110	130	$^{\circ}C$	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	$^{\circ}C$	

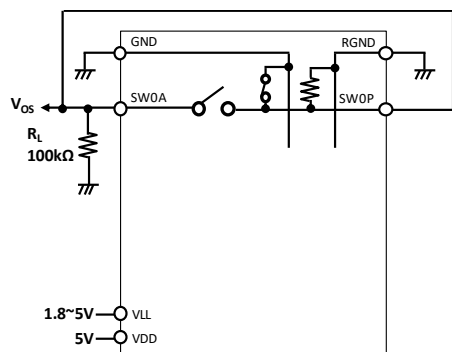
AC Characteristics

Table 5 AC Characteristics

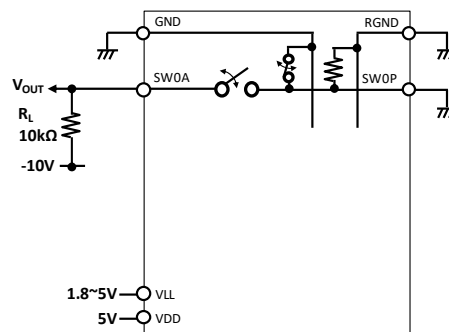
$V_{LL}=3.3V$, $V_{DD}=5V$, $LEB=0$, $DS_ASW=0/1$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Turn-on time	t_{ON}	-	2	5	μs	
		t_{ON_ASW}	-	2	5	μs	
2	Turn-off time	t_{OFF}	-	2	5	μs	
		t_{OFF_ASW}	-	2	5	μs	
3	Output switching frequency	f_{SW}	-	-	50	kHz	Duty cycle=50%
4	Small signal frequency	f_{SIG}	0.01	-	20	MHz	$C_L=220pF$
5	Off isolation	V_{ISO}	-	-53	-	dB	$f_{SIG}=5MHz$, $R_L/C_L=1k\Omega/15pF$, $DS_ASW=0$
			-	-57	-	dB	$f_{SIG}=5MHz$, $R_L=50\Omega$, $DS_ASW=0$
			-	-25	-	dB	$f_{SIG}=5MHz$, $R_L/C_L=1k\Omega/15pF$, $DS_ASW=1$
			-	-49	-	dB	$f_{SIG}=5MHz$, $R_L=50\Omega$, $DS_ASW=1$
6	Crosstalk	V_{CT}	-	-60	-	dB	$f_{SIG}=5MHz$, $R_L=50\Omega$
7	Off capacitance SW_P to GND	$C_{OFF(SWP)}$	-	10	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=0$
			-	12	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=1$
8	Off capacitance SW_A to GND	$C_{OFF(SWA)}$	-	30	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=0$
			-	10	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=1$
9	On capacitance SW_P to GND	$C_{ON(SWP)}$	-	15	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=0$
			-	15	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=1$
10	On capacitance SW_A to GND	$C_{ON(SWA)}$	-	15	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=0$
			-	15	-	pF	$V_{SIG}=0V$, $f_{SIG}=1MHz$, $DS_ASW=1$
11	Output spike voltage (SW_P)	$V_{SPK_ON(SWP)}$	-15	60	90	mV	50Ω load @switch on, $DS_ASW=0$
			-15	80	120	mV	50Ω load @switch on, $DS_ASW=1$
		$V_{SPK_OFF(SWP)}$	-15	100	150	mV	50Ω load @switch off, $DS_ASW=0$
			-15	100	150	mV	50Ω load @switch off, $DS_ASW=1$
12	Output spike voltage (SW_A)	$V_{SPK_ON(SWA)}$	-15	60	90	mV	50Ω load @switch on, $DS_ASW=0$
			-15	80	120	mV	50Ω load @switch on, $DS_ASW=1$
		$V_{SPK_OFF(SWA)}$	-15	100	150	mV	50Ω load @switch off, $DS_ASW=0$
			-15	100	150	mV	50Ω load @switch off, $DS_ASW=1$
13	Charge injection	QC	-	10	-	pC	

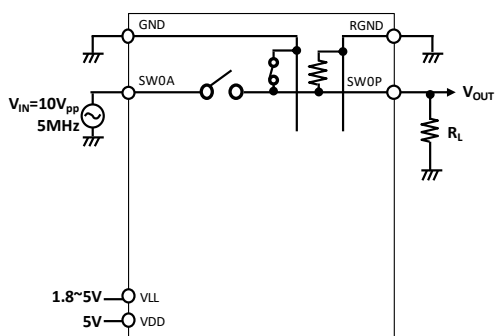
4. Test Circuits



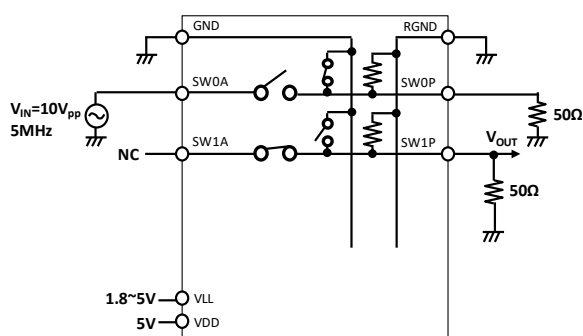
DC Offset OFF



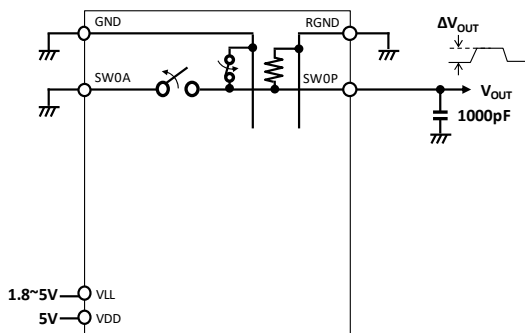
t_{ON}/t_{OFF} test circuit



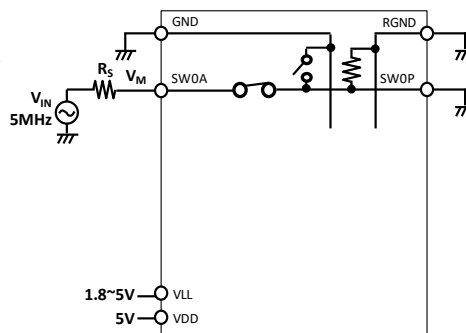
$V_{ISO}=20\text{Log}(V_{OUT}/V_{IN})$
Off isolation



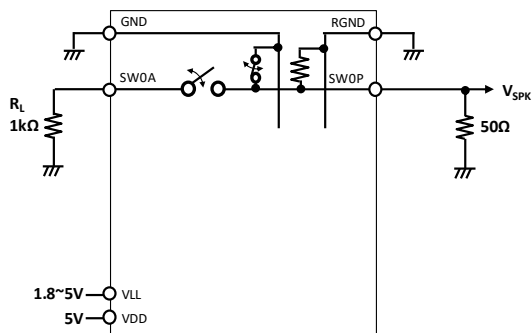
$V_{CT}=20\text{Log}(V_{OUT}/V_{IN})$
Crosstalk



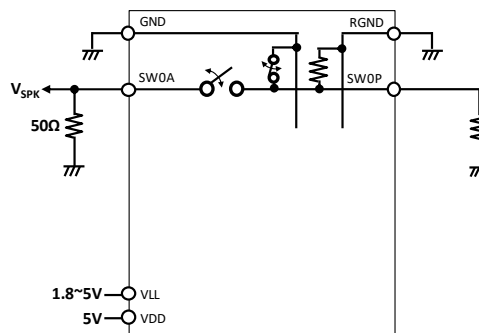
$Q=1000\text{pF} \cdot \Delta V_{OUT}$
Charge Injection



$R_{ON}=R_S \cdot V_M / (V_{IN}-V_M)$
On resistance test circuit



Output spike voltage SW_P



Output spike voltage SW_A

Fig.2 Test Circuits

5. Truth Table

Table 6 Truth Table

Logic Inputs										Analog Switch State											
LEB	CLR	DS_ASW	DIN							SW0		SW1		...	SW15		SW16		...	SW31	
			D0	D1	...	D15	D16	...	D31	Main SW	Clamp SW	Main SW	Clamp SW		Main SW	Clamp SW	Main SW	Clamp SW		Main SW	Clamp SW
L	L	L	L	-		-	-		-	OFF	ON	-	-		-	-	-	-		-	-
L	L	L	H	-		-	-		-	ON	OFF	-	-		-	-	-	-		-	-
L	L	L	-	L		-	-		-	-	-	OFF	ON		-	-	-	-		-	-
L	L	L	-	H		-	-		-	-	-	ON	OFF		-	-	-	-		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		L	-		-	-	-	-	-		OFF	ON	-	-		-	-
L	L	L	-	-		H	-		-	-	-	-	-		ON	OFF	-	-		-	-
L	L	L	-	-		-	L		-	-	-	-	-		-	-	OFF	ON		-	-
L	L	L	-	-		-	H		-	-	-	-	-		-	-	ON	OFF		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-		-	-	-	-	-		-	-	-	-		-	-
L	L	L	-	-		-	-		L	-	-	-	-		-	-	-	-		OFF	ON
L	L	L	-	-		-	-		H	-	-	-	-		-	-	-	-		ON	OFF
L	L	H	L	-		-	-		-	OFF	OFF	-	-		-	-	-	-		-	-
L	L	H	H	-		-	-		-	ON	OFF	-	-		-	-	-	-		-	-
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L	L	H	-	-		-	-		H	-	-	-	-		-	-	-	-		ON	OFF
H	L	X	X	X	X	X	X	X	X	Hold Previous State											
X	H	X	X	X	X	X	X	X	X	ALL "Main SWs" OFF											

6. Logic Timing

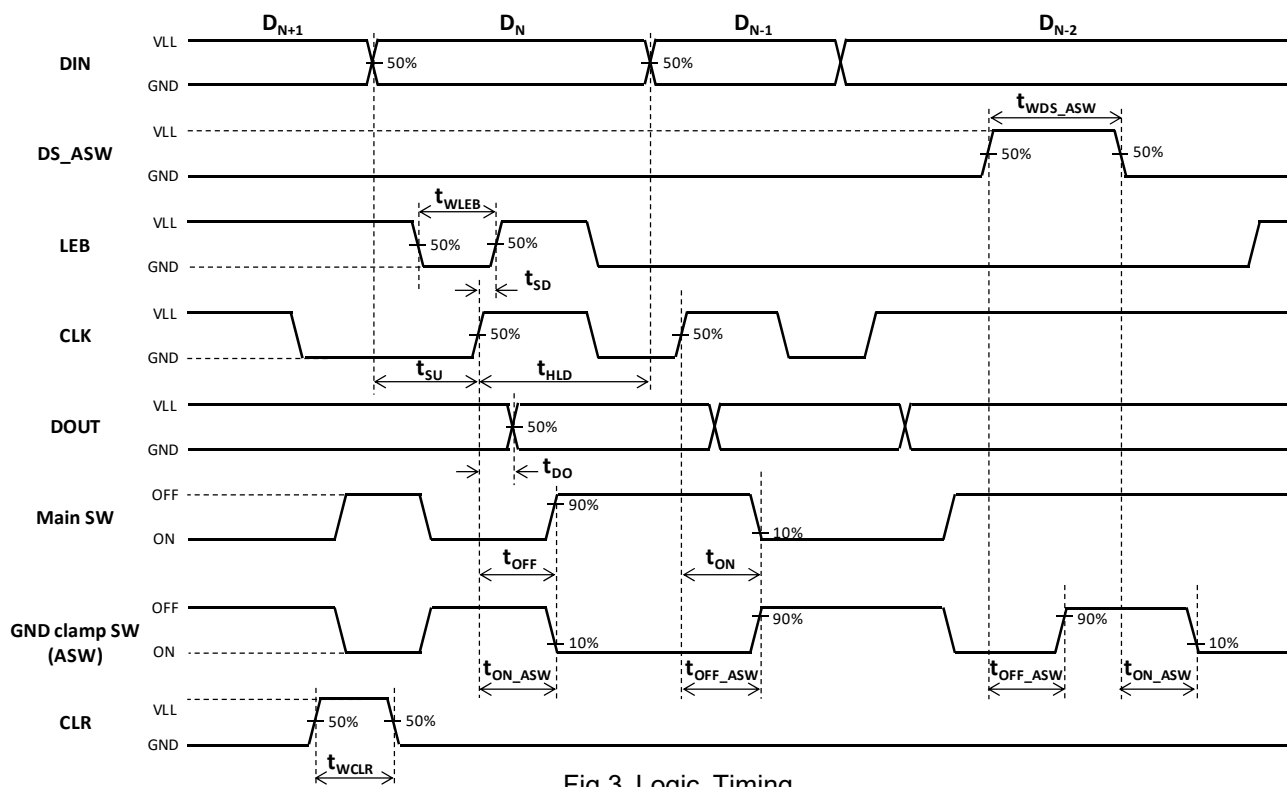


Fig.3 Logic Timing

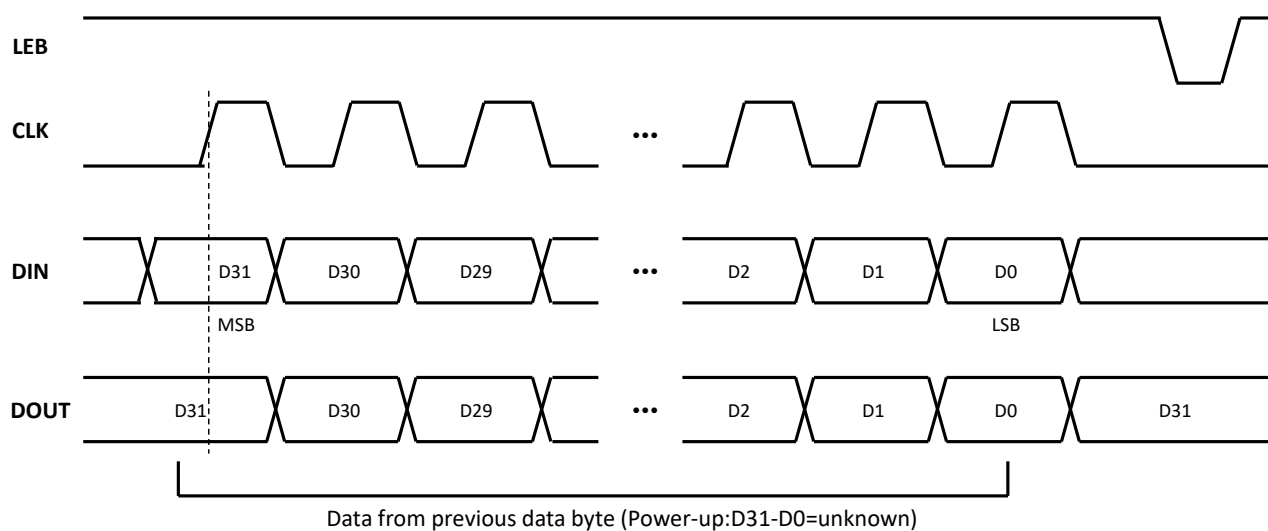


Fig.4 Latch Enable Interface Timing

Table 7 Pin Configuration

Pin#	Pin Name	I/O	Function
1	DIN	I	Serial-Data input
2	GND	-	Drive power ground (0V)
3	SW0A	I/O	Analog switch terminal 0 (AFE side)
4	SW1A	I/O	Analog switch terminal 1 (AFE side)
5	SW2A	I/O	Analog switch terminal 2 (AFE side)
6	SW3A	I/O	Analog switch terminal 3 (AFE side)
7	SW4A	I/O	Analog switch terminal 4 (AFE side)
8	SW5A	I/O	Analog switch terminal 5 (AFE side)
9	SW6A	I/O	Analog switch terminal 6 (AFE side)
10	SW7A	I/O	Analog switch terminal 7 (AFE side)
11	NC	-	No connection (Not internally connected)
12	SW24A	I/O	Analog switch terminal 24 (AFE side)
13	SW25A	I/O	Analog switch terminal 25 (AFE side)
14	SW26A	I/O	Analog switch terminal 26 (AFE side)
15	SW27A	I/O	Analog switch terminal 27 (AFE side)
16	SW28A	I/O	Analog switch terminal 28 (AFE side)
17	SW29A	I/O	Analog switch terminal 29 (AFE side)
18	SW30A	I/O	Analog switch terminal 30 (AFE side)
19	SW31A	I/O	Analog switch terminal 31 (AFE side)
20	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
21	DOUT	O	Serial-Data output
22	CLK	I	Serial-Clock input
23	RGND	-	Bleed resistor ground (0V)
24	SW31P	I/O	Analog switch terminal 31 (Probe side)
25	SW30P	I/O	Analog switch terminal 30 (Probe side)
26	SW29P	I/O	Analog switch terminal 29 (Probe side)
27	SW28P	I/O	Analog switch terminal 28 (Probe side)
28	SW27P	I/O	Analog switch terminal 27 (Probe side)
29	SW26P	I/O	Analog switch terminal 26 (Probe side)
30	SW25P	I/O	Analog switch terminal 25 (Probe side)
31	SW24P	I/O	Analog switch terminal 24 (Probe side)
32	NC	-	No connection (Not internally connected)
33	SW23P	I/O	Analog switch terminal 23 (Probe side)
34	SW22P	I/O	Analog switch terminal 22 (Probe side)
35	SW21P	I/O	Analog switch terminal 21 (Probe side)
36	SW20P	I/O	Analog switch terminal 20 (Probe side)
37	SW19P	I/O	Analog switch terminal 19 (Probe side)
38	SW18P	I/O	Analog switch terminal 18 (Probe side)
39	SW17P	I/O	Analog switch terminal 17 (Probe side)
40	SW16P	I/O	Analog switch terminal 16 (Probe side)
41	VDD	-	Positive low voltage power supply (+5V)
42	CLR	I	Shift register and latch clear input

Table 7 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
43	DS_ASW	I	GND clamp control, Hi=always disabled, Low=main switches and GND clamp switches are alternately turned on and off
44	GND	-	Drive power ground (0V)
45	SW16A	I/O	Analog switch terminal 16 (AFE side)
46	SW17A	I/O	Analog switch terminal 17 (AFE side)
47	SW18A	I/O	Analog switch terminal 18 (AFE side)
48	SW19A	I/O	Analog switch terminal 19 (AFE side)
49	SW20A	I/O	Analog switch terminal 20 (AFE side)
50	SW21A	I/O	Analog switch terminal 21 (AFE side)
51	SW22A	I/O	Analog switch terminal 22 (AFE side)
52	SW23A	I/O	Analog switch terminal 23 (AFE side)
53	NC	-	No connection (Not internally connected)
54	SW8A	I/O	Analog switch terminal 8 (AFE side)
55	SW9A	I/O	Analog switch terminal 9 (AFE side)
56	SW10A	I/O	Analog switch terminal 10 (AFE side)
57	SW11A	I/O	Analog switch terminal 11 (AFE side)
58	SW12A	I/O	Analog switch terminal 12 (AFE side)
59	SW13A	I/O	Analog switch terminal 13 (AFE side)
60	SW14A	I/O	Analog switch terminal 14 (AFE side)
61	SW15A	I/O	Analog switch terminal 15 (AFE side)
62	VLL	-	Positive voltage supply of low voltage interface (+1.8V~+5V)
63	THP	O	Thermal protection output flag, open N-MOS drain
64	GND	-	Drive power ground (0V)
65	RGND	-	Bleed resistor ground (0V)
66	SW15P	I/O	Analog switch terminal 15 (Probe side)
67	SW14P	I/O	Analog switch terminal 14 (Probe side)
68	SW13P	I/O	Analog switch terminal 13 (Probe side)
69	SW12P	I/O	Analog switch terminal 12 (Probe side)
70	SW11P	I/O	Analog switch terminal 11 (Probe side)
71	SW10P	I/O	Analog switch terminal 10 (Probe side)
72	SW9P	I/O	Analog switch terminal 9 (Probe side)
73	SW8P	I/O	Analog switch terminal 8 (Probe side)
74	NC	-	No connection (Not internally connected)
75	SW7P	I/O	Analog switch terminal 7 (Probe side)
76	SW6P	I/O	Analog switch terminal 6 (Probe side)
77	SW5P	I/O	Analog switch terminal 5 (Probe side)
78	SW4P	I/O	Analog switch terminal 4 (Probe side)
79	SW3P	I/O	Analog switch terminal 3 (Probe side)
80	SW2P	I/O	Analog switch terminal 2 (Probe side)
81	SW1P	I/O	Analog switch terminal 1 (Probe side)
82	SW0P	I/O	Analog switch terminal 0 (Probe side)
83	VDD	-	Positive low voltage power supply (+5V)
84	LEB	I	Active-Low latch enable input, Hi=Hold data, Low=Latch data input

■ Package

Table 8 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-84(1010)B	QN084-B-P-SD	QFN10x10-T-SD	QN084-B-M-S1	QN084-B-L-SD	QN084-B-K-SD

■ Storage, Mounting

1. Storage conditions

- 1.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.
- 1.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering. It is necessary to check the package surface temperature (resin) before setting the temperature profile.

Figure 6 shows the resistance to soldering heat condition for package (Reflow method).

Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

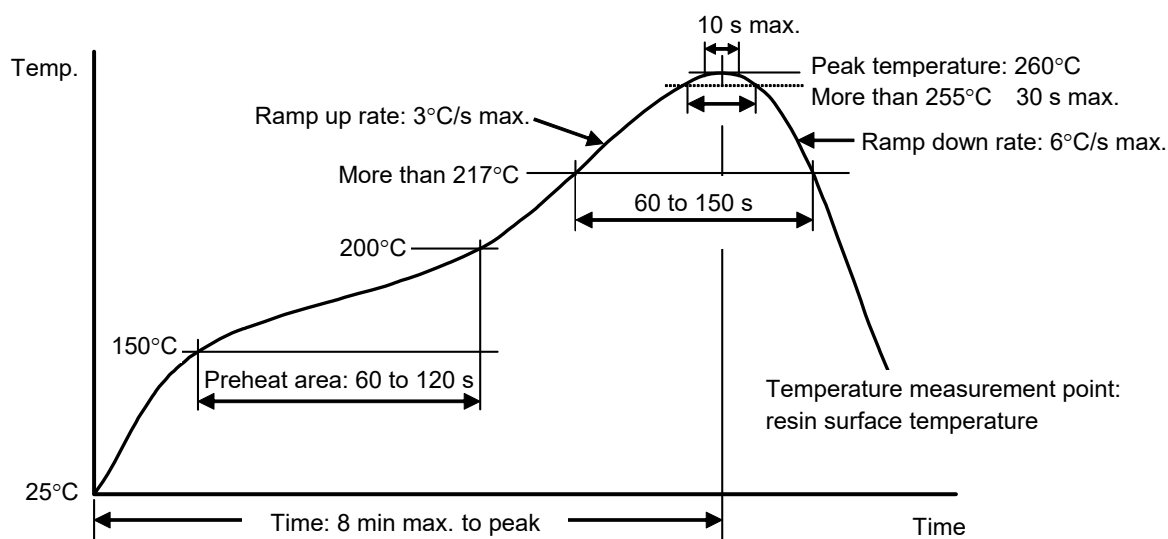


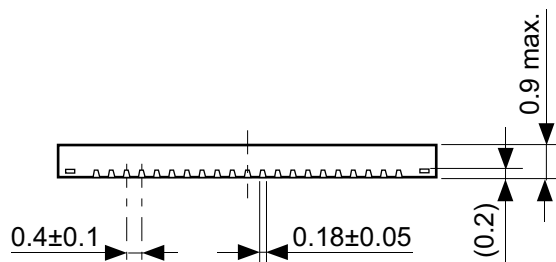
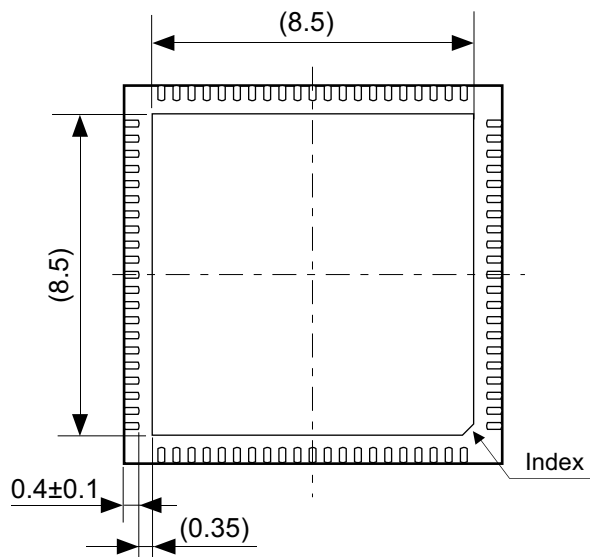
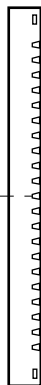
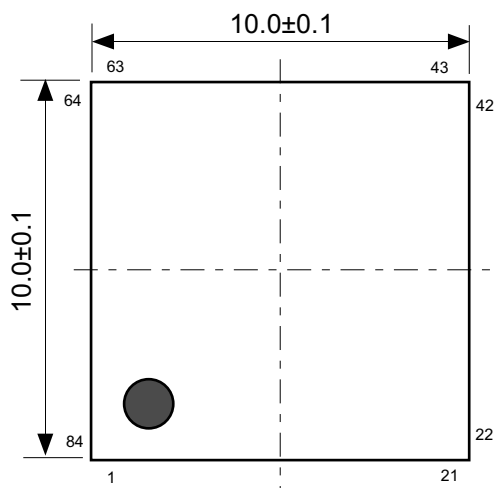
Figure 6 Resistance to Soldering Heat Condition for Package (Reflow Method)

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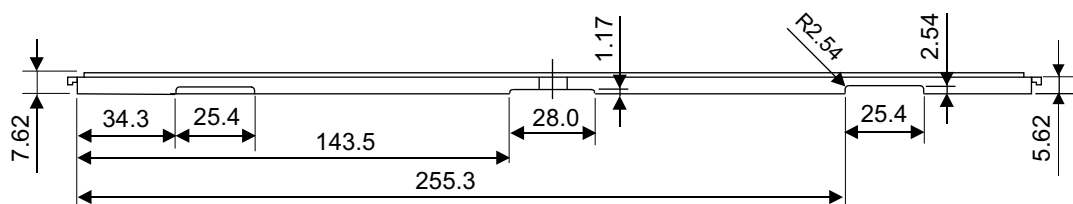
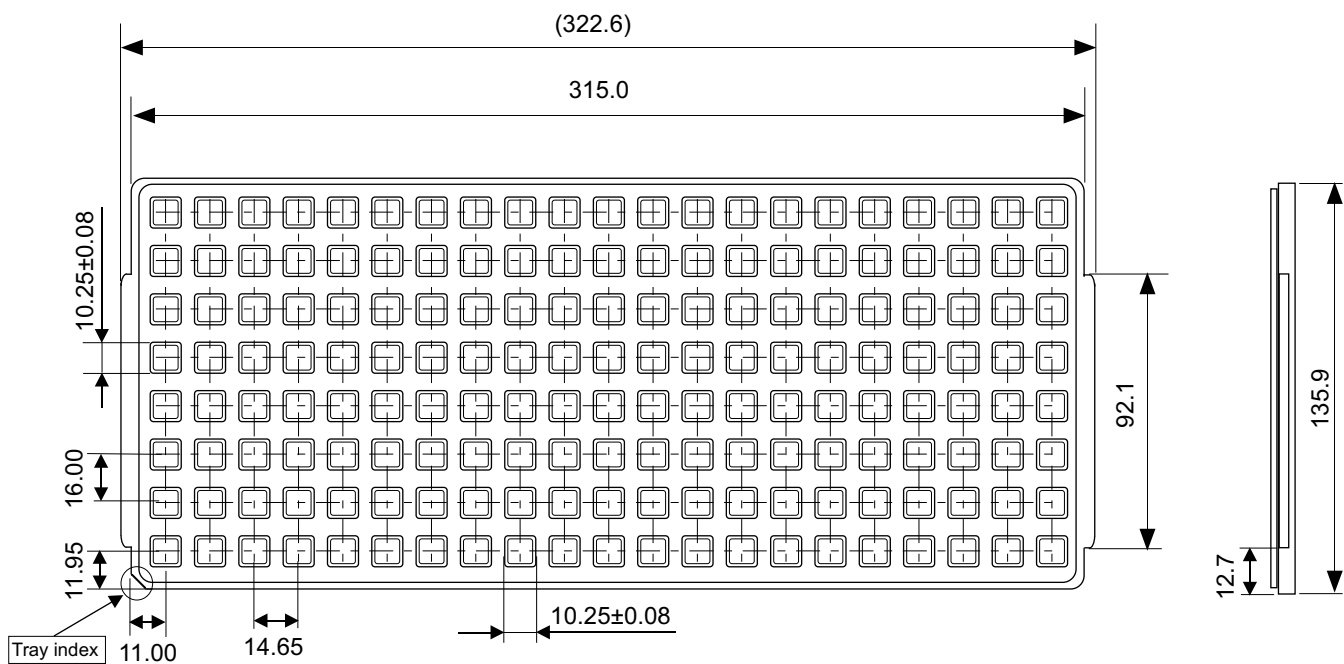
■ Cautions

1. Customers are advised to follow the cautions below to protect products from damage caused by electrical static discharge (ESD).
 - 1.1 Material of container or any device to carry products should be free from ESD, which may be caused by vibration while transportation. It is recommended that electric-conductive container or aluminum sheet be used as an effective countermeasure.
 - 1.2 Those that touch products, such as work platform, machine, or measurement/test equipment, should be grounded.
 - 1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
 - 1.4 Prevent friction with other materials made with high polymer.
 - 1.5 Prevent vibration or friction when carrying the printed circuit board (PCB) where products are mounted. To short circuit terminals is a recommended countermeasure to keep the same electric potential on the PCB.
 - 1.6 Avoid dealing with or storing products in an extremely arid environment.
2. "Absolute maximum ratings" should never be exceeded during use regardless of any change in external conditions. Otherwise, products may be damaged or destroyed. In no event shall ABLIC Inc. be liable for any failure in products or any secondary damage resulting from use at a value exceeding the absolute maximum ratings.
3. Products may experience failures due to accident or unexpected surge voltages. Accordingly, adopt safe design features, such as redundancy or prevention of erroneous action, to avoid extensive damage in the event of a failure. (If a semiconductor device fails, there may be cases in which the semiconductor device, wiring or wiring pattern will emit smoke or cause a fire or in which the semiconductor device will burst.)
4. Products may experience failures or malfunction in poor surroundings, such as electrical leakage in products due to long-term use in high humidity, malfunctioning or permanent damage due to chemical reaction of products in corrosive environment or due to discharge by strongly charged object near products or due to excessive mechanical shock. To use products in radiation environment is not assumed. To use products near material easy to ignite may cause a fire due to its flammable package. Avoid using products in such environment or take appropriate countermeasures depending on the environment.
5. Products are not designed, manufactured, or warranted to be suitable for use where extremely high reliability is required (such as use in nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment). Inclusion of products in such application shall be fully at the risk of customers. ABLIC Inc. assumes no liability for applications assistance, customer product design, or performance.

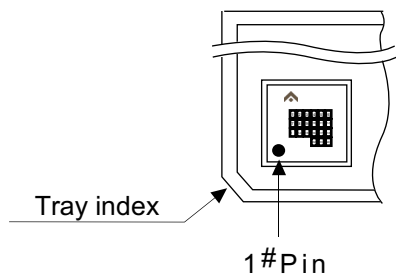


No. QN084-B-P-SD-2.0

TITLE	QFN84-B-PKG Dimensions
No.	QN084-B-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

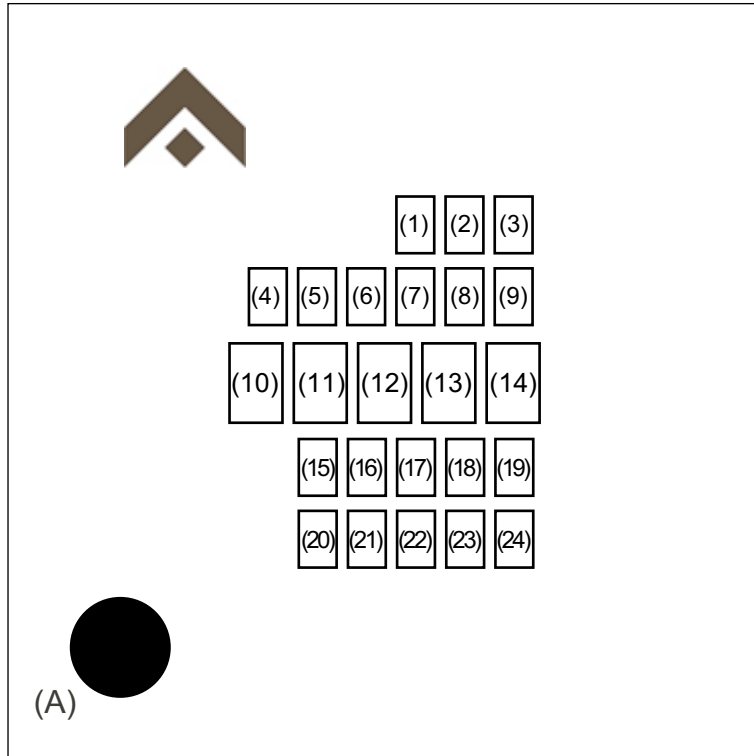


(Direction of IC in tray)



No. QFN10x10-T-SD-1.0

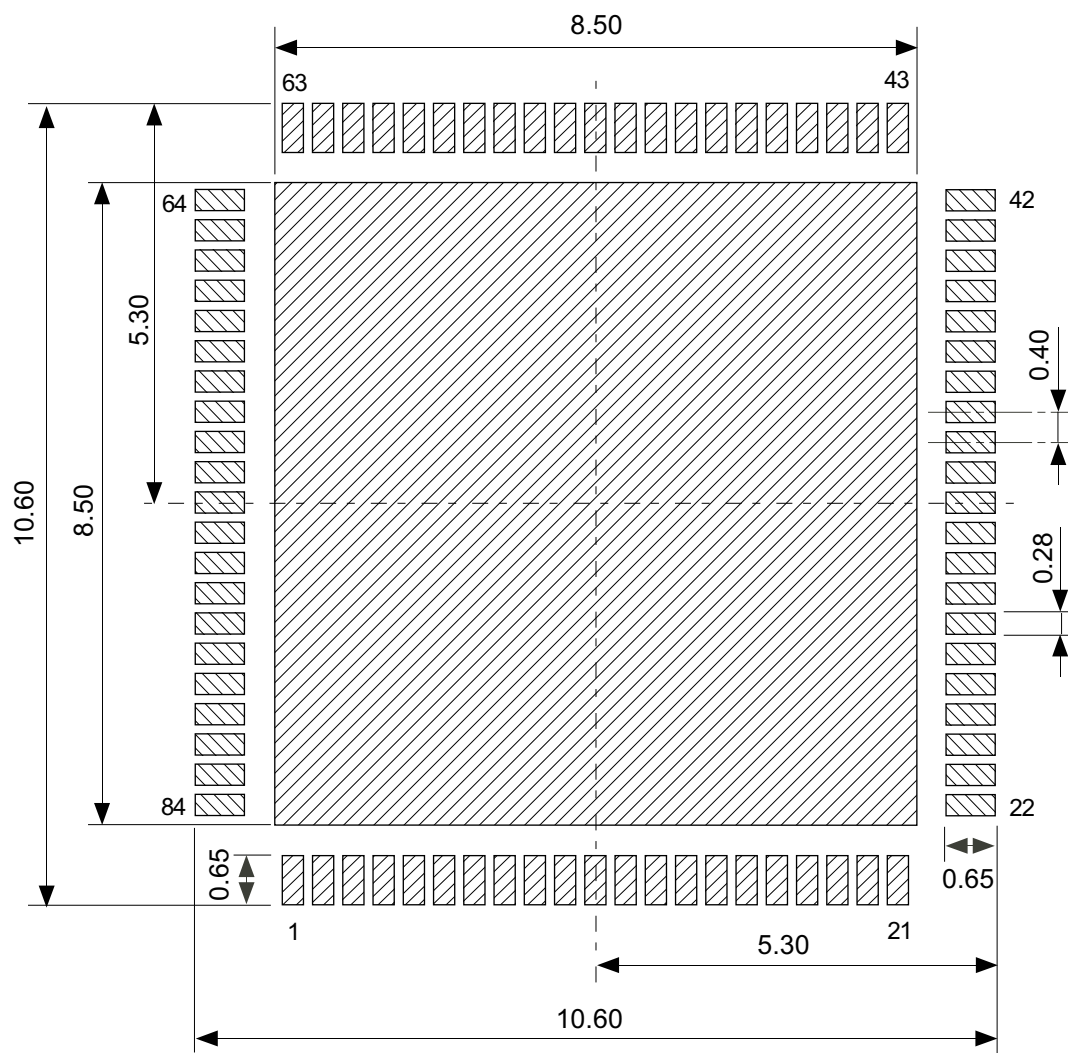
TITLE	QFN10x10-B-Tray		
No.	QFN10x10-T-SD-1.0		
ANGLE		QTY.	168
UNIT	mm		
ABLIC Inc.			



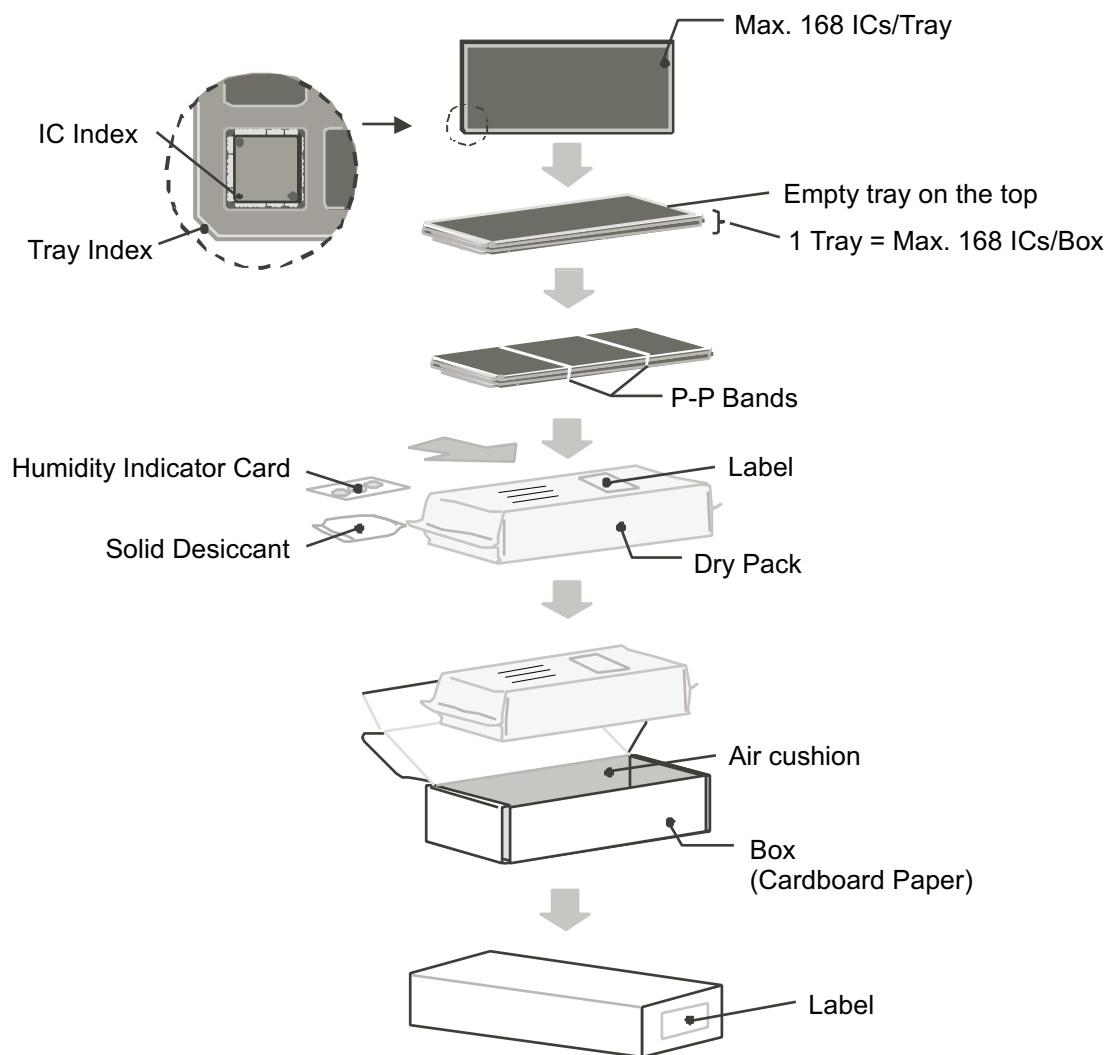
- (1) : Year of assembly
 (2) : Month of assembly
 (3) : Week of assembly
 (4) to (14) : Product code
 (15) to (24) : Quality control code
 (A) : 1-pin mark

No. QFN84-B-M-S1-1.0

TITLE	QFN84-B-Markings (S-UM6522BN)		
No.	QN084-B-M-S1-1.0		
ANGLE			
UNIT		TYPE	LASER
ABLIC Inc.			



TITLE	QFN84-B -Land Recommendation
No.	QN084-B-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN084-B-K-SD-1.0

TITLE	QFN84-B -Packing Procedure
No.	QN084-B-K-SD-1.0
ANGLE	
UNIT	
ABLIC Inc.	

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The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
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2.4-2019.07