HEF4020B

14-stage binary counter

Rev. 12 — 8 August 2024 Product data sheet

1. General description

The HEF4020B is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and 12 buffered parallel outputs (Q0, and Q3 to Q13). The counter advances on the HIGH-to-LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of $\overline{CP}$. Each counter stage is a static toggle flip-flop. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- High speed operation
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4020BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

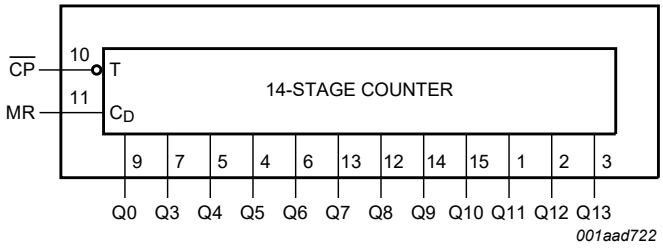


Fig. 1. Functional diagram

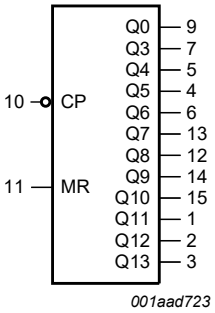


Fig. 2. Logic symbol

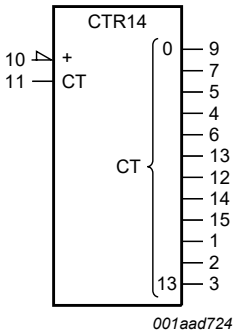


Fig. 3. IEC Logic symbol

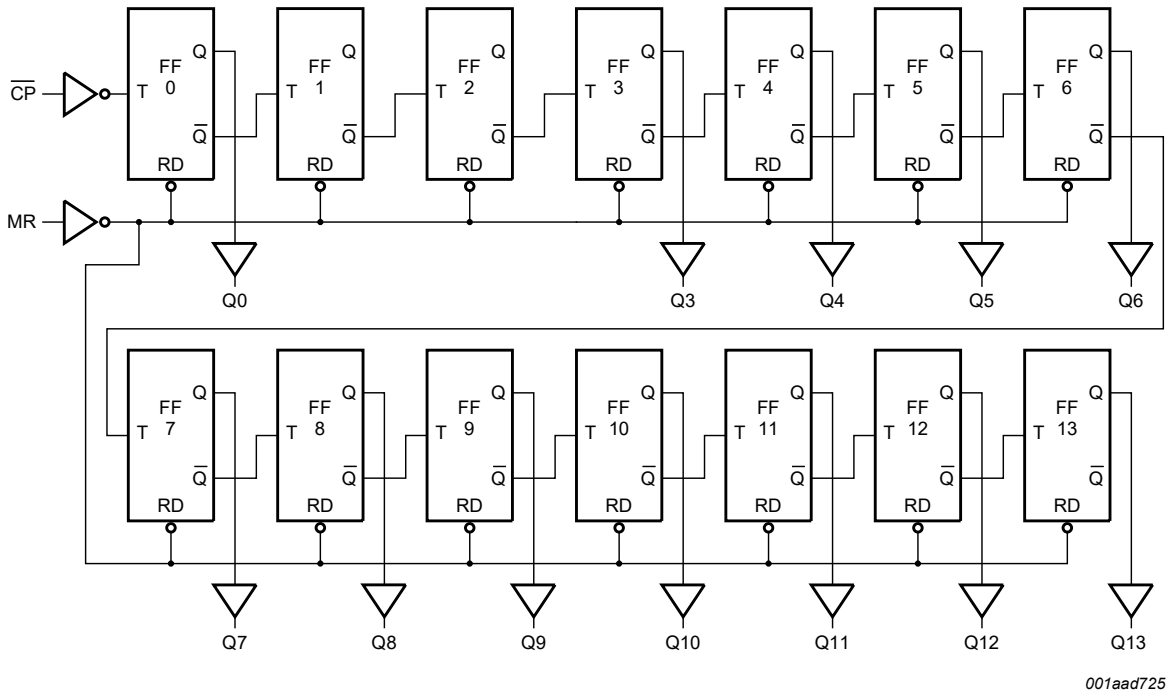
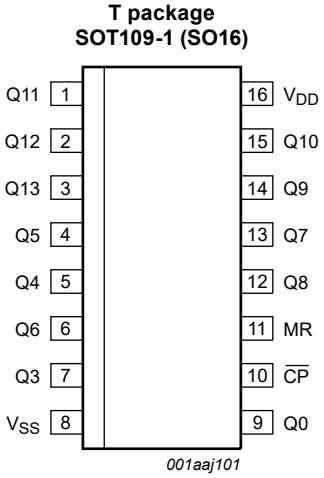


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13	7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	parallel output (Q3 to Q13)
V_{SS}	8	ground supply voltage
Q0	9	parallel output
$\overline{CP}$	10	clock input (HIGH-to-LOW edge triggered)
MR	11	master reset input (active HIGH)
V_{DD}	16	supply voltage

6. Functional description

Table 3. Functional table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

Input		Output
$\overline{CP}$	MR	Q0, Q3 to Q13
↑	L	no change
↓	L	count
X	H	L

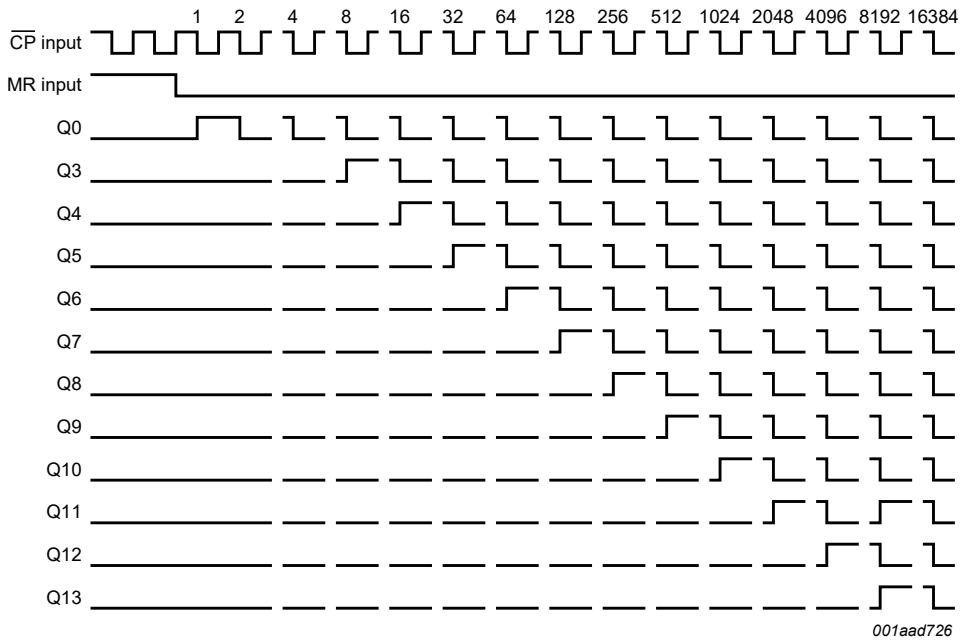


Fig. 5. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	T_{amb} -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	µs/V
		V_{DD} = 10 V	-	-	0.5	µs/V
		V_{DD} = 15 V	-	-	0.08	µs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	$\overline{CP}$ to Q0; see Fig. 6	5 V	78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V	34 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	65	ns
		Qn to Qn + 1	5 V	53 ns + (0.55 ns/pF)C_L	-	80	160	ns
			10 V	19 ns + (0.23 ns/pF)C_L	-	30	60	ns
			15 V	12 ns + (0.16 ns/pF)C_L	-	20	40	ns
		MR to Qn; see Fig. 6	5 V	153 ns + (0.55 ns/pF)C_L	-	180	360	ns
			10 V	79 ns + (0.23 ns/pF)C_L	-	90	180	ns
			15 V	62 ns + (0.16 ns/pF)C_L	-	70	140	ns
t_{PLH}	LOW to HIGH propagation delay	$\overline{CP}$ to Q0; see Fig. 6	5 V	78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V	39 ns + (0.23 ns/pF)C_L	-	50	95	ns
			15 V	27 ns + (0.16 ns/pF)C_L	-	35	70	ns
		Qn to Qn + 1	5 V	43 ns + (0.55 ns/pF)C_L	-	70	140	ns
			10 V	14 ns + (0.23 ns/pF)C_L	-	25	50	ns
			15 V	12 ns + (0.16 ns/pF)C_L	-	20	40	ns
t_t	transition time	see Fig. 6	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_W	pulse width	$\overline{CP}$ = HIGH; minimum width; see Fig. 6	5 V		50	25	-	ns
			10 V		25	15	-	ns
			15 V		20	10	-	ns
		MR = HIGH; minimum width; see Fig. 6	5 V		130	65	-	ns
			10 V		95	50	-	ns
			15 V		90	45	-	ns
t_{rec}	recovery time	MR input; see Fig. 6	5 V		115	60	-	ns
			10 V		65	35	-	ns
			15 V		55	25	-	ns
f_{max}	maximum frequency	see Fig. 6	5 V		5	10	-	MHz
			10 V		13	25	-	MHz
			15 V		18	35	-	MHz

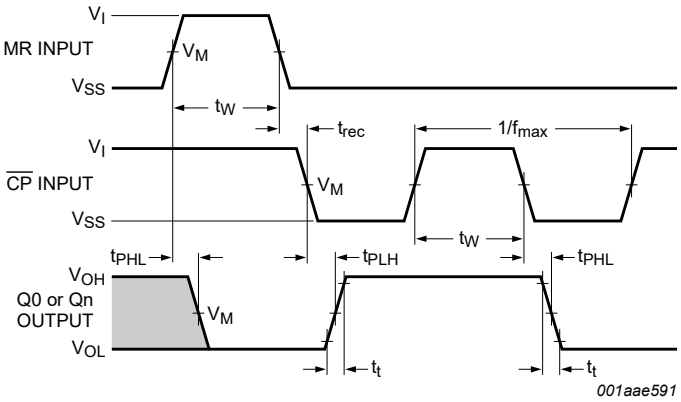
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 600 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz, f_o = output frequency in MHz, C_L = output load capacitance in pF, V_{DD} = supply voltage in V, $\sum(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 2800 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 8200 \times f_i + \sum(f_o \times C_L) \times V_{DD}^2$	

10.1. Waveforms and test circuit

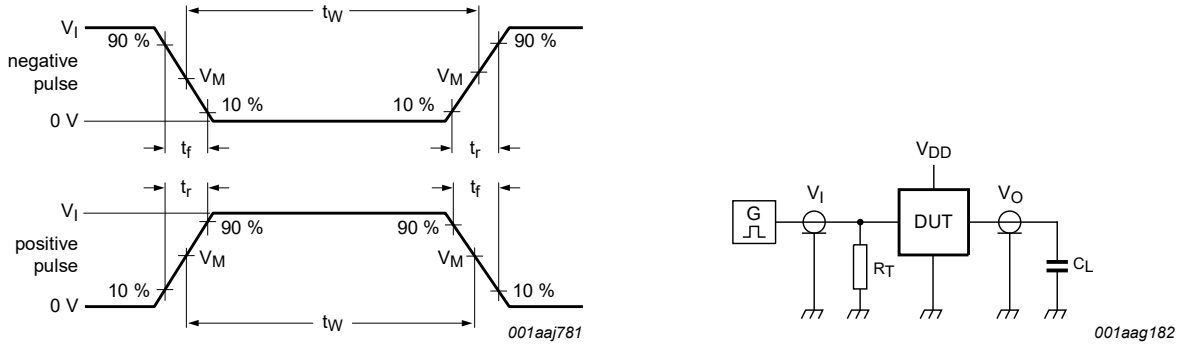


Measurement points are given in Table 9.

Fig. 6. Propagation delays, minimum pulse widths, transition and recovery times and maximum clock frequency

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



a. Input waveforms

b. Test circuit

Test data is given in Table 10.

Definitions test circuit:

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

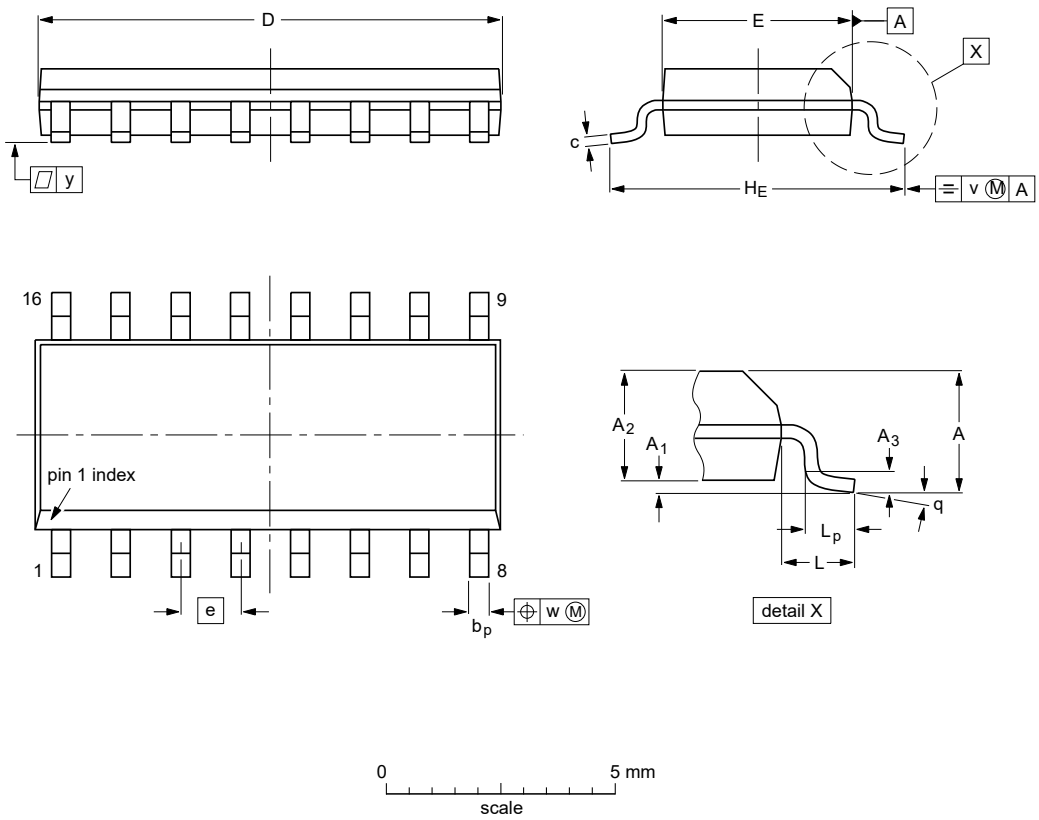
Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 8. Package outline SOT109-1 (SO16)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4020B v.12	20240808	Product data sheet	-	HEF4020B v.11
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 8: Aligned SO package outline drawing to JEDEC MS-012			
HEF4020B v.11	20211207	Product data sheet	-	HEF4020B v.10
Modifications:	• Section 1 and Section 2 updated.			
HEF4020B v.10	20181018	Product data sheet	-	HEF4020B v.9
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
HEF4020B v.9	20160321	Product data sheet	-	HEF4020B v.8
Modifications:	• Type number HEF4020BP (SOT38-4) removed.			
HEF4020B v.8	20111118	Product data sheet	-	HEF4020B v.7
Modifications:	• Legal pages updated. • Changes in "General description" and "Features and benefits". • Section "Applications" removed.			
HEF4020B v.7	20111010	Product data sheet	-	HEF4020B v.6
HEF4020B v.6	20091127	Product data sheet	-	HEF4020B v.5
HEF4020B v.5	20090707	Product data sheet	-	HEF4020B v.4
HEF4020B v.4	20081204	Product data sheet	-	HEF4020B_CNV v.3
HEF4020B_CNV v.3	19950101	Product specification	-	HEF4020B_CNV v.2
HEF4020B_CNV v.2	19950101	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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