HEF40244B

Octal buffers with 3-state outputs

Rev. 6 — 8 August 2024 Product data sheet

1. General description

The HEF40244B is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables (1$\overline{OE}$ and 2$\overline{OE}$), each controlling four of the 3-state outputs. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Complies with JEDEC standard JESD 13-B
- ESD protection
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from −40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF40244BT	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

4. Functional diagram

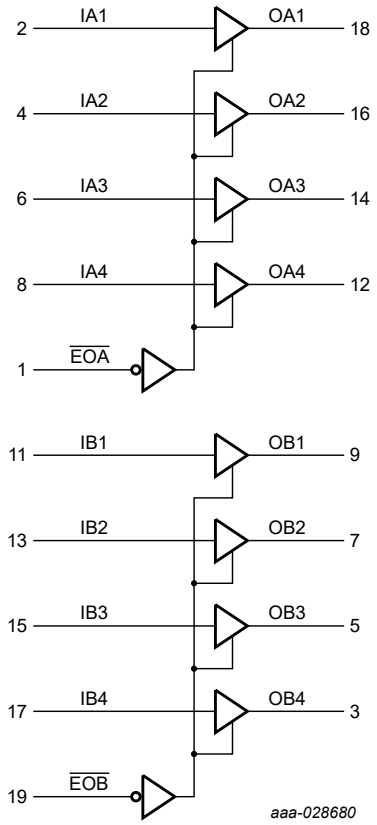


Fig. 1. Logic symbol

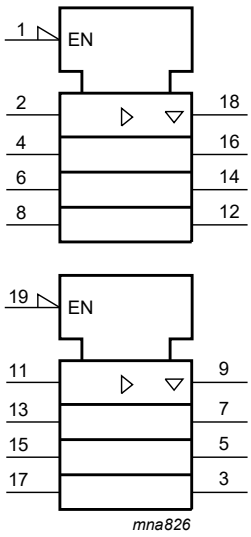


Fig. 2. IEC logic symbol

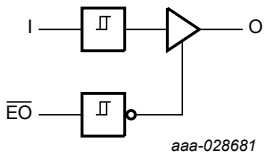
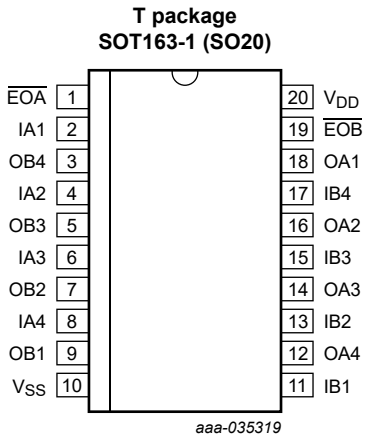


Fig. 3. Logic diagram (one buffer)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{EOA}$, $\overline{EOB}$	1, 19	output enable inputs (active low)
IA1, IA2, IA3, IA4	2, 4, 6, 8	data inputs
OA1, OA2, OA3, OA4	18, 16, 14, 12	data outputs
IB1, IB2, IB3, IB4	11, 13, 15, 17	data inputs
OB1, OB2, OB3, OB4	9, 7, 5, 3	data outputs
V_{SS}	10	ground supply voltage
V_{DD}	20	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
$\overline{EOA}$ or $\overline{EOB}$	**IAn or IBn**	**OAn or OBn**
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+18	V
V_I	input voltage		−0.5	V_{DD} + 0.5	V
I_{DD}	supply current		-	±100	mA
I_{IK}	input clamping current		-	±10	mA
I_{OK}	output clamping current		-	±25	mA
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	referenced to V_{SS} (usually ground)	3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	3.75	µs/V
		V_{DD} = 10 V	-	0.5	µs/V
		V_{DD} = 15 V	-	0.08	µs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions		T_{amb} = -40 °C		T_{amb} = 25 °C			T_{amb} = 85 °C		Unit
			V_{DD}	Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA									
		V_O = 0.5 V or 4.5 V	5 V	3.5	-	3.5	-	-	3.5	-	V
		V_O = 1.0 V or 9.0 V	10 V	7.0	-	7.0	-	-	7.0	-	V
		V_O = 1.5 V or 13.5 V	15 V	11.0	-	11.0	-	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA									
		V_O = 0.5 V or 4.5 V	5 V	-	1.5	-	-	1.5	-	1.5	V
		V_O = 1.0 V or 9.0 V	10 V	-	3.0	-	-	3.0	-	3.0	V
		V_O = 1.5 V or 13.5 V	15 V	-	4.0	-	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V	4.95	-	4.95	-	-	4.95	-	V
			10 V	9.95	-	9.95	-	-	9.95	-	V
			15 V	14.95	-	14.95	-	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V	-	0.05	-	-	0.05	-	0.05	V
			10 V	-	0.05	-	-	0.05	-	0.05	V
			15 V	-	0.05	-	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	see Fig. 4 and Fig. 5									
		V_{OH} = 3.6 V	5 V	−9.3	-	−10	−24	-	−10.7	-	mA
		V_{OH} = 4.6 V	5 V	−0.75	-	−0.6	−1.2	-	−0.45	-	mA
		V_{OH} = 8.4 V	10 V	−14.4	-	−15	−46	-	−15	-	mA
		V_{OH} = 9.5 V	10 V	−1.85	-	−1.5	−3.0	-	−1.1	-	mA
		V_{OH} = 13.2 V	15 V	−19.5	-	−20	−62	-	−19.8	-	mA
		V_{OH} = 13.5 V	15 V	−14.5	-	−15	−50	-	−15.5	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	5 V	2.9	-	2.3	5.4	-	1.75	-	mA
		V_{OL} = 0.5 V	10 V	9.5	-	7.6	17	-	5.5	-	mA
		V_{OL} = 1.5 V	15 V	30.0	-	25	45	-	19.0	-	mA
I_I	input leakage current	[1]	15 V	-	±0.3	-	-	±0.3	-	±1.0	µA
I_{OZ}	OFF-state output current	V_O = V_{DD}	15 V	-	1.6	-	-	1.6	-	12.0	µA
		V_O = V_{SS}	15 V	-	−1.6	-	-	−1.6	-	−12.0	µA

Symbol	Parameter	Conditions		T_{amb} = -40 °C		T_{amb} = 25 °C			T_{amb} = 85 °C		Unit
			V_{DD}	Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	supply current	I_O = 0 A	5 V	-	4.0	-	-	4.0	-	30	µA
			10 V	-	8.0	-	-	8.0	-	60	µA
			15 V	-	16.0	-	-	16.0	-	120	µA
V_H	hysteresis voltage		5 V	-	-	-	220	-	-	-	mV
			10 V	-	-	-	250	-	-	-	mV
			15 V	-	-	-	320	-	-	-	mV
C_I	input capacitance			-	-	-	7.5	-	-	-	pF

[1] Unused inputs must be connected to V_{DD}, V_{SS} or another input.

10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; unless otherwise specified; for waveform and test circuit, see Fig. 9.

Symbol	Parameter	Conditions	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	IAn to OAn; IBn to OBn; see Fig. 6. [1]					
		V_{DD} = 5 V	83 ns + (0.24 ns/pF)C_L	-	95	190	ns
		V_{DD} = 10 V	35 ns + (0.10 ns/pF)C_L	-	40	80	ns
		V_{DD} = 15 V	26 ns + (0.07 ns/pF)C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	IAn to OAn; IBn to OBn; see Fig. 6. [1]					
		V_{DD} = 5 V	82 ns + (0.06 ns/pF)C_L	-	85	170	ns
		V_{DD} = 10 V	38 ns + (0.03 ns/pF)C_L	-	40	80	ns
		V_{DD} = 15 V	29 ns + (0.02 ns/pF)C_L	-	30	60	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{EOA}$ to OAn; $\overline{EOB}$ to OBn; see Fig. 8.					
		V_{DD} = 5 V		-	80	160	ns
		V_{DD} = 10 V		-	35	70	ns
		V_{DD} = 15 V		-	30	60	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{EOA}$ to OAn; $\overline{EOB}$ to OBn; see Fig. 8.					
		V_{DD} = 5 V		-	90	180	ns
		V_{DD} = 10 V		-	40	80	ns
		V_{DD} = 15 V		-	30	60	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$\overline{EOA}$ to OAn; $\overline{EOB}$ to OBn; see Fig. 8.					
		V_{DD} = 5 V		-	70	140	ns
		V_{DD} = 10 V		-	35	70	ns
		V_{DD} = 15 V		-	30	60	ns
t_{PLZ}	LOW to OFF-state propagation delay	$\overline{EOA}$ to OAn; $\overline{EOB}$ to OBn; see Fig. 8.					
		V_{DD} = 5 V		-	75	150	ns
		V_{DD} = 10 V		-	40	80	ns
		V_{DD} = 15 V		-	30	60	ns

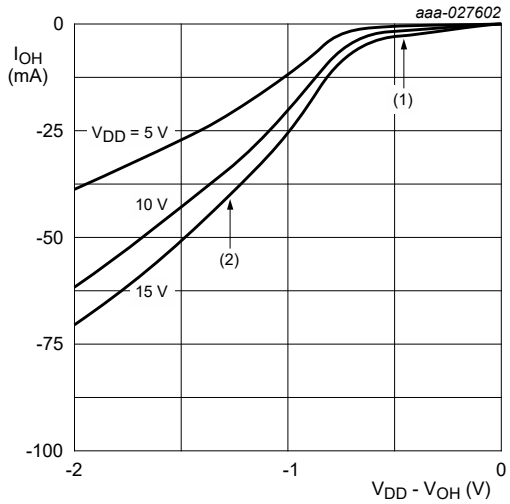
Symbol	Parameter	Conditions	Extrapolation formula	Min	Typ	Max	Unit
t_{THL}	HIGH to LOW output transition time	OAn; OBn; see Fig. 6 and Fig. 7.					
		V_{DD} = 5 V		-	40	80	ns
		V_{DD} = 10 V		-	20	40	ns
		V_{DD} = 15 V		-	15	30	ns
t_{TLH}	LOW to HIGH output transition time	OAn; OBn; see Fig. 6 and Fig. 7.					
		V_{DD} = 5 V		-	30	60	ns
		V_{DD} = 10 V		-	20	40	ns
		V_{DD} = 15 V		-	15	30	ns

[1] The typical values of the propagation delay are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation

Symbol	Parameter	V_{DD}	Typical formula	where:
P_D	dynamic power dissipation	5 V	$P_D = 4250 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; $\Sigma(f_o \times C_L)$ = sum of the outputs; V_{DD} = supply voltage in V.
		10 V	$P_D = 17000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	
		15 V	$P_D = 46000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ (μW)	

10.1. Waveforms and test circuit



(1) P-channel MOS transistor conducting.

(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

Fig. 4. Typical output source current characteristic.

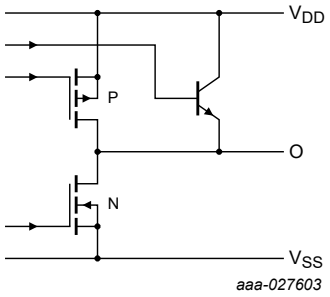
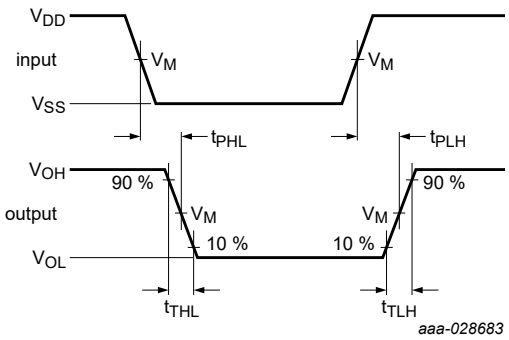


Fig. 5. Schematic diagram of output stage.



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. Input (IAn; IBn) to output (OAn; OBn) propagation delays and output transition time.

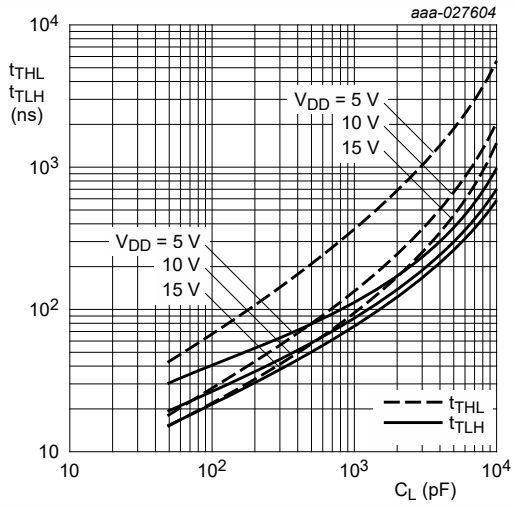
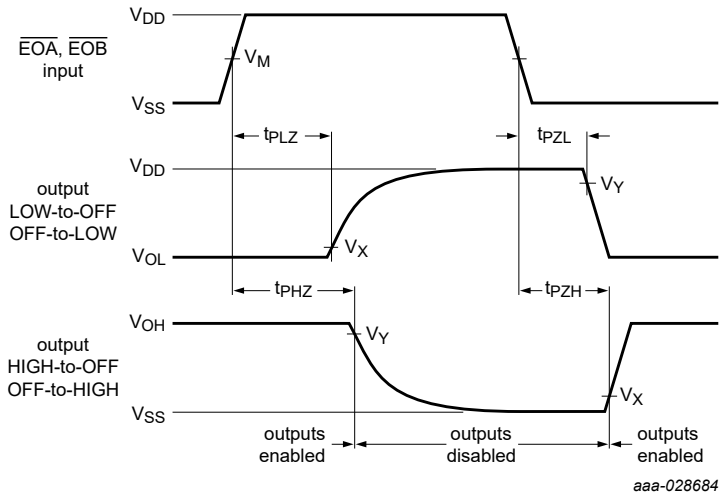


Fig. 7. Output transition times as a function of the load capacitance



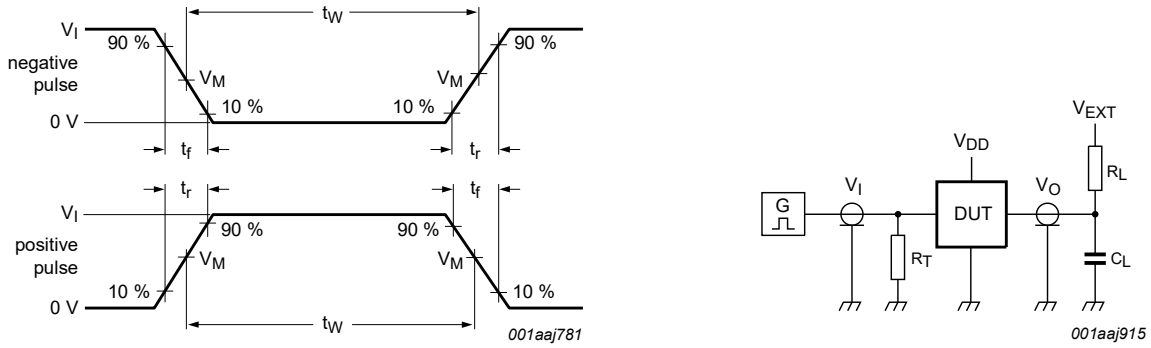
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 8. 3-state enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{DD}	V_M	V_M	V_X	V_Y
5 V to 15 V	0.5 × V_{DD}	0.5 × V_{DD}	0.1 × V_{DD}	0.9 × V_{DD}



a. Input waveform

b. Test circuit

Test and measurement data is given in Table 10.

Definitions test circuit:

R_L = Load resistance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance.

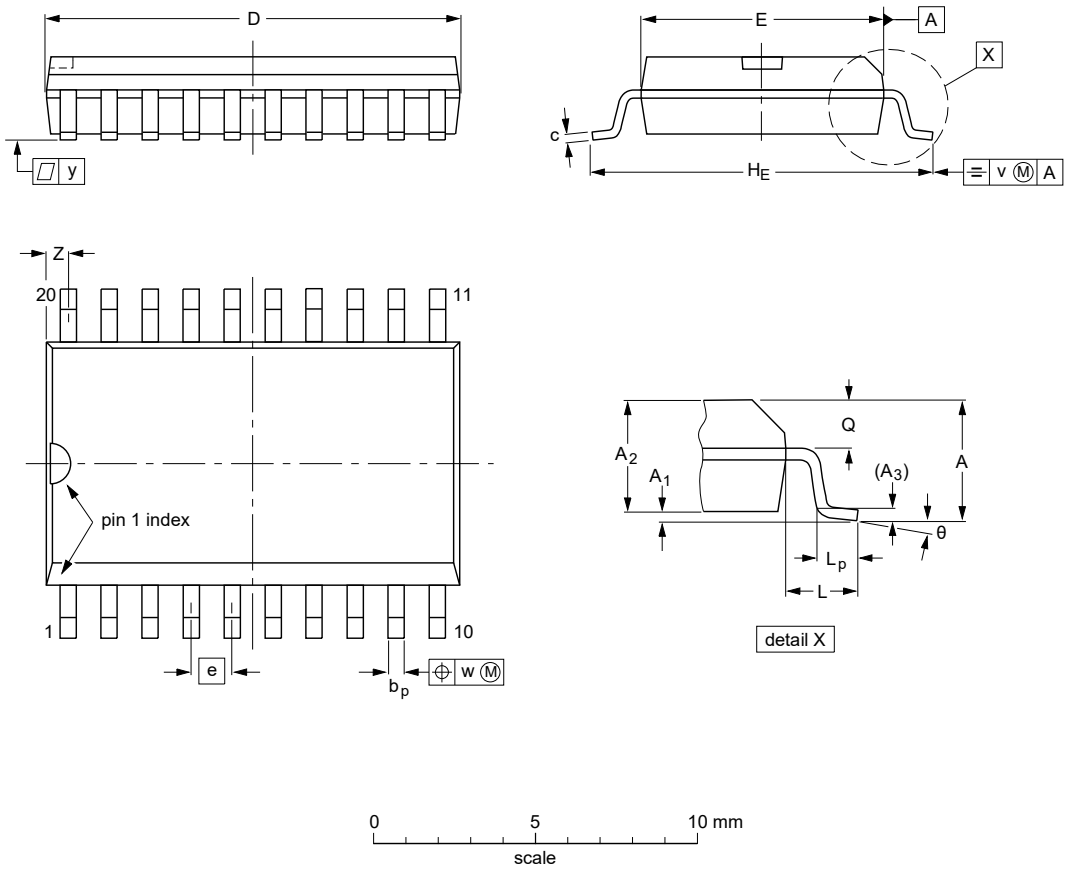
Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{DD}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	1 kΩ	open	V_{SS}	V_{DD}

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT163-1 (SO20)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40244B v.6	20240808	Product data sheet	-	HEF40244B v.5
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
HEF40244B v.5	20231020	Product data sheet	-	HEF40244B v.4
Modifications:	• Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation removed.			
HEF40244B v.4	20180629	Product data sheet	-	HEF40244B v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
HEF40244B v.3	19950101	Product specification	-	HEF40244B v.2
HEF40244B v.2	19950101	Product specification	-	HEF40244B v.1

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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