HEF4027B-Q100

Dual JK flip-flop

Rev. 3 — 8 August 2024 Product data sheet

1. General description

The HEF4027B-Q100 is a dual positive-edge triggered JK flip-flop featuring independent set direct (nSD), clear direct (nCD), clock inputs (nCP) and complementary outputs (nQ and n$\overline{Q}$). Data is accepted when nCP is LOW, and transferred to the output on the positive-going edge of the clock. The asynchronous clear-direct (nCD) and set-direct (nSD) are independent and override the nJ, nK, and nCP inputs. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

- Registers
- Counters
- Control circuits

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4027BT-Q100	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5. Functional diagram

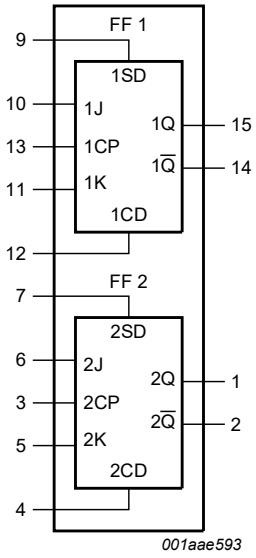


Fig. 1. Functional diagram

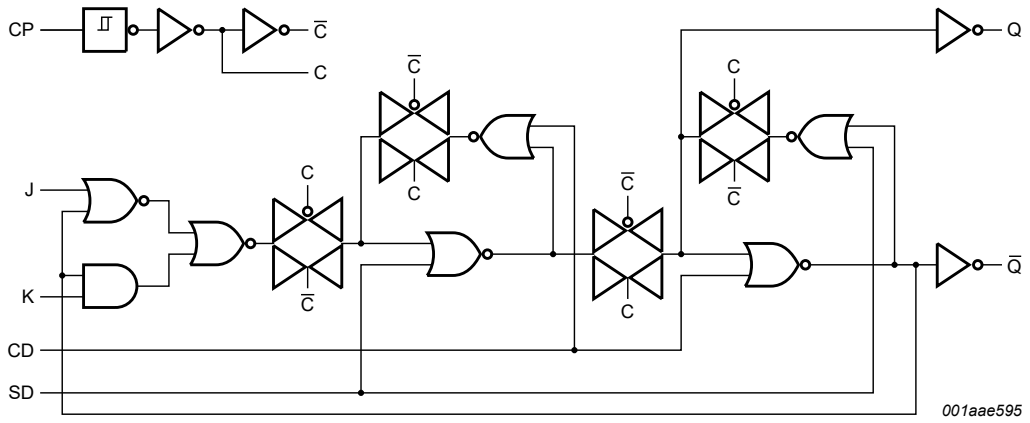
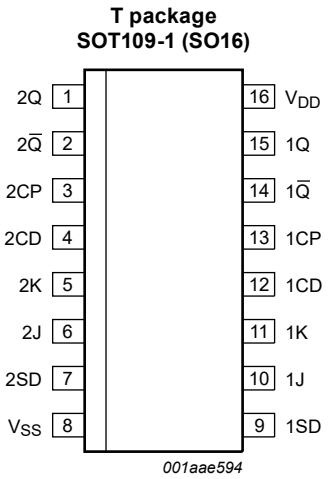


Fig. 2. Logic diagram of one flip-flop

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{SS}	8	ground supply voltage
1SD, 2SD	9, 7	asynchronous set-direct input (active HIGH)
1J, 2J	10, 6	synchronous input
1K, 2K	11, 5	synchronous input
1CD, 2CD	12, 4	asynchronous clear-direct input (active HIGH)
1CP, 2CP	13, 3	clock input (LOW-to-HIGH edge-triggered)
$1\overline{Q}$, $2\overline{Q}$	14, 2	complement output
1Q, 2Q	15, 1	true output
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.; ↑ = positive-going transition.

Inputs					Outputs	
nSD	**nCD**	**nCP**	**nJ**	**nK**	**nQ**	**n$\overline{Q}$**
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H
L	L	↑	L	L	no change	no change
L	L	↑	H	L	H	L
L	L	↑	L	H	L	H
L	L	↑	H	H	n$\overline{Q}$	nQ

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature	in free air	-40	+85	°C
P_{tot}	total power dissipation	T_{amb} -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		3	15	V
V_I	input voltage		0	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	3.75	µs/V
		V_{DD} = 10 V	-	0.5	µs/V
		V_{DD} = 15 V	-	0.08	µs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	I_O = 0 A	5 V	-	4.0	-	4.0	-	30	µA
			10 V	-	8.0	-	8.0	-	60	µA
			15 V	-	16.0	-	16.0	-	120	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP → Q, $\overline{Q}$; see Fig. 3	5 V	78 ns + (0.55 ns/pF)C_L	-	105	210	ns
			10 V	29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
		CD → Q; see Fig. 3	5 V	93 ns + (0.55 ns/pF)C_L	-	120	240	ns
			10 V	33 ns + (0.23 ns/pF)C_L	-	45	90	ns
			15 V	27 ns + (0.16 ns/pF)C_L	-	35	70	ns
		SD → $\overline{Q}$; see Fig. 3	5 V	113 ns + (0.55 ns/pF)C_L	-	140	280	ns
			10 V	44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C_L	-	40	80	ns

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula [1]	Min	Typ	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	CP → Q, $\overline{Q}$; see Fig. 3	5 V	58 ns + (0.55 ns/pF)C_L	-	85	170	ns
			10 V	27 ns + (0.23 ns/pF)C_L	-	35	70	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
		CD → $\overline{Q}$; see Fig. 3	5 V	48 ns + (0.55 ns/pF)C_L	-	75	150	ns
			10 V	24 ns + (0.23 ns/pF)C_L	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF)C_L	-	25	50	ns
		SD → Q; see Fig. 3	5 V	43 ns + (0.55 ns/pF)C_L	-	70	140	ns
			10 V	19 ns + (0.23 ns/pF)C_L	-	30	60	ns
			15 V	17 ns + (0.16 ns/pF)C_L	-	25	50	ns
t_t	transition time	see Fig. 3	5 V [2]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{su}	set-up time	J, K → CP; see Fig. 4	5 V		50	25	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns
t_h	hold time	J, K → CP; see Fig. 4	5 V		25	0	-	ns
			10 V		20	0	-	ns
			15 V		15	5	-	ns
t_W	pulse width	CP LOW; minimum width; see Fig. 4	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
		SD, CD HIGH; minimum width; see Fig. 5	5 V		90	45	-	ns
			10 V		40	20	-	ns
			15 V		30	15	-	ns
t_{rec}	recovery time	SD, CD inputs; see Fig. 5	5 V		+20	-15	-	ns
			10 V		+15	-10	-	ns
			15 V		+10	-5	-	ns
f_{max}	maximum frequency	CP input; J = K = HIGH; see Fig. 4	5 V		4	8	-	MHz
			10 V		12	25	-	MHz
			15 V		15	30	-	MHz

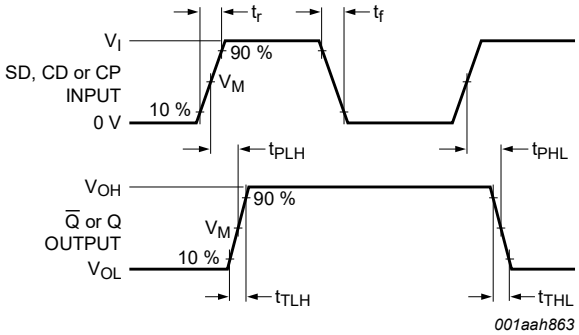
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).
[2] t_t is the same as t_{TLH} and t_{THL}.

Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

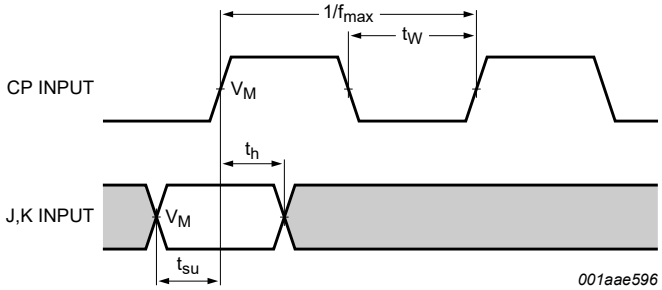
Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	Where:
P_D	dynamic power dissipation	5 V	$P_D = 900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz f_o = output frequency in MHz C_L = output load capacitance in pF V_{DD} = supply voltage in V $\Sigma(f_o \times C_L)$ = sum of the outputs
		10 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 13200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.1. Waveforms and test circuit



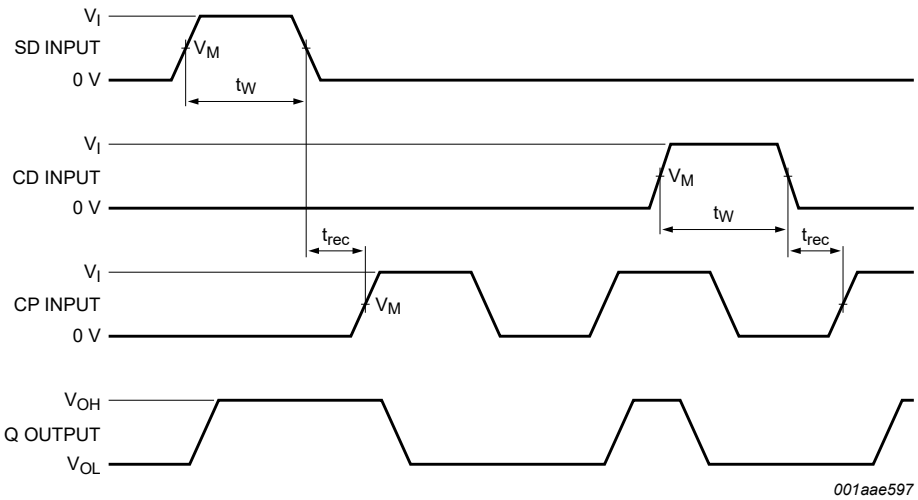
V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.
Measurement points are given in Table 9.

Fig. 3. Waveforms showing rise, fall, and transition times, and propagation delays



Measurement points are given in Table 9.

Fig. 4. Waveforms showing set-up times, hold times, and minimum clock pulse width

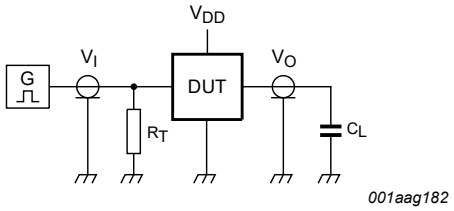


V_{OH} and V_{OL} are typical output voltages levels that occur with the output load.
Measurement points are given in Table 9.

Fig. 5. Waveforms showing pulse widths and recovery times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in Table 10.

Definitions test circuit:

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

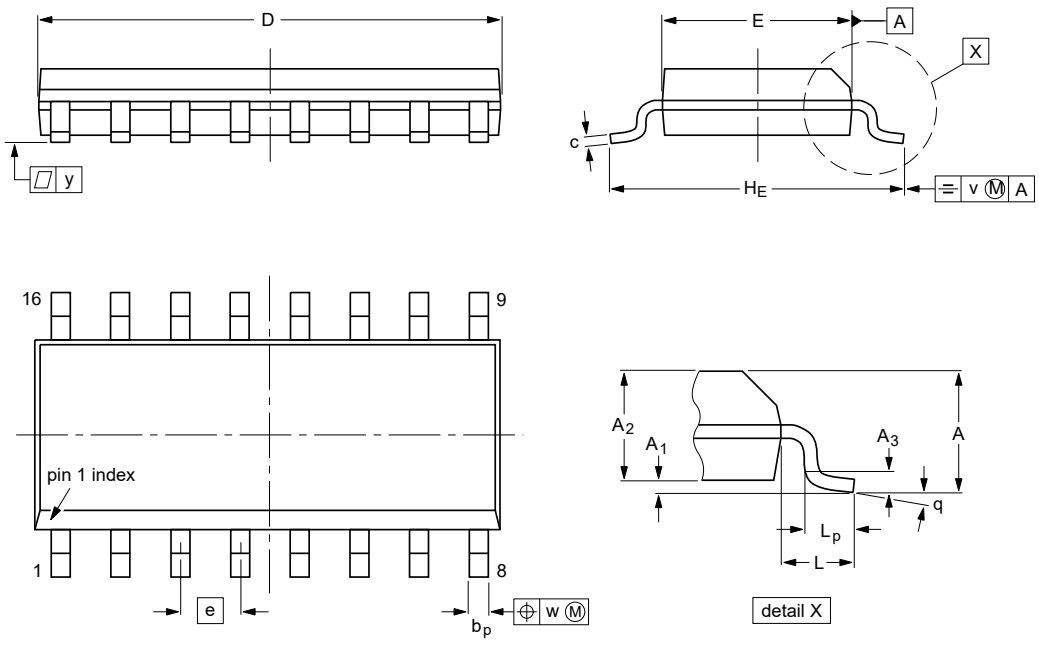
Fig. 6. Test circuit

Table 10. Test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4027B_Q100 v.3	20240808	Product data sheet	-	HEF4027B_Q100 v.2
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 7: Aligned SO package outline drawing to JEDEC MS-012			
HEF4027B_Q100 v.2	20211207	Product data sheet	-	HEF4027B_Q100 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated.			
HEF4027B_Q100 v.1	20130626	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 8 August 2024