

# HEF4066B-Q100

## Quad single-pole single-throw analog switch

Rev. 5 — 25 July 2024

Product data sheet

### 1. General description

The HEF4066B-Q100 is a quad single pole, single throw analog switch. Each switch features two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

### 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

### 3. Applications

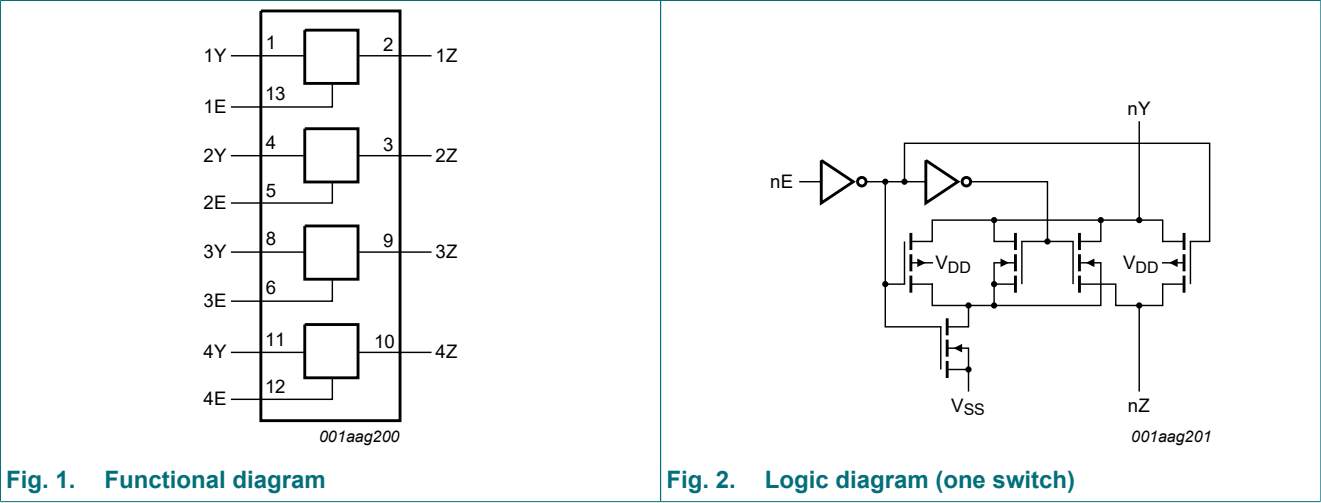
- Industrial and automotive
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

### 4. Ordering information

Table 1. Ordering information

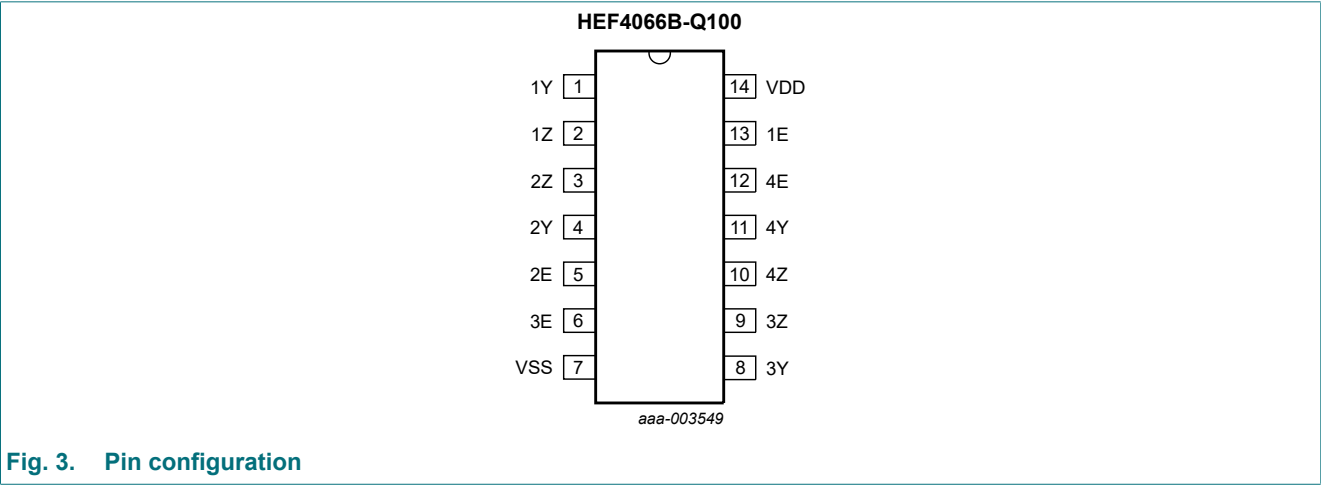
Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">HEF4066BT-Q100</a>	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 8, 11	independent input or output
1Z, 2Z, 3Z, 4Z	2, 3, 9, 10	independent input or output
1E, 2E, 3E, 4E	13, 5, 6, 12	enable input (active HIGH)
V <sub>SS</sub>	7	ground (0 V)
V <sub>DD</sub>	14	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nE	Switch
H	ON
L	OFF

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0\text{ V}$  (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V
$I_{I/O}$	input/output current	[1]	-	$\pm 10$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+125	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW
P	power dissipation	per switch	-	100	mW

- [1] To avoid drawing  $V_{DD}$  current out of terminal nZ, when switch current flows into terminals nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no  $V_{DD}$  current will flow out of terminals nY, in this case there is no limit for the voltage drop across the switch, but the voltages at nY and nZ may not exceed  $V_{DD}$  or  $V_{SS}$ .
- [2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		T <sub>amb</sub> = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	I <sub>O</sub>   < 1 µA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V <sub>IL</sub>	LOW-level input voltage	I <sub>O</sub>   < 1 µA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
I <sub>I</sub>	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	µA
I <sub>S(OFF)</sub>	OFF-state leakage current	per channel; see Fig. 4	15 V	-	-	-	200	-	-	-	-	nA
I <sub>DD</sub>	supply current	all valid input combinations	5 V	-	1.0	-	1.0	-	7.5	-	7.5	µA
			10 V	-	2.0	-	2.0	-	15.0	-	15.0	µA
			15 V	-	4.0	-	4.0	-	30.0	-	30.0	µA
C <sub>I</sub>	input capacitance	nE input	-	-	-	-	7.5	-	-	-	-	pF

10.1. Test circuit

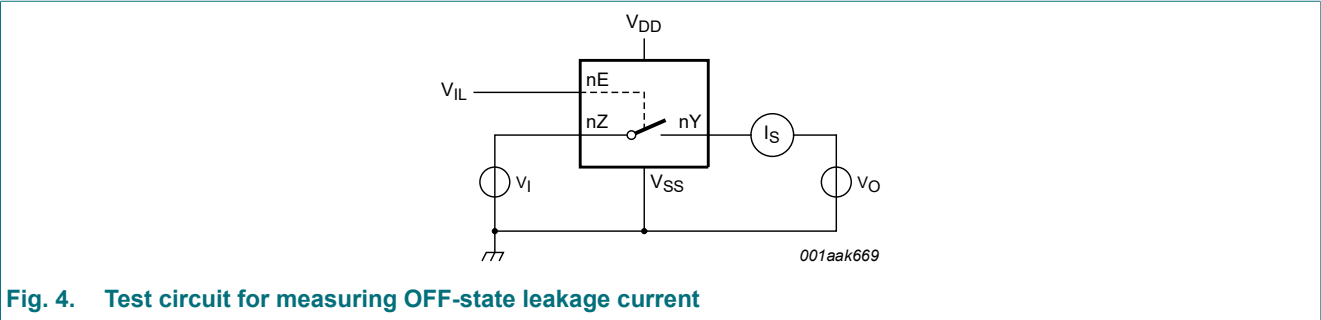


Fig. 4. Test circuit for measuring OFF-state leakage current

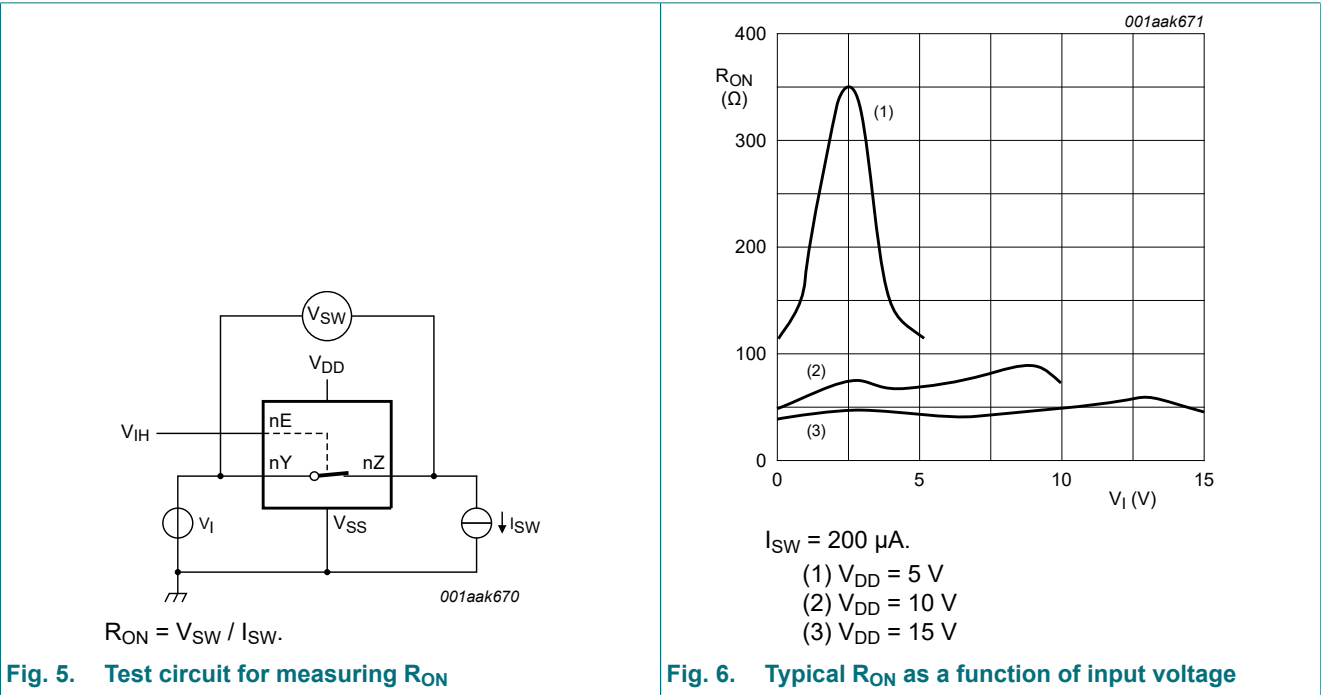
10.2. ON resistance

Table 7. ON resistance

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $I_{SW} = 200\text{ }\mu\text{A}$ ;  $V_{SS} = 0\text{ V}$ .

Symbol	Parameter	Conditions	$V_{DD}$	Typ	Max	Unit
$R_{ON(peak)}$	ON resistance (peak)	$V_I = 0\text{ V to }V_{DD}$ ; see Fig. 5 and Fig. 6.	5 V	350	2500	$\Omega$
			10 V	80	245	$\Omega$
			15 V	60	175	$\Omega$
$R_{ON(rail)}$	ON resistance (rail)	$V_I = 0\text{ V}$ ; see Fig. 5 and Fig. 6.	5 V	115	340	$\Omega$
			10 V	50	160	$\Omega$
			15 V	40	115	$\Omega$
		$V_I = V_{DD}$ ; see Fig. 5 and Fig. 6.	5 V	120	365	$\Omega$
			10 V	65	200	$\Omega$
			15 V	50	155	$\Omega$
$\Delta R_{ON}$	ON resistance mismatch between channels	$V_I = 0\text{ V to }V_{DD}$ ; see Fig. 5	5 V	25	-	$\Omega$
			10 V	10	-	$\Omega$
			15 V	5	-	$\Omega$

10.2.1. ON resistance waveform and test circuit



11. Dynamic characteristics

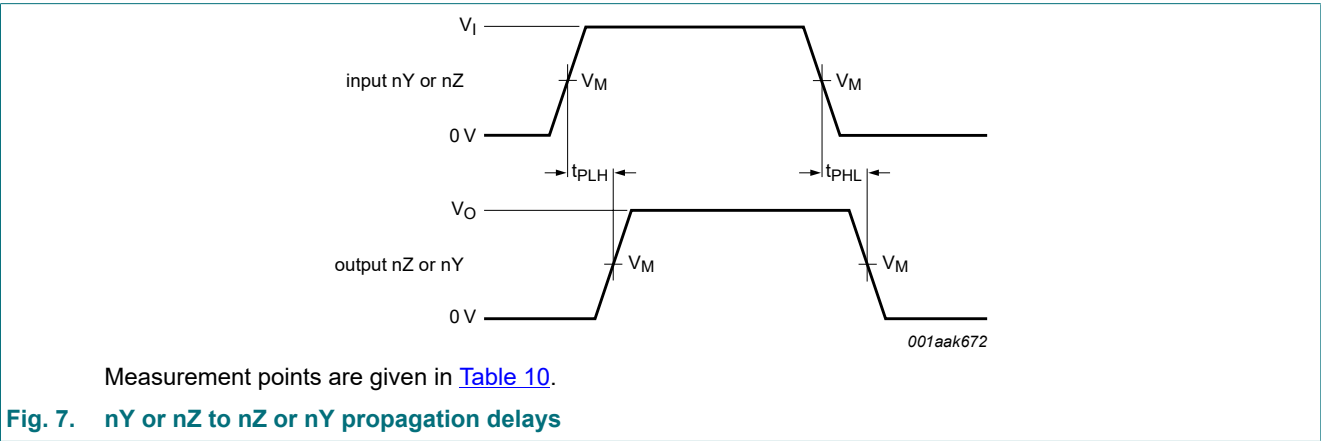
Table 8. Dynamic characteristics  
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{SS} = 0\text{ V}$ ; for test circuit see Fig. 9.

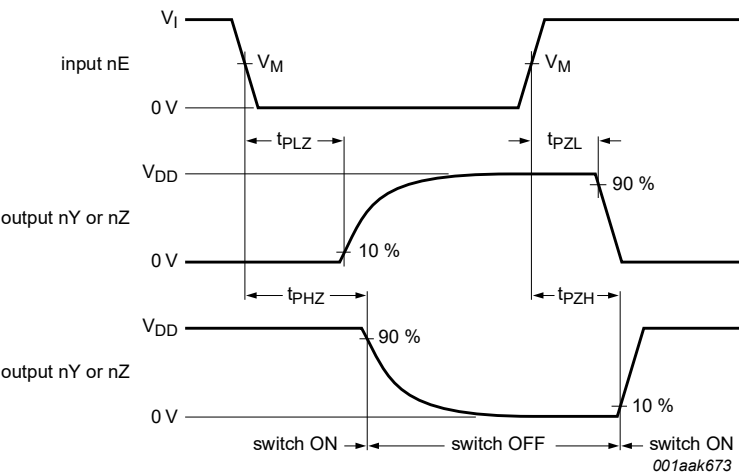
Symbol	Parameter	Conditions	V <sub>DD</sub>	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	nY, nZ to nZ, nY; see Fig. 7	5 V	10	20	ns
			10 V	5	10	ns
			15 V	5	10	ns
		nY, nZ to nZ, nY; see Fig. 7	5 V	10	20	ns
			10 V	5	10	ns
			15 V	5	10	ns
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	nE to nY, nZ; see Fig. 8	5 V	80	160	ns
			10 V	65	130	ns
			15 V	60	120	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	nE to nY, nZ; see Fig. 8	5 V	40	80	ns
			10 V	20	40	ns
			15 V	15	30	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	nE to nY, nZ; see Fig. 8	5 V	80	160	ns
			10 V	70	140	ns
			15 V	70	140	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	nE to nY, nZ; see Fig. 8	5 V	45	90	ns
			10 V	20	40	ns
			15 V	15	30	ns

Table 9. Dynamic power dissipation  
 $P_D$  can be calculated from the formulas shown;  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	V <sub>DD</sub>	Typical formula for P <sub>D</sub> (μW)	where:
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 2500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(C_L \times f_o)$ = sum of the outputs.
		10 V	$P_D = 11500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 29000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.1. Waveforms and test circuit



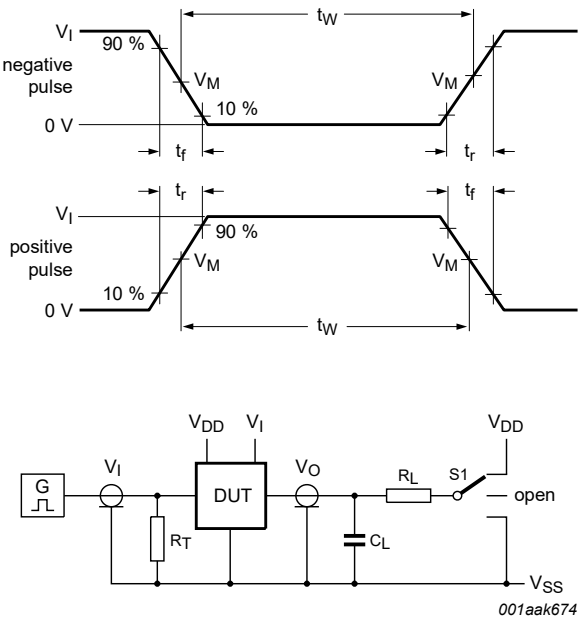


Measurement points are given in [Table 10](#).

Fig. 8. Enable and disable times

Table 10. Measurement points

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 11](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$C_L$  = Load capacitance including test jig and probe;

$R_L$  = Load resistance.

Fig. 9. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		S1 position		
V <sub>DD</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
5 V to 15 V	0 V or V <sub>DD</sub>	≤ 20 ns	50 pF	10 kΩ	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>

11.2. Additional dynamic parameters

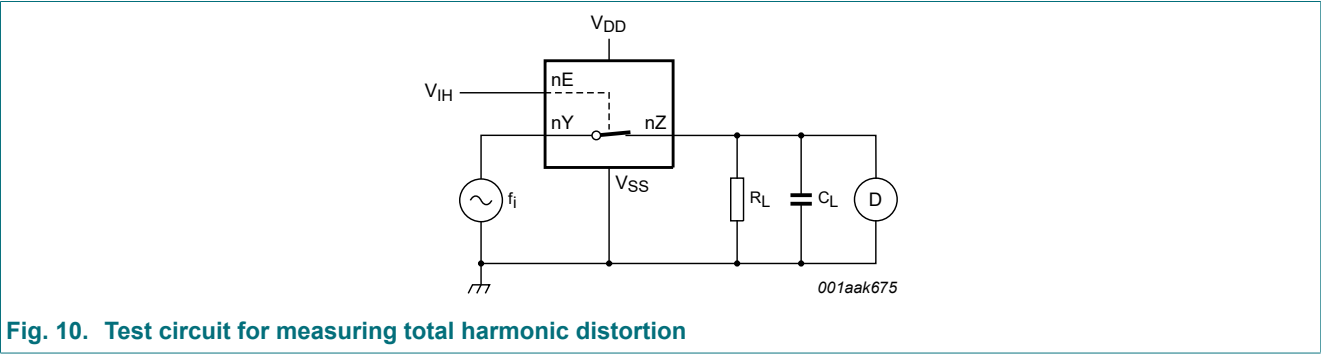
Table 12. Additional dynamic characteristics

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

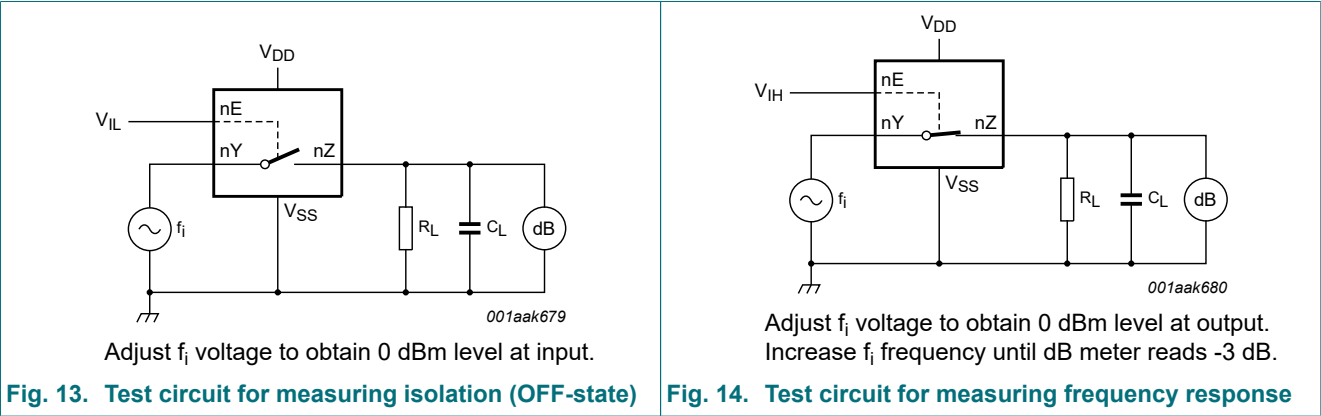
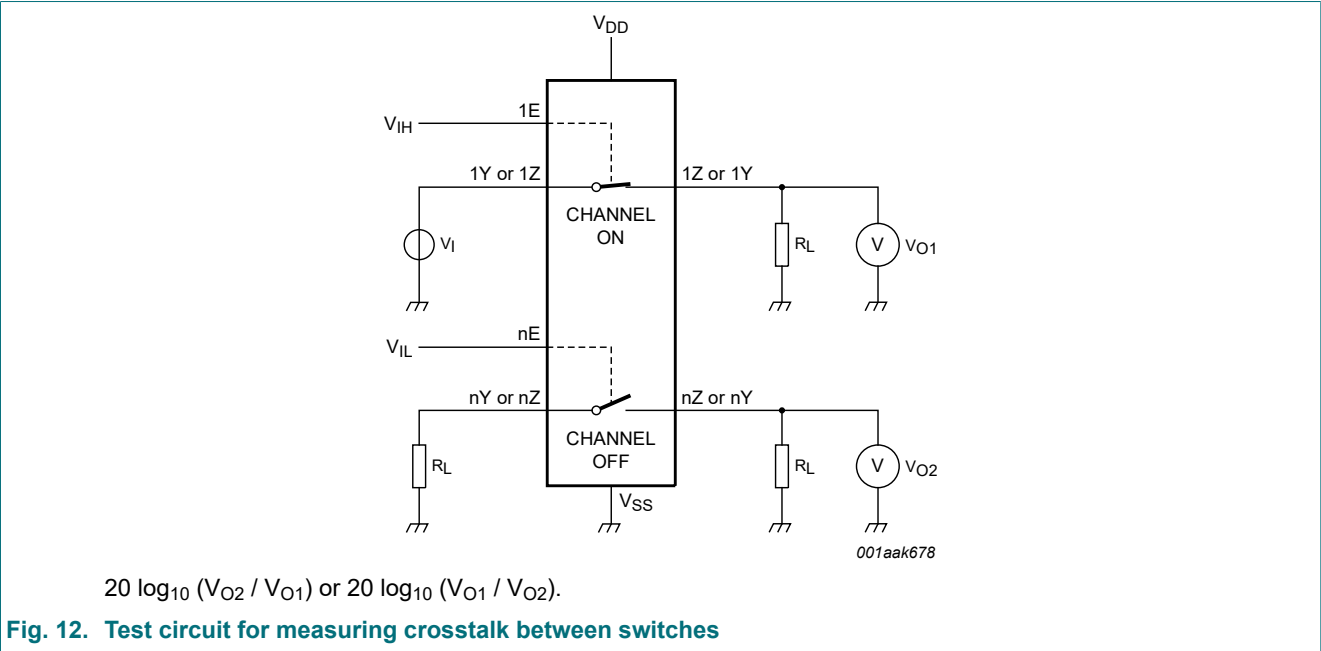
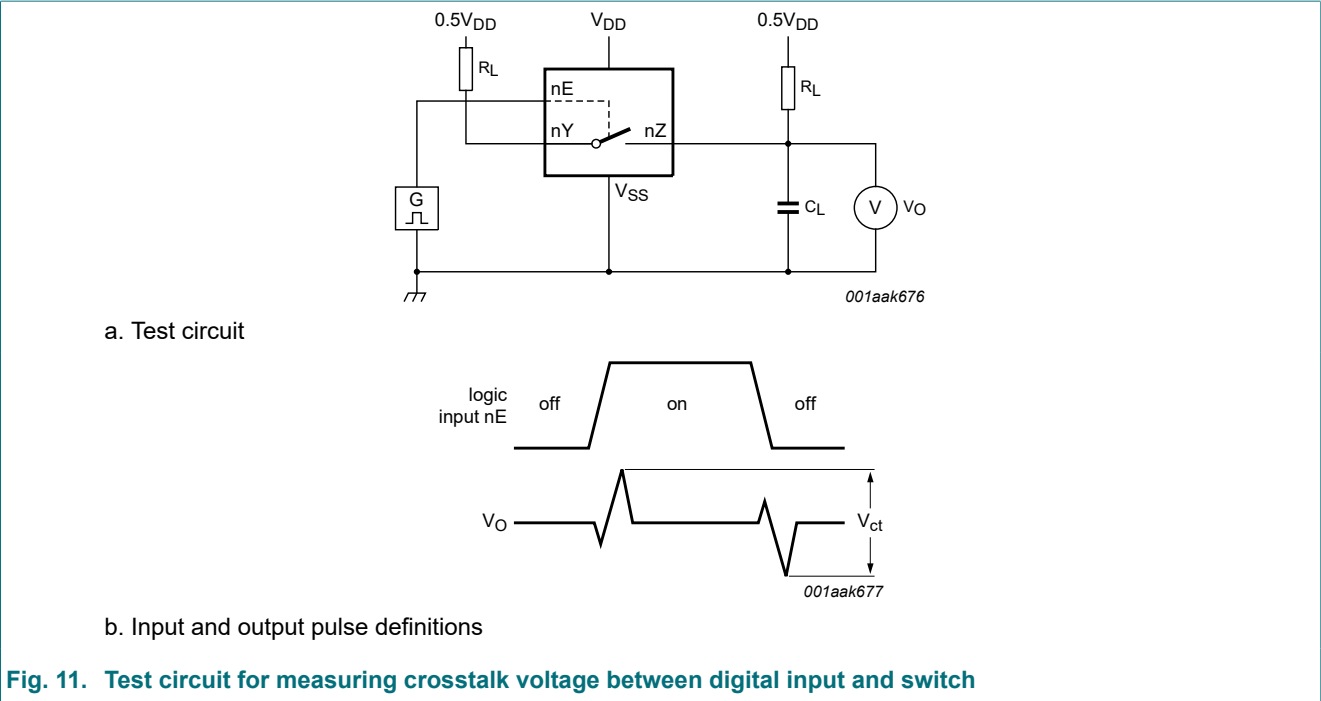
Symbol	Parameter	Conditions	$V_{DD}$	Typ	Max	Unit
THD	total harmonic distortion	see Fig. 10; $R_L = 10\text{ k}\Omega$ ; $C_L = 15\text{ pF}$ ; channel ON; $V_I = 0.5V_{DD}$ (p-p); $f_i = 1\text{ kHz}$	[1] 5 V	0.25	-	%
			10 V	0.04	-	%
			15 V	0.04	-	%
$V_{ct}$	crosstalk voltage	nE input to switch; see Fig. 11; $R_L = 10\text{ k}\Omega$ ; $C_L = 15\text{ pF}$ ; nE = $V_{DD}$ (square-wave)	10 V	50	-	mV
Xtalk	crosstalk	between switches; see Fig. 12; $f_i = 1\text{ MHz}$ ; $R_L = 1\text{ k}\Omega$ ; $V_I = 0.5V_{DD}$ (p-p)	[1] 10 V	-50	-	dB
$\alpha_{iso}$	isolation (OFF-state)	see Fig. 13; $f_i = 1\text{ MHz}$ ; $R_L = 1\text{ k}\Omega$ ; $C_L = 5\text{ pF}$ ; $V_I = 0.5V_{DD}$ (p-p)	[1] 10 V	-50	-	dB
$f_{(-3dB)}$	-3 dB frequency response	see Fig. 14; $R_L = 1\text{ k}\Omega$ ; $C_L = 5\text{ pF}$ ; $V_I = 0.5V_{DD}$ (p-p)	[1] 10 V	90	-	MHz

[1]  $f_i$  is biased at  $0.5V_{DD}$ .

11.2.1. Test circuits







12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

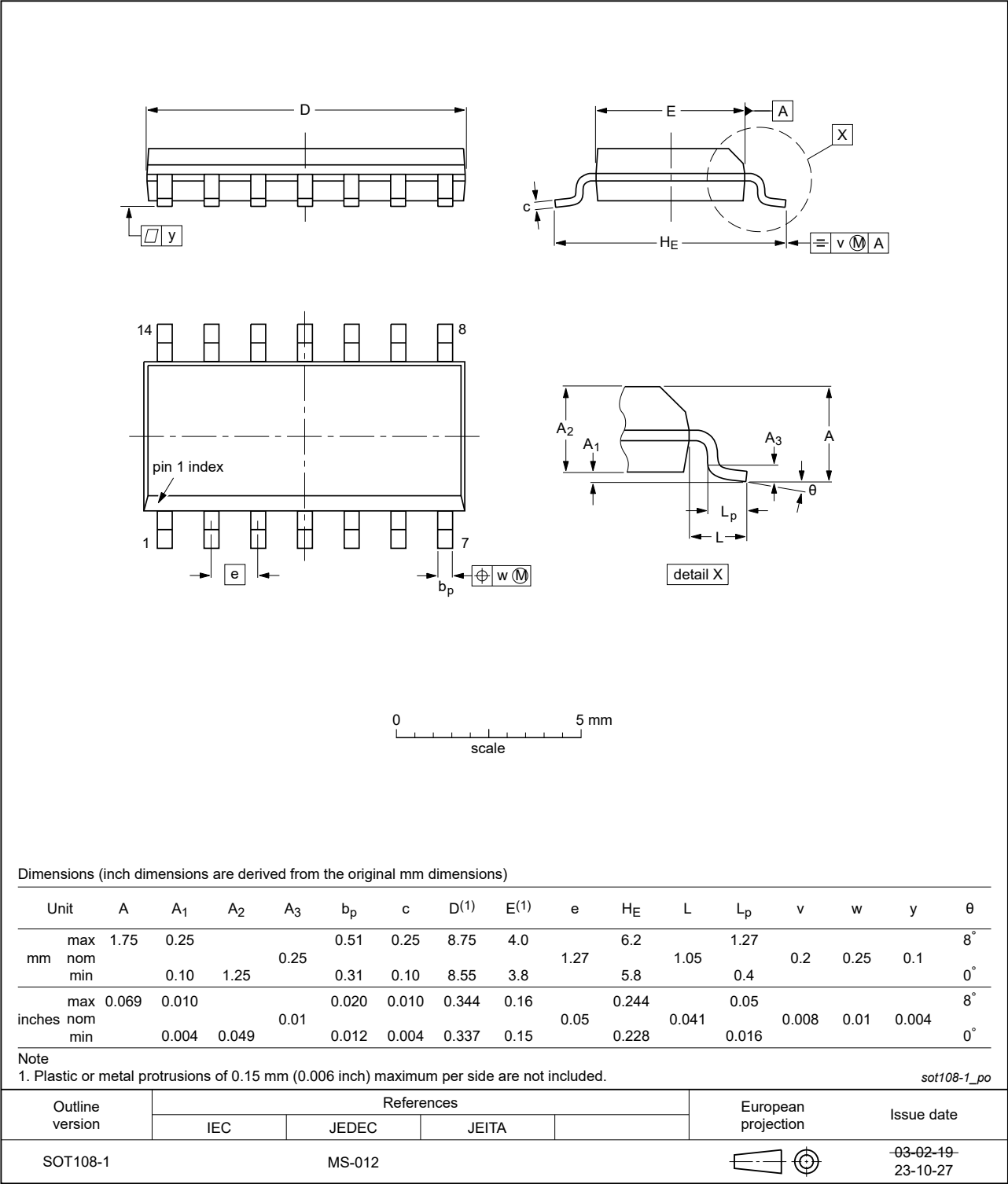


Fig. 15. Package outline SOT108-1 (SO14)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4066B_Q100 v.5	20240725	Product data sheet	-	HEF4066B_Q100 v.4
Modifications:	<ul style="list-style-type: none"><li>Section 2: ESD specification updated according to the latest JEDEC standard.</li><li>Fig. 15: Aligned SO package outline drawing to JEDEC MS-012</li></ul>			
HEF4066B_Q100 v.4	20211221	Product data sheet	-	HEF4066B_Q100 v.3
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Section 1 and Section 2 updated.</li><li>Table 4: Derating values for P<sub>tot</sub> total power dissipation updated.</li></ul>			
HEF4066B_Q100 v.3	20160419	Product data sheet	-	HEF4066B_Q100 v.2
Modifications:	<ul style="list-style-type: none"><li>Table 4: Condition for total power dissipation changed (errata).</li><li>Table 4: Maximum ambient temperature changed (errata).</li></ul>			
HEF4066B_Q100 v.2	20140911	Product data sheet	-	HEF4066B_Q100 v.1
Modifications:	<ul style="list-style-type: none"><li>Fig. 11: Test circuit modified.</li></ul>			
HEF4066B_Q100 v.1	20120807	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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