HEF4518B

Dual BCD counter

Rev. 10 — 5 September 2024 Product data sheet

1. General description

The HEF4518B is a dual 4-bit internally synchronous BCD counter. The counter has two clock inputs (CP0 and $\overline{CP}1$), buffered outputs from all four bit positions (O0 to O3) and an asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP0 input if $\overline{CP}1$ is HIGH or the HIGH to LOW transition of the $\overline{CP}1$ input if CP0 is LOW. Either CP0 or $\overline{CP}1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O0 to O3 = LOW) independent of CP0 and $\overline{CP}1$. Schmitt-trigger action in the clock inputs makes the circuit highly tolerant to slower clock rise and fall times. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Applications

- Multistage synchronous counting
- Multistage asynchronous counting
- Frequency dividers

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4518BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

nexperia

5. Functional diagram

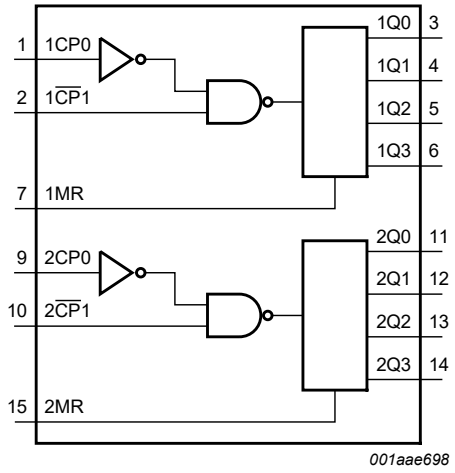


Fig. 1. Functional diagram

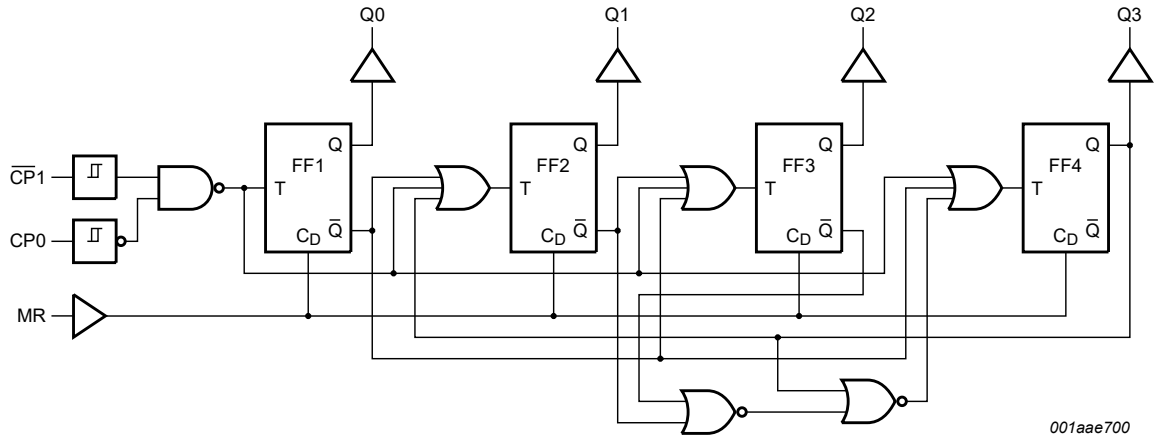


Fig. 2. Logic diagram for one counter

6. Pinning information

6.1. Pinning

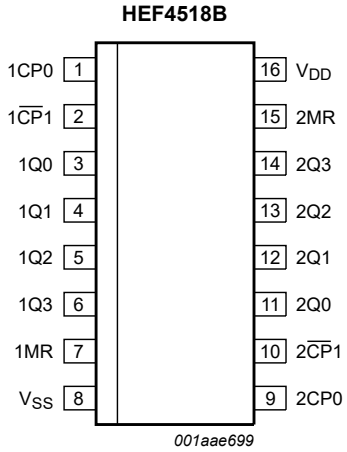


Fig. 3. Pin configuration for SOT109-1 (SO16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP0, 2CP0	1, 9	clock input (LOW-to-HIGH triggered)
$1\overline{CP}1$, $2\overline{CP}1$	2, 10	clock input (HIGH-to-LOW triggered)
1Q0, 2Q0	3, 11	output
1Q1, 2Q1	4, 12	output
1Q2, 2Q2	5, 13	output
1Q3, 2Q3	6, 14	output
1MR, 2MR	7, 15	master reset input
V_{DD}	16	supply voltage
V_{SS}	8	ground supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

nCP0	n$\overline{CP}$1	nMR	Mode
↑	H	L	counter advances
L	↓	L	counter advances
↓	X	L	no change
X	↑	L	no change
↑	L	L	no change
H	↓	L	no change
X	X	H	nQ0, nQ1, nQ2, nQ3 = LOW

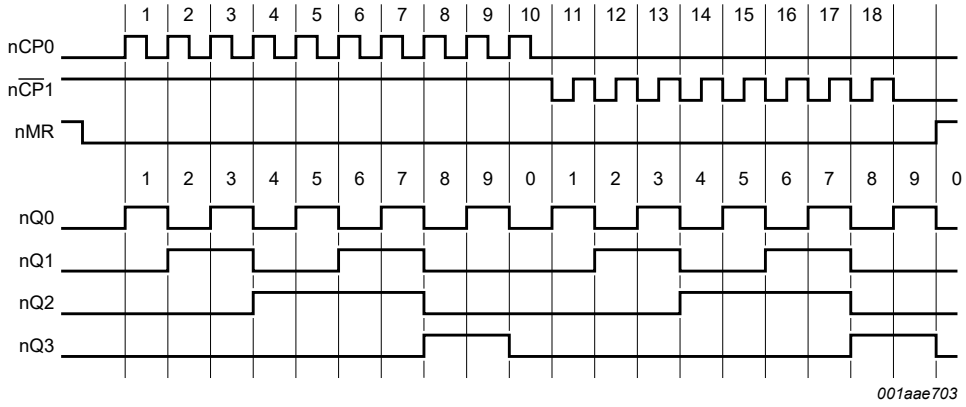


Fig. 4. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
P_{tot}	total power dissipation	T_{amb} -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	µs/V
		V_{DD} = 10 V	-	-	0.5	µs/V
		V_{DD} = 15 V	-	-	0.08	µs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.5	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current	V_{DD} = 15 V	15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	nCP0, n$\overline{CP}$1 to nQn; see Fig. 5	5 V	93 ns + (0.55 ns/pF)C_L	-	120	240	ns
			10 V	44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C_L	-	40	80	ns
		nMR to nQn; see Fig. 5	5 V	48 ns + (0.55 ns/pF)C_L	-	75	150	ns
			10 V	24 ns + (0.23 ns/pF)C_L	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF)C_L	-	25	50	ns
t_{PLH}	LOW to HIGH propagation delay	nCP0, n$\overline{CP}$1 to nQn; see Fig. 5	5 V	93 ns + (0.55 ns/pF)C_L	-	120	240	ns
			10 V	44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C_L	-	40	80	ns
t_t	transition time	nQn; see Fig. 5	5 V	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_W	pulse width	nCP0 input LOW; minimum width; see Fig. 5	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		n$\overline{CP}$1 input HIGH; minimum width see Fig. 5	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nMR input HIGH; minimum width; see Fig. 5	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns
t_{rec}	recovery time	nMR input; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t_{su}	set-up time	nCP0 to n$\overline{CP}$1; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		n$\overline{CP}$1 to nCP0; see Fig. 5	5 V		50	25	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
f_{max}	maximum frequency	nCP0, n$\overline{CP}$1; see Fig. 5	5 V		8	16	-	MHz
			10 V		15	30	-	MHz
			15 V		20	40	-	MHz

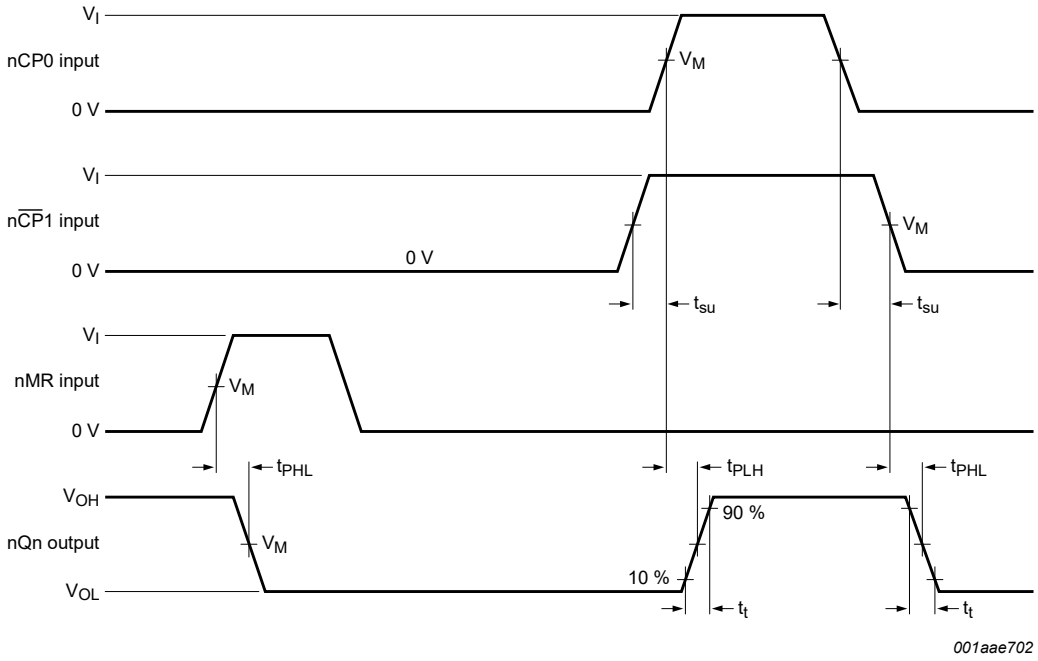
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

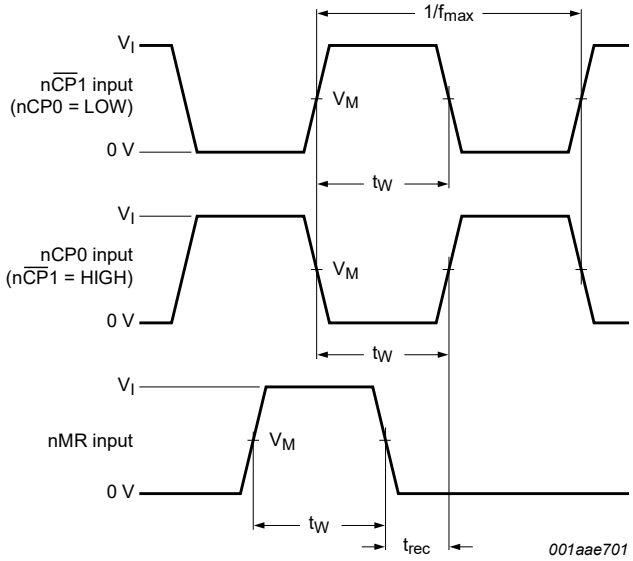
P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	Where:
P_D	dynamic power dissipation	5 V	$P_D = 750 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 3300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 8000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.1. Waveforms and test circuit



a. nCP0 and nCP1 set-up times, propagation delays, and output transition times



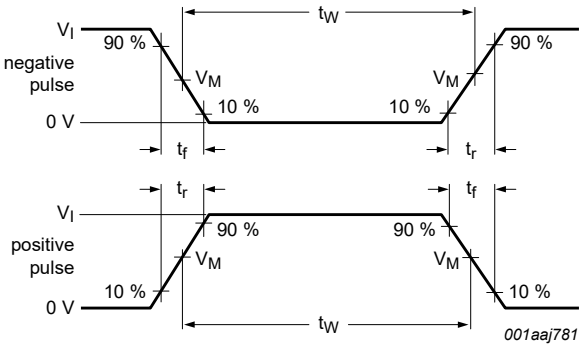
b. nMR recovery time, minimum nCP0, nCP1, and nMR pulse widths, and maximum frequency

Measurement points are given in table Table 9.
The logic levels V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.

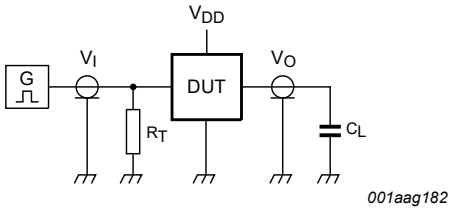
Fig. 5. Waveforms showing measurements for switching times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$



a. Input waveforms



b. Test circuit

Test data is given in Table 10.

Definitions test circuit:

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

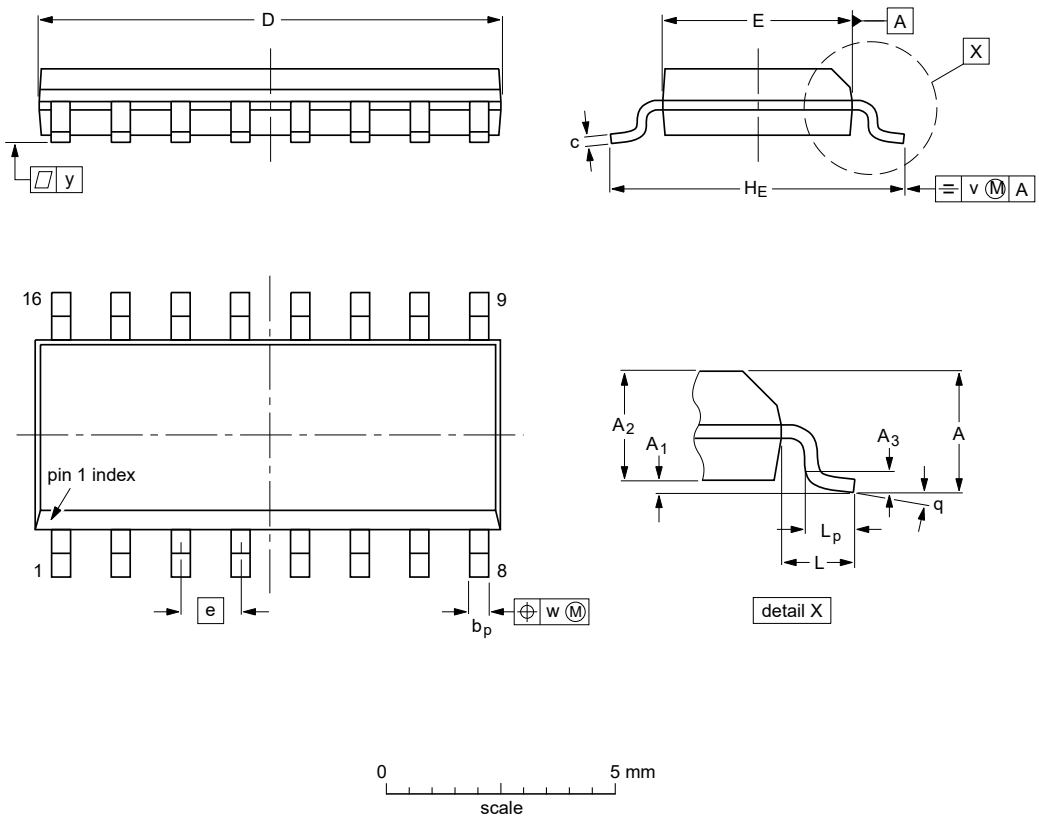
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4518B v.10	20240905	Product data sheet	-	HEF4518B v.9
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 7: Aligned SO package outline drawing to JEDEC MS-012			
HEF4518B v.9	20211203	Product data sheet	-	HEF4518B v.8
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 13 added.			
HEF4518B v.8	20160419	Product data sheet	-	HEF4518B v.7
Modifications:	• Type number HEF4518BP (SOT38-4) removed.			
HEF4518B v.7	20111121	Product data sheet	-	HEF4518B v.6
Modifications:	• Table 6: I_{OH} minimum values changed to maximum • Fig. 6: added "DUT = Device Under Test"			
HEF4518B v.6	20091210	Product data sheet	-	HEF4518B v.5
HEF4518B v.5	20090727	Product data sheet	-	HEF4518B v.4
HEF4518B v.4	20090703	Product data sheet	-	HEF4518B_CNV v.3
HEF4518B_CNV v.3	19950101	Product specification	-	HEF4518B_CNV v.2
HEF4518B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 5 September 2024