LIN Bus Transceiver with Integrated LDO

General Description

The IS32IO1028 is a LIN transceiver designed according to the LIN specification 2.0, 2.1, 2.2, 2.2A and SAEJ2602-2, with a built-in low-drop voltage regulator (3.3V or 5V up to 100mA supply). The combination of voltage regulator and bus transceiver makes it possible to develop simple slave nodes in LIN bus systems. The IS32IO1028 is designed to handle the low-speed data communication in vehicles (for example, in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20kBaud. The bus output is designed to withstand high voltage. Sleep mode (voltage regulator switched off) and standby mode (communication off but VCC LDO on) ensure minimum current consumption.

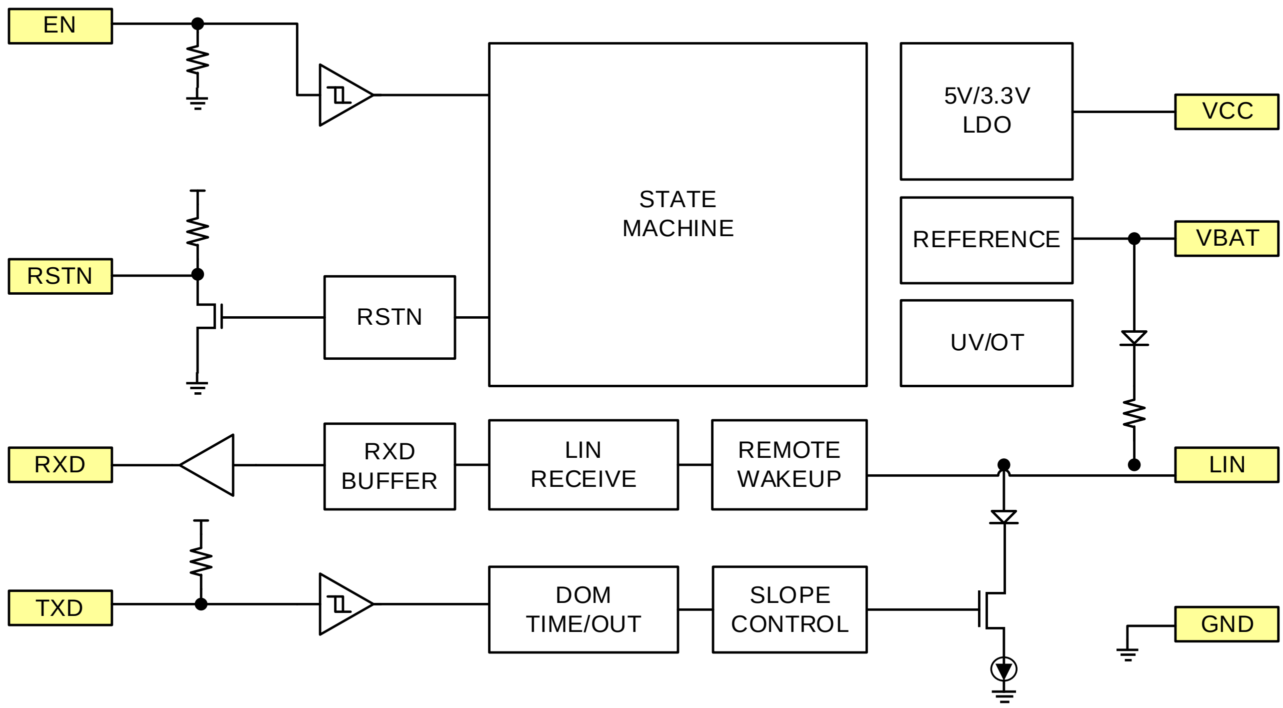
Applications

- Automotive networking
- Industrial networking

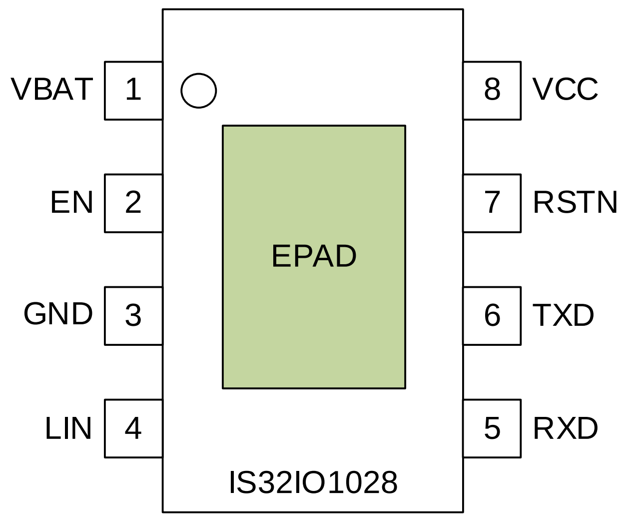
Features

- LIN 2.X/SAE J2602 compliant
- Operating Voltage VBAT = 6V to 30V
  - Undervoltage protection on VBAT
- Support up to 20kBaud
  - Slew rate control
  - Withstand +40V/-27V on Pin LIN
- Build-in LDO output on VCC pin for supplying external components
  - 3.3V/5.0V options
  - +/- 5% accuracy
  - Up to 100mA load
  - Undervoltage protection on V_{CC}
  - Short circuit protection with current limiting
  - Generates reset conditions for RSTN output
- Sleep mode and Wakeup
  - Low current consumption in sleep mode
  - LIN bus wakeup function and Local wakeup from EN pin
- TXD dominant time out function
- Over temperature shut-down
- SOP-8 with exposed pad (eSOP-8), and wettable flank DFN-8 (WDFN-8) packages
  - RoHS and Halogen-Free compliant
- AEC-Q100 qualification
- IS32IO1028A VCC=5V
- IS32IO1028B VCC=3.3V
- TSCA compliance

Block Diagram



Pin Connection



EPAD is GND

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1. Pin Description

PIN #	NAME	I/O	DESCRIPTION
1	VBAT	P	Battery Supply Voltage
2	EN	I	Enable Input with internal pull-down resistor.
3	GND	G	Negative supply ground
4	LIN	I/O	LIN bus pin
5	RXD	O	LIN receive data output
6	TXD	I	LIN transmit data input with internal pull-up resistor. TXD=0 for bus dominant; TXD=1 for bus recessive.
7	RSTN	I/O	Active low reset open-drain output with internal pull-up resistor.
8	VCC	O	LDO regulator output. Output decoupling capacitor of 10uF is necessary.

2. Functional Descriptions

Since the LIN physical layer is independent from higher LIN layers (e.g., LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes, which are according to older versions (i.e., LIN1.0, LIN 1.1, LIN 1.2, LIN 1.3) without any restrictions.

2.1 Supply Pin (VBAT)

LIN operating voltage is VBAT = 6V to 30V. The IS32IO1028 can handle voltages up to 40 V (max). An undervoltage detection is implemented to disable transmission if VBAT falls below V_{BATOFF} in order to avoid false bus messages. After switching on VBAT, the IS32IO1028 starts with the fail-safe mode and the voltage regulator is switched on. The supply current is typically 22µA in sleep mode and 70µA in standby mode.

2.2 Ground Pin (GND)

The IC does not affect the LIN Bus in the event of GND disconnection. It is able to handle a loss of ground under VBAT =18V and VLIN=0V conditions.

2.3 LDO Output (VCC)

The internal 5V/3.3V voltage regulator is capable of driving loads up to 100mA which can supply the microcontroller and other ICs on the PCB and is protected against overload by means of current limitation and over-temperature protection. Furthermore, the output voltage is monitored and will cause a reset condition if it drops below a defined threshold V_{UVD}.

2.4 Reset Output (RSTN)

RSTN is an I/O pin with open-drain output and is pulled low under reset conditions. When RSTN is pulled low by IO1028, it is extended with minimum RSTN low duration of T_{RST}. RSTN as input is used and monitored as a state transition input. RSTN has an internal pull-up 6K Ohm resistor to V_{CC}.

2.5 LIN Bus (LIN)

A low-side driver with internal current limitation and thermal shutdown as well as an internal pull-up resistor according to LIN specification 2.x is implemented. The voltage range is from –27V to +40V. This pin exhibits minimum reverse current from the LIN bus to VBAT, even in the event of a GND shift or VBAT disconnection. The LIN receiver thresholds are compatible with the LIN protocol specification. The fall time (from recessive to dominant) and the rise time (from dominant to recessive) are slope controlled.

2.6 Transmit Data (TXD)

In normal mode, the TXD pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in the recessive state.

The TXD input has an internal pull-up resistor to VCC. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD=0 lasts longer than $T_{DOM,\ TO}$, the dominant output is disabled. The disabled state is released by TXD=1.

2.7 Receive Data (RXD)

In normal mode, this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD and LIN low (dominant state) is indicated by a low level at RXD.

The output is a push-pull stage switching between VCC and GND.

In STB mode, the RXD output indicates if a remote wakeup event has occurred or not. RXD=0 indicates the remote wakeup event has occurred.

2.8 Enable Input (EN)

The Enable Input pin controls the operation mode of the device. If EN is high, the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active. The VCC voltage regulator operates with 3.3V & 5V/100mA output capability. If EN is switched to low while TXD is still high, the device is forced to standby mode. No data transmission is then possible, and the current consumption is reduced to I_{BAT} with a typical 75µA. The VCC regulator has its full functionality. If EN is switched to low while TXD is low, the device is forced to sleep mode. No data transmission is possible, and the voltage regulator is switched off.

EN should not have a duration of less than 100usec to prevent any misinterpretation of state transition.

3. Modes of Operation

There are four states of operations, Off (OFF), Standby (STB), Normal (NRM), and Sleep (SLP) modes. The state transition is illustrated in the following state diagram. The state operation is clocked by a 50KHz clock, and thus the transition of the states may take up to 20usec when conditions of transitions are met.

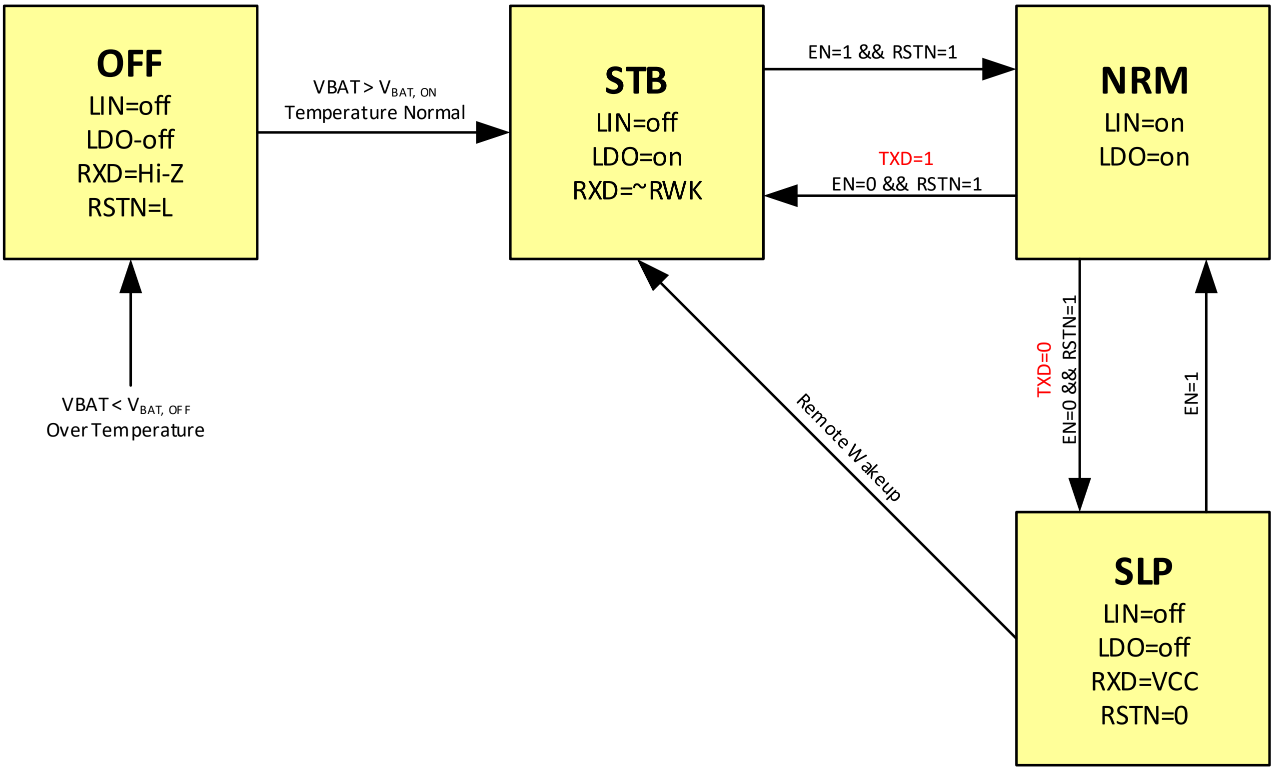


Figure 3-1 State Operation Diagram

3.1 OFF Mode

OFF mode is the initial mode after power-on. It is also the mode entered when VBAT is undervoltage or over-temperature condition occurs. In this mode, LIN function is disabled, and LDO is turned off.

3.2 STB Mode

When VBAT meets minimum operation voltage and temperature is normal, OFF mode transits to STB mode. In STB mode, LIN function is still off but LIN remote wakeup detection is turned on. LDO is also turned on to supply external MCU or local circuits. RXD output reflects the status of remote wakeup detection. If remote wakeup (either from SLP mode transition or in STB mode) was detected, RXD is 0, otherwise RXD is 1. External MCU can use RXD as input for wakeup preparation and set EN=1 which allows STB to NRM transition.

Since LDO is on in STB mode, RSTN reflects the power good condition of V_{CC} supply. RSTN is released until V_{CC} reaches above undervoltage recovery threshold. And RSTN is typically used to reset the external MCU, and RSTN must be de-asserted to allow the transition to NRM mode to ensure the external MCU is fully functional.

Typical current consumption in STB mode is around 70uA.

3.3 NRM Mode

This is the normal transmitting and receiving mode of the LIN physical layer in accordance. The LDO is also on to provide supply voltage for external circuit. If V_{CC} undervoltage is detected, then RSTN is pulled low.

Although LIN physical layer is enabled in NRM mode, to prevent glitches on the LIN bus and to start LIN transmission, TXD=1 must be detected first to enable following transmission onto LIN bus. Another glitch prevention measure is when RSTN=0 or EN=0, the transmission is turned off immediately.

The exit of NRM mode is by setting EN=0. When EN=0 is detected, TXD is also detected to determine the destination state either STB or SLP modes. TXD is sampled after 10usec to 20usec after EN changes from 1 to 0. If sampled TXD is 1, then STB mode is entered, if sampled TXD is 0, then SLP is entered. In addition, RSTN must be high for any transition to be valid.

To ensure correct transition and avoid any glitches erroneously transmitted onto LIN bus, the external MCU should set TXD to 1 first, then set EN to 0. Then after 1usec or longer but less than 8usec, set TXD to 0 or 1, and maintain TXD level for at least 40usec.

3.4 SLP Mode

As described in NRM mode, SLP mode is entered from NRM mode if EN=0 and TXD=0. In SLP mode, only wakeup detection circuit is still active and LIN transceiver as well as LDO is turned off to minimize current consumption. The typical current in SLP mode is around 22uA.

In SLP mode, RXD is pulled up to VCC (as LDO is disabled, VCC will drop to GND gradually), and RSTN is pulled low.

If EN=1 in SLP mode, it will transit back to NRM mode. And in SLP mode, if a remote wakeup condition is detected then it will transit to STB mode. Remote wakeup is a condition the LIN bus is pulled low longer than TWAKEUP (30usec – 150usec) and followed by a LIN bus recessive state.

4. Fail-safe Features

During a short circuit at LIN to VBAT, the current in the transmitter output stage is limited to I_{BUS_LIM}.

The reverse current is very low at pin LIN during the loss of VBAT. This is optimal behavior for bus systems where some slave nodes are supplied from battery.

During a short circuit at VCC, the output limits the output current to I_{VCCLIM}. Because of undervoltage detection, RSTN switches to low and sends a reset to the microcontroller.

Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.

Pin TXD provides a pull-up resistor to force the transceiver into recessive bus level if TXD is disconnected by a bad solder joint or floating microcontroller port pin.

If the TXD pin stays at GND level by application failures, the timer is triggered by a negative edge on the TXD pin. If the pin remains LOW for longer than the TXD dominant time-out time (T_{TXDTO}), the transmitter is disabled forcing the bus line to a recessive state. The timer is reset by a positive edge on TXD. This feature prevents the bus line from being accidentally driven to dominant state after normal mode has been activated (e.g., in the case of a short circuit at TXD to GND) and also prevents a rogue slave node from continuing to overpower the bus line.

The temperature of the IC is monitored in Normal, Standby, and Off modes. If the temperature is too high ($T_J > T_{JOTS}$), the IS32IO1028 will switch to Off mode. The voltage regulator and the LIN transmitter will be switched off and the RSTN pin driven LOW. When the temperature falls below the over-temperature protection release threshold ($T_J < T_{JOTR}$), the IS32IO1028 switches to Standby mode.

5. Electrical Specifications

5.1 Maximum Limit

Parameter	Conditions	MIN	MAX	Unit
Voltage on Pin	Pin VBAT	-0.3	40	V
	Pin TXD, RXD, RSTN and EN	-0.3	VCC + 0.3	V
	Pin LIN with respect to GND	-27	40	V
ESD Rating	HBM			
	Pin LIN and VBAT (Note 1)	-8	+8	kV
	at any other pin	-2	+2	kV
	IEC 61000-4-2			
	Pin LIN and VBAT	-8	+8	kV
	MM			
	Any Pin	-250	+250	V
	CDM			
	Corner Pins	-750	+750	V
	Any Pin	-500	+500	V
Junction Temperature		-40	+125	°C
Storage Temperature		-55	+150	°C

Note 1: VCC and VBAT connected to GND, emulating application circuit.

5.2 Thermal Characteristics

Symbol	Parameter	Conditions	TYP	Unit
Rth(j-a)	thermal resistance from junction to ambient	eSO8 package free air	60	°K/W
		eDFN8 package free air	67	°K/W

5.3 DC Characteristics

V_{BAT} = 6V to 30V and T_J = -40°C to +125°C. Typical values are given at V_{BAT} = 12V/25°C unless otherwise specified.

All voltages are defined with respect to GND. Positive currents flow into the IC.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Pin VBAT						
V_{BAT}	Battery supply voltage		6	-	30	V
$V_{BAT, ON}$	Battery Power On Voltage		-	-	5.0	V
$V_{BAT, OFF}$	Batter Power Off Voltage		3.5	-	-	V
I_{BAT}	Battery Supply current	SLP; V_{LIN} = $V_{BAT,}$ V_{BAT} = 12V	-	22	40	µA
		STB; V_{LIN} = $V_{BAT,}$ V_{BAT} = 12V	-	70	140	µA
		SLP; V_{LIN} = $V_{BAT,}$ V_{BAT} = 30V	-	32	72	µA
		STB; V_{LIN} = $V_{BAT,}$ V_{BAT} = 30V	-	80	150	µA
		NRM Recessive, VCC no load	-	1.0	2.0	mA
		NRM Dominant, VCC no load	-	2.0	4.0	mA
Pin VCC						
V_{CC}	LDO Output Voltage I_{VCC} = 0 to 100mA	5V option (V_{BAT} >= 6.5V)	4.75	5.0	5.25	V
		3.3V option (V_{BAT} >= 5.0V)	3.15	3.3	3.46	V

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
$V_{UVD, VCC}$	VCC Undervoltage detection	5V option	3.6	4.0	4.4	V
		3.3V option	2.3	2.6	2.9	V
$V_{UVR, VCC}$	VCC Undervoltage recovery	5V option	3.9	4.2	4.6	V
		3.3V option	2.4	2.7	3.0	V
$I_{LIM, VCC}$	LDO Current Limit	VCC short to GND	-260	-210	-160	mA
C_{VCC}	VCC decoupling capacitance	Minimum for stability	1.0	10	-	µF
PIN TXD						
$V_{IH, TXD}$	Input High voltage		$0.7V_{CC}$	-	$V_{CC}+0.3$	V
$V_{IL, TXD}$	Input Low voltage		-0.3	-	$0.3V_{CC}$	V
$R_{PU, TXD}$	Pull-up resistance	Pull up to VCC	4	8	12	kΩ
Pin RXD						
$V_{OH, RXD}$	Output High voltage	NRM, I_{OH} = 1mA	V_{CC}–0.5	-	-	V
$V_{OL, RXD}$	Output Low voltage	NRM, I_{OL} = 1mA	-	-	0.5	V
Pin EN						
$V_{IH, EN}$	High-level input voltage		2	-	-	V
$V_{IL, EN}$	Low-level input voltage		-	-	0.8	V
$R_{PD, EN}$	Pull-down resistance		80	130	180	kΩ
Pin RSTN						
$V_{OL, RSTN}$	Low-level output voltage	I_{OL} = 4mA	-	-	0.5	V
$V_{TH, RSTN}$	Input threshold voltage		1.0	1.4	1.8	V
$R_{PU, RSTN}$	Pull-up resistance	Pull up to VCC	4	6	8	kΩ
Pin LIN						
$V_{BUS, REC}$	Receive Recessive State		0.60	-	-	V_{BAT}
$V_{BUS, DOM}$	Receive Dominant State		-	-	0.40	V_{BAT}
$V_{BUS, CNT}$	Threshold Center Voltage	$V_{BUS, CNT} = (V_{BUS, REC}+V_{BUS, DOM})/2$	0.475	0.50	0.525	V_{BAT}
$V_{BUS, HYS}$	Receive Hysteresis	$V_{BUS, REC} - V_{BUS, DOM}$	0.05	0.10	0.175	V_{BAT}
V_{SERD}	Voltage drops of serial diode	I_{SERD} = 0.9mA (note 1)	0.4	-	1.0	V
$V_{OL, DOM}$	Dominant Output Voltage	$I_{OL, DOM}$ = 40mA	-	1.0	2.0	V
$I_{LIM, BUS}$	Current Limit of dominant state	$V_{BAT} = V_{LIN}$ = 18 V	50	75	100	mA
$I_{IL, REC}$	Receiver Input current, bus recessive state input	V_{BAT} = 7V, V_{LIN} = 18V	-	10	20	µA
$I_{IL, DOM}$	Receiver Input current, bus dominant state input	V_{BAT} = 12V, V_{LIN} = 0V	-600	-300	-	µA
$I_{BUS, NGND}$	Loss-of-ground current	V_{BAT}=GND=12V V_{LIN} = 0V – 18V	-1000	-	+1000	µA
$I_{BUS, NBAT}$	Loss-of-battery current	V_{BAT}=GND=0V, V_{LIN} = 0V - 18V	-	10	100	µA
$C_{IN, BUS}$	Capacitance on pin LIN	(note 1)	-	-	30	pF
R_{SLAVE}	Slave resistance	V_{BAT} = 12V, V_{LIN} = 0V	20	30	60	kΩ
Thermal Protection						

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
T_{JOTS}	Shutdown temperature	(note 1)	-	175	-	°C
T_{JOTR}	Recovery temperature	(note 1)	-	145	-	°C

Note 1: Not tested. Guaranteed by design and characterization.

5.4 AC Characteristics

V_{BAT} = 6V to 30V, T_J = -40°C to +125°C. Typical values are given at V_{BAT} = 12V/25°C unless otherwise specified. All voltages are defined with respect to GND. Positive currents flow into the IC.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
Duty Cycles						
D1	Duty Cycle 1 (note 1)	$V_{TH, REC, MAX}$ = 0.744 * V_{BAT}; $V_{TH, DOM, MAX}$ = 0.581 * V_{BAT}; V_{BAT} = 7.0V to 18V; T_{BIT} = 50μs; D1 = $T_{BUS, REC, MIN}$ / (2 x T_{BIT})	0.396	-	-	-
D2	Duty Cycle 2 (note 1)	$V_{TH, REC, MIN}$ = 0.422 * V_{BAT}; $V_{TH, DOM, MIN}$ = 0.284 * V_{BAT}; V_{BAT} = 7.6V to 18V; T_{BIT} = 50μs; D2 = $T_{BUS, REC, MAX}$ / (2 * T_{BIT})	-	-	0.581	-
D3	Duty Cycle 3 (note 1)	$V_{TH, REC, MAX}$ = 0.778 * V_{BAT}; $V_{TH, DOM, MAX}$ = 0.616 * V_{BAT}; V_{BAT} = 7.0V to 18V; T_{BIT} = 96μs; D3 = $T_{BUS, REC, MIN}$ / (2 * T_{BIT})	0.471	-	-	-
D4	Duty Cycle 4 (note 1)	$V_{TH, REC, MIN}$ = 0.389 * V_{BAT}; $V_{TH, DOM, MIN}$ = 0.251 * V_{BAT}; V_{BAT} = 7.6V to 18V; T_{BIT} = 96μs; D4 = $T_{BUS, REC, MAX}$ / (2 * T_{BIT})	-	-	0.590	-
Timing Characteristics						
$T_{PD, RXF}$, $T_{PD, RXR}$	Receive Propagation Delay	C_{RXD} = 20pF	-	2	6	μs
$T_{SYM, RX}$	Receive propagation delay symmetry	C_{RXD} = 20pF	-2	0	+2	μs
T_{WAKEUP}	Remote wakeup time		30	80	150	μs
$T_{DOM, TO}$	TXD dominant time-out time		6	-	20	ms
$T_{MD, SEL}$	Mode transition time	Note 1	5	15	25	μs
$T_{PD, TX}$	Transmit Propagation Delay	R_{LIN} = 500, C_{LIN} = 220pF	-	-	15	μs
$T_{EN, TX}$	Enable time from EN to TXD		0	-	1	μs
T_{RSTN}	RSTN extension time		2	4	8	ms

Note 1: Not tested. Guaranteed by design and characterization.

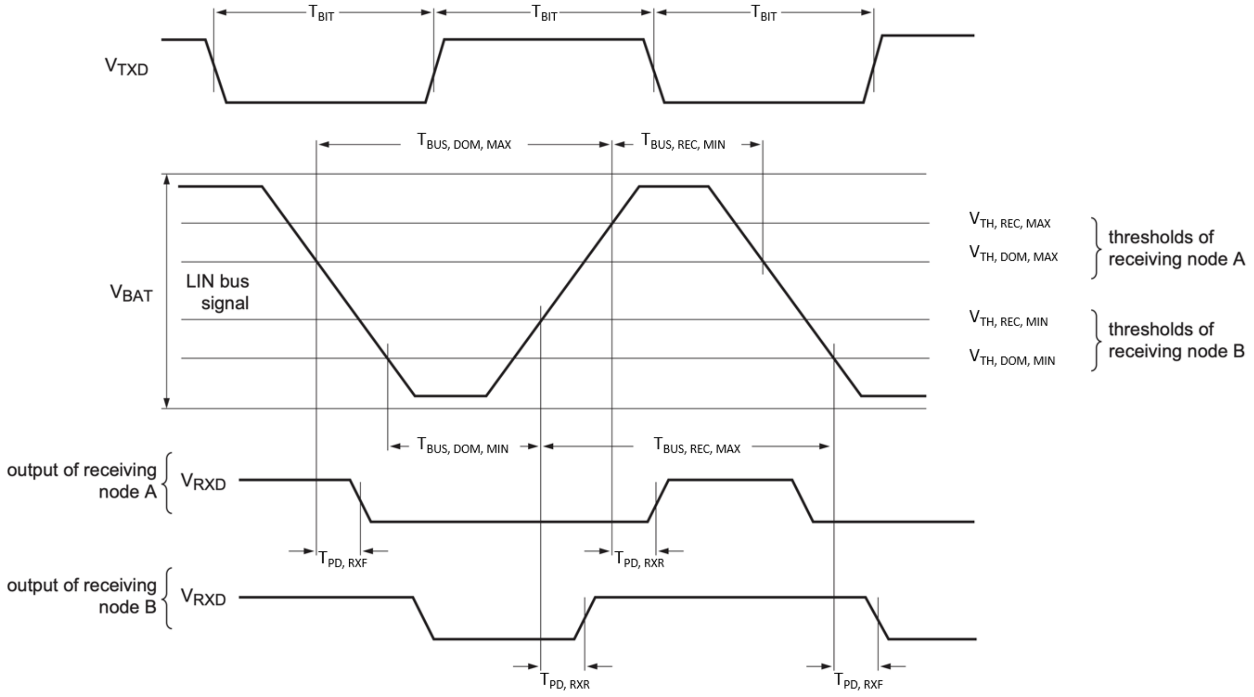


Figure 5-1 Definition of Bus Timing Parameters

6. Application Circuit

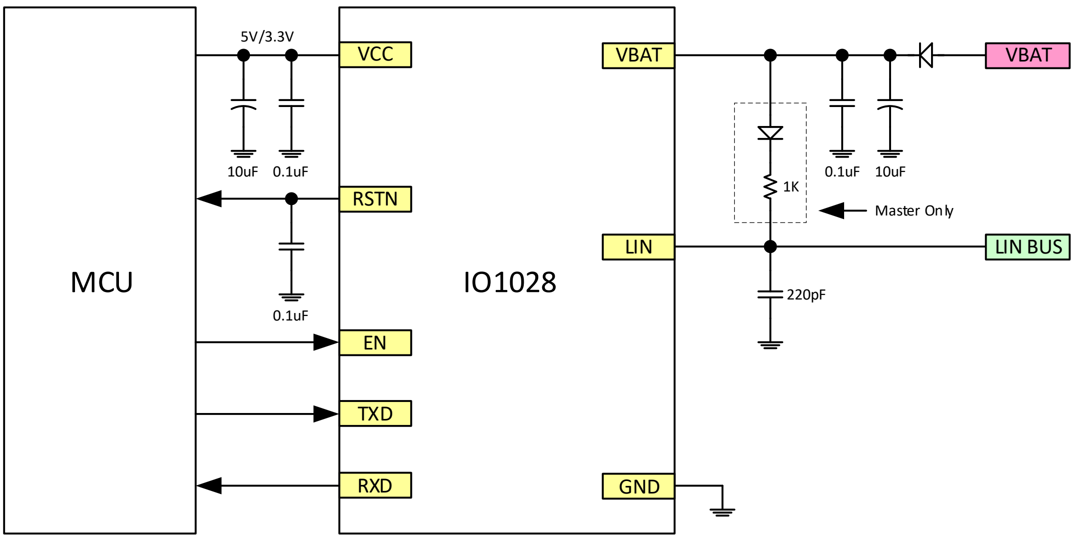
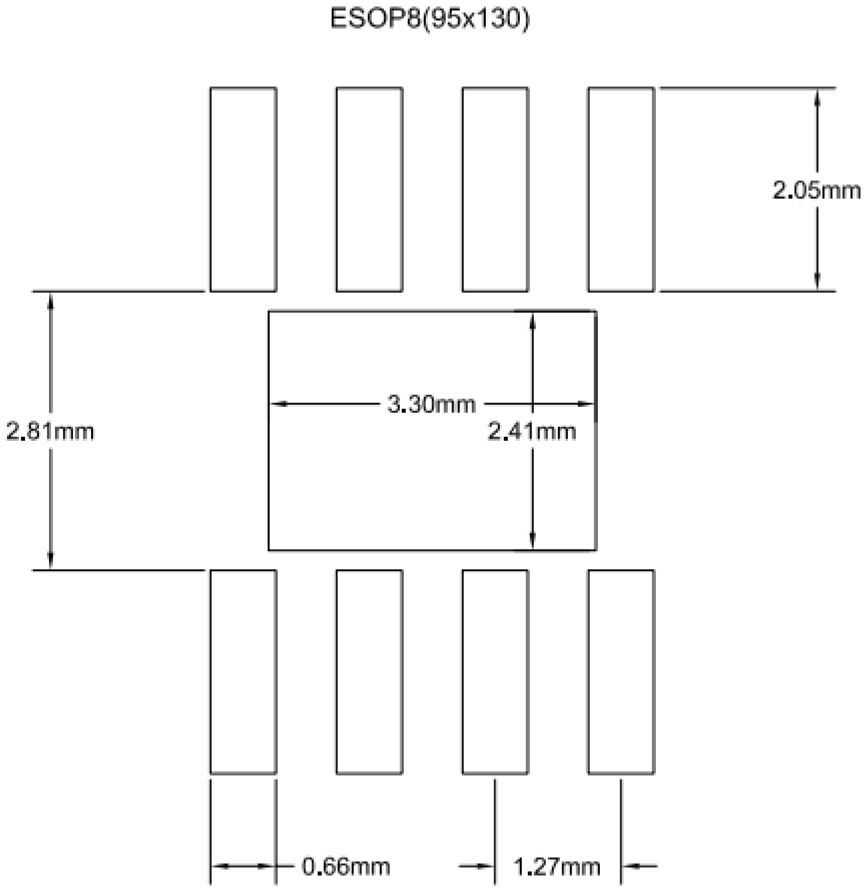


Figure 6-1 Application Circuit Diagram

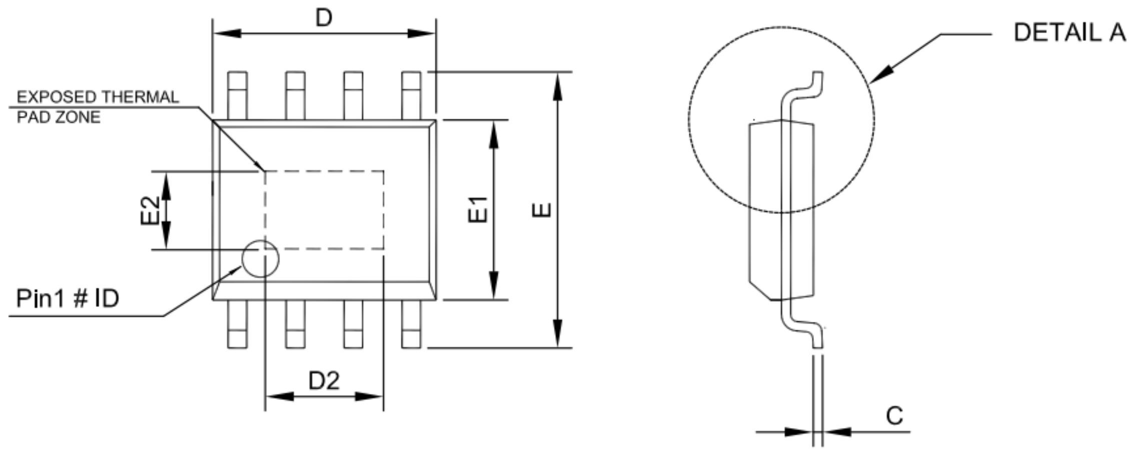
7. Packaging Outline

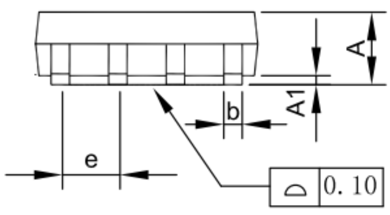
7.1 eSOP-8 Package Outline

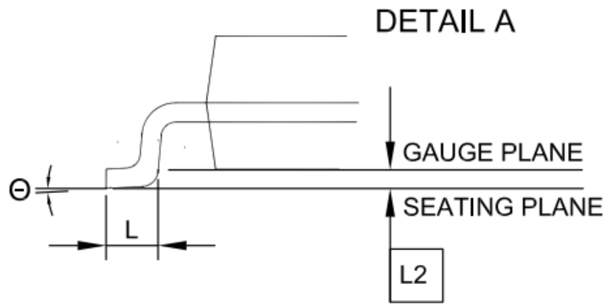
7.1.1 RECOMMENDED LAND PATTERN



7.1.2 POD







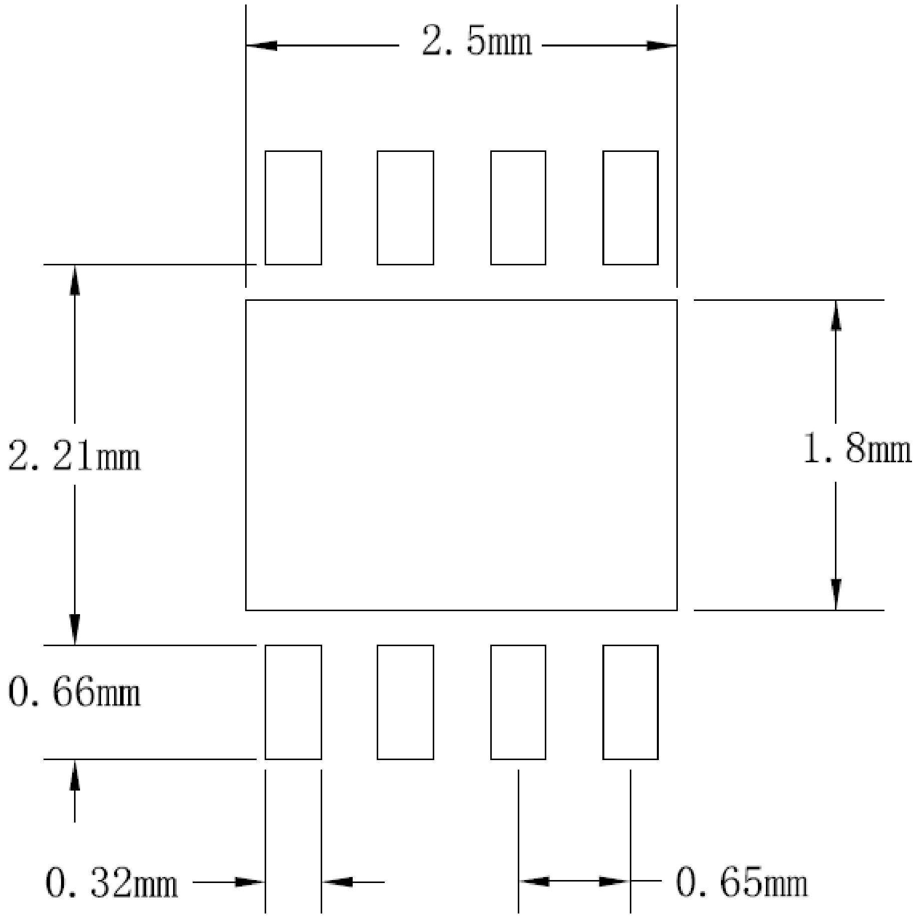
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	–	–	1.70
A1	–	–	0.15
E1	3.70	3.90	4.10
E	5.80	6.00	6.20
D	4.70	4.90	5.10
b	0.31	–	0.51
e	1.27BSC		
L	0.40	–	1.27
L2	0.25BSC		
θ	0°	–	8°
C	0.10	–	0.25
D2	1.50	–	–
E2	1.00	–	–

NOTE:

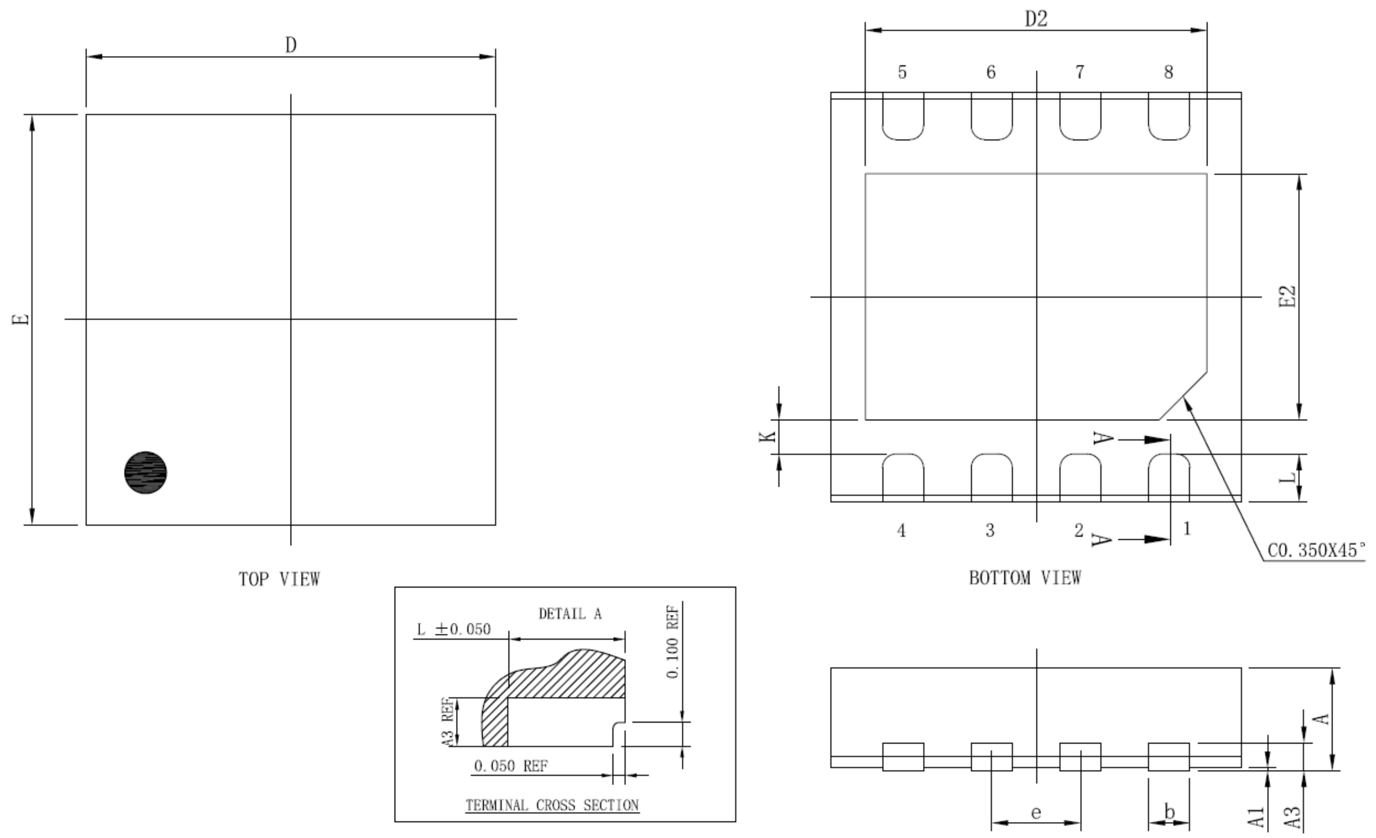
1. CONTROLLING DIMENSION: MM
2. DIMENSION D DOES NOT INCLUDE MODE FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMESION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. PEFERENCE DOCUMENT: JEDEC MS-012
5. THE SHAPE OF BODY AND THERMAL PAD SHOW DIFFERENT SHAPE AMONG DIFFERENT FACTORIES.

7.2 WDFN-8 Package Outline

7.2.1 RECOMMENDED LAND PATTERN



7.2.2 POD



SYMBOLS	MIN.	NOM.	MAX.
A	0. 70	0. 75	0. 80
A1	0. 00	0. 02	0. 05
A3	0. 203 REF.		
b	0. 25	0. 30	0. 35
D	2. 90	3. 00	3. 10
E	2. 90	3. 00	3. 10
e	0. 65 BSC		
L	0. 30	0. 35	0. 40
D2	2. 45	2. 50	2. 55
E2	1. 75	1. 80	1. 85
K	0. 20	—	—

NOTE:
1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-229F

8. Ordering Information

Operating temperature -40°C to 105°C

Order Part No.	Package	QTY/Reel	Remark
IS32IO1028A-GRLA2-TR	SOP-8 with exposed pad, Lead-free	2500/Reel	VCC=5V
IS32IO1028B-GRLA2-TR	SOP-8 with exposed pad, Lead-free	2500/Reel	VCC=3.3V
IS32IO1028A-DWLA2-TR	Wettable flank DFN-8, Lead-free	2500/Reel	VCC=5V
IS32IO1028B-DWLA2-TR	Wettable flank DFN-8, Lead-free	2500/Reel	VCC=3.3V

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a.) the risk of injury or damage has been minimized;
b.) the user assumes all such risks; and
c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances.

9. ERRATA

10. Revisions

Revision	Detailed Information	Date
0B	A preliminary release.	2022.06.09
0C	Add D1~D4 duty cycle spec. and Figure 3. Definition of Bus Timing Parameters	2022.12.29
0D	Add WDFN-8 package and its corresponding ordering information. Update battery current with 12V/30V separation Update application circuits Relabel Figure 3 as Figure1	2023.08.08
A	Product Release 1. Add "TSCA compliance" in product Features 2. Figure 3-1 State Operation Diagram Von→$V_{BAT, ON}$, VOFF →$V_{BAT, OFF}$ 3. P.6 RTHJA→Rth(j-a) 4. P.7 PIN LIN $V_{BUS, REC}$:Receive Recessive Threshold →Receive Recessive State $V_{BUS, DOM}$:Receive Dominant Threshold →Receive Dominant State 5. AC Characteristics V_{BAT} = 6V to 3V, T_J = -40°C to +125°C→V_{BAT} = 6V to 30V, T_J = -40°C to +125°C 6. Figure 6-1 Application Circuit Diagram BAT→VBAT 7. Ordering Information Operating temperature -40°C to 125°C→Operating temperature -40°C to 105°C 8. Revisions 0D eDFN-8→WDFN-8	2023.09.22