

M100PF Hardware Manual

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CHAPTER

ONE

ABOUT THIS MANUAL

1.1 Imprint

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1.2 Disclaimer

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1.5 Care and Maintenance

- Keep the device dry. Precipitation, humidity, and all types of liquids or moisture can contain minerals that will corrode electronic circuits. If your device does get wet, allow it to dry completely.
- Do not use or store the device in dusty, dirty areas. Its moving parts and electronic components can be damaged.
- Do not store the device in hot areas. High temperatures can shorten the life of electronic devices, damage batteries, and warp or melt certain plastics.
- Do not store the device in cold areas. When the device returns to its normal temperature, moisture can form inside the device and damage electronic circuit boards.
- Do not attempt to open the device.
- Do not drop, knock, or shake the device. Rough handling can break internal circuit boards and fine mechanics.
- Do not use harsh chemicals, cleaning solvents, or strong detergents to clean the device.
- Do not paint the device. Paint can clog the moving parts and prevent proper operation.
- Unauthorized modifications or attachments could damage the device and may violate regulations governing radio devices.

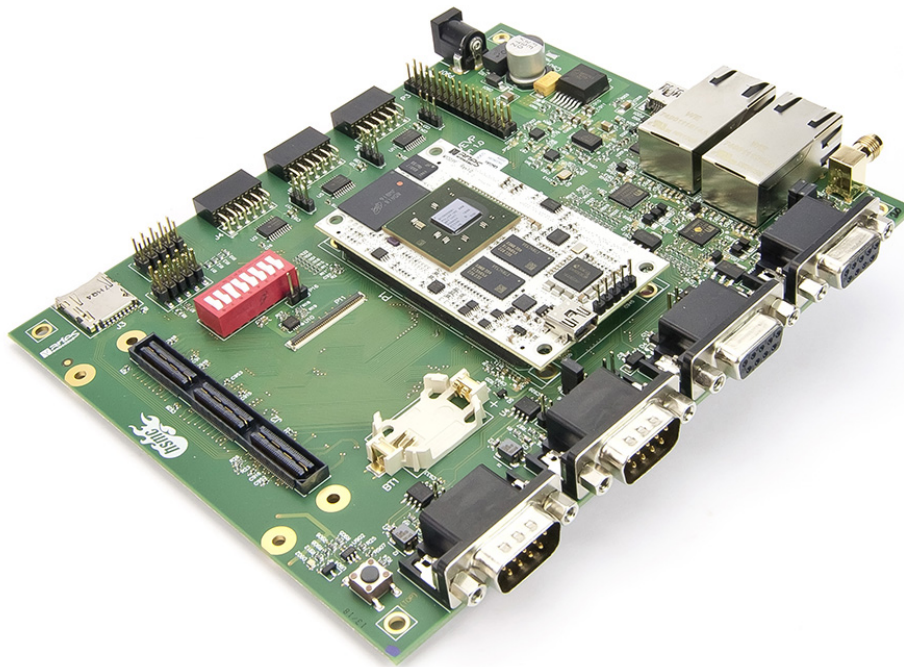
1.6 Change Log

Revision	Date	Revised	Comment
1.0	04.06.2019	js	Initial creation
1.1	12.01.2022	dk	I2C0/I2C1 connections changed
1.2.1	14.10.2022	dk	Connector Location added

CHAPTER**TWO**

OVERVIEW**2.1 M100PF**

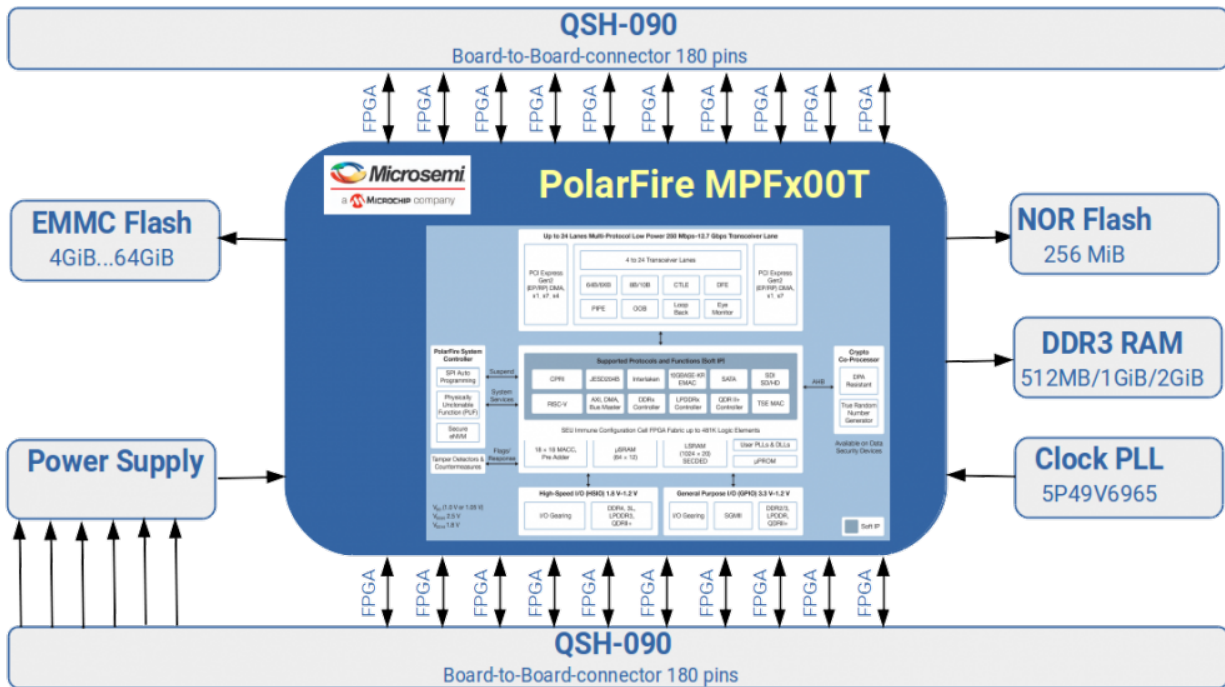
The M100PF is based on the PolarFire FPGA family by Microchip. The SoM targets demanding industrial and medical applications and offers the full flexibility of the populated FPGAs. The populated FPGAs deliver the industry's lowest power at mid-range densities with exceptional security and reliability. The FPGA SoM for Embedded Applications spans from 100K logic elements (LEs) to 300K LEs, features 12.7G transceivers and offers up to 50% lower power than competing mid-range FPGAs.



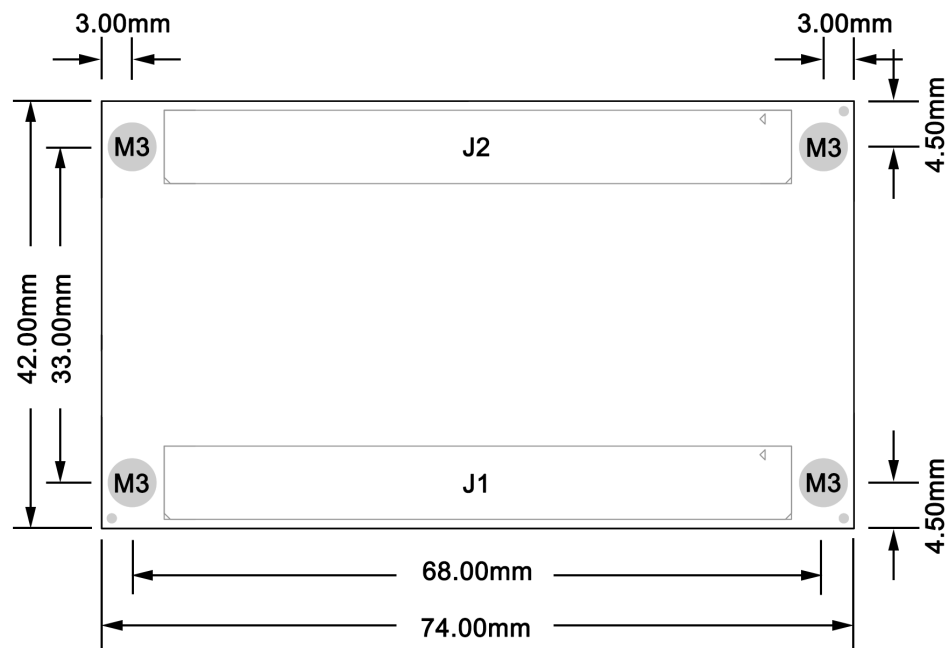
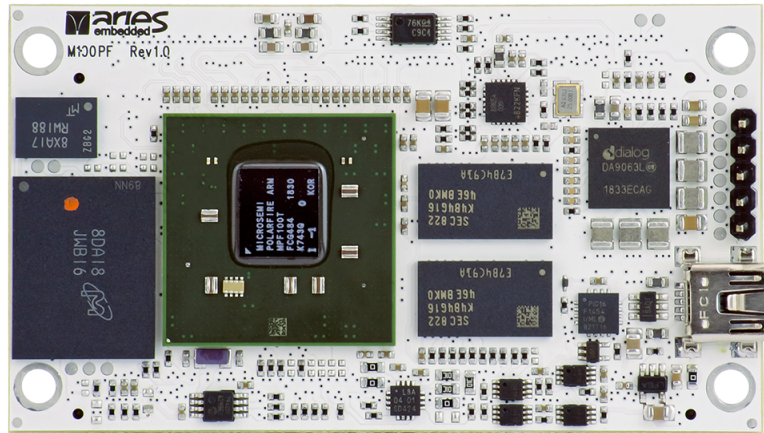
2.2 Feature Set

- Microchip PolarFire FPGA
 - MPF100T - 109KLE, 336 Math Blocks (18x18MACC)
 - MPF200T - 192KLE, 588 Math Blocks (18x18MACC)
 - MPF300T - 300KLE, 924 Math Blocks (18x18MACC)
- 512 MiB / 1 GiB / 2 GiB DDR3 RAM
- 128 MiB configuration SPI NOR Flash
- 4 GiB to 64 GiB eMMC memory
- 8 SERDES Lanes, 250Mbps to 12.7 Gbps
- 2 PCIe Gen2 End Points/Root Ports
- Clock distribution
- single 3,3V supply
- size 74mmx42mm
- 2 x Samtec QSH-090-01-F-D-A board-to-board interconnect
- commercial (0°C...+70°C) / industrial (-40°C...+85°C) temperature range

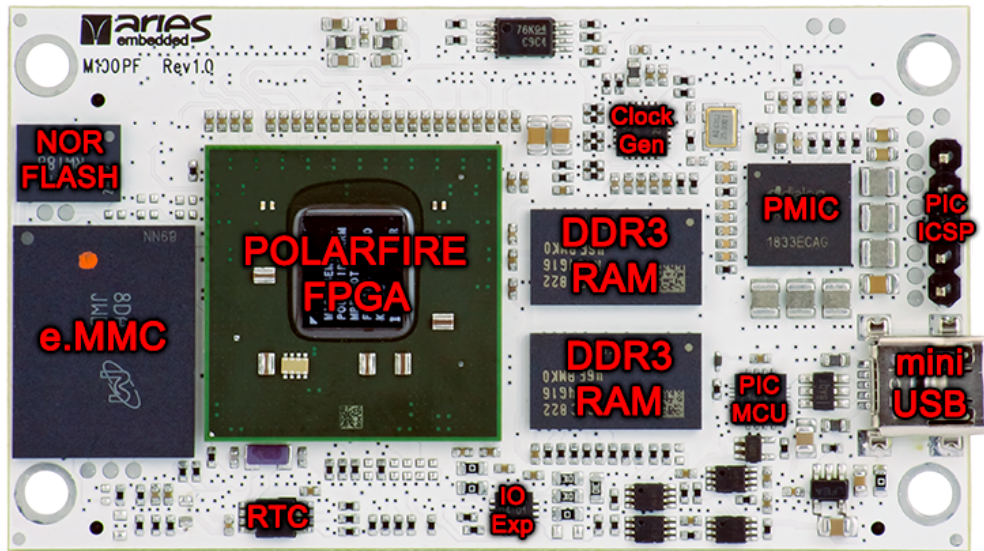
2.3 Block Diagram



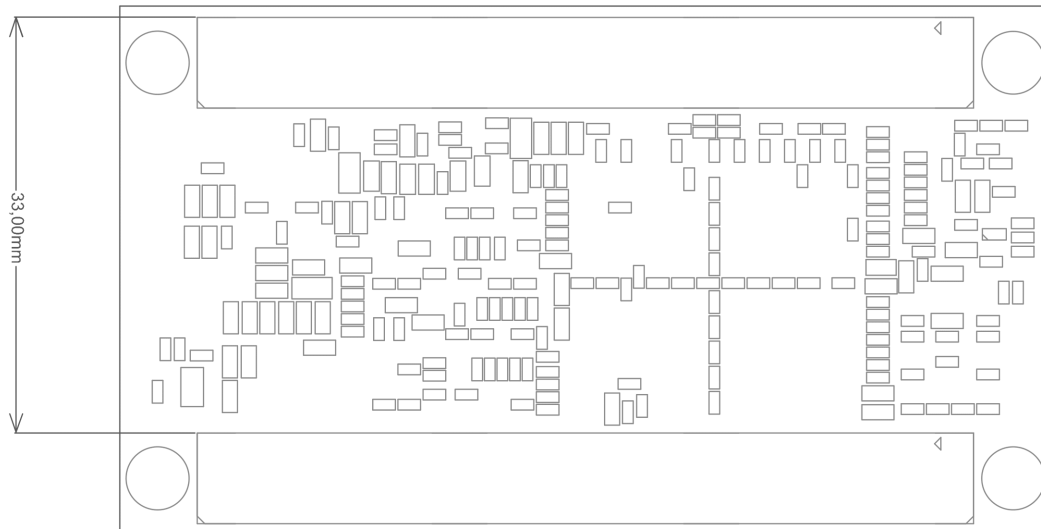
2.4 Dimensions



2.5 Part Overview

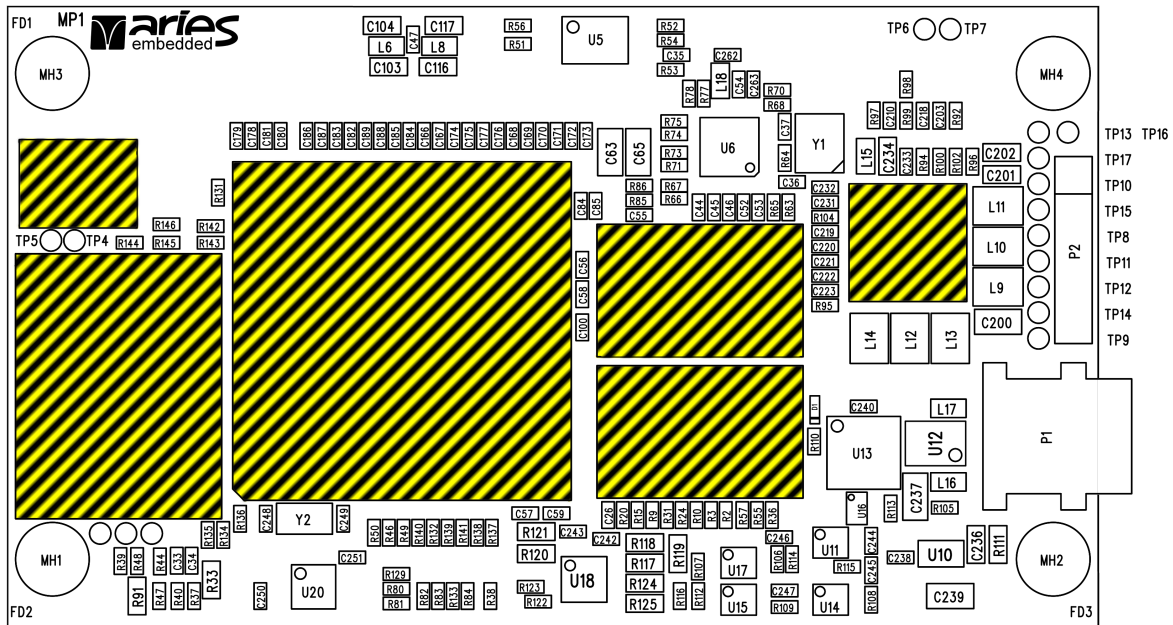


Connector Location:



2.6 Handling Recommendations

The populated Samtec connectors require certain mechanical force to insert the SoM into its mating base-board connectors. To avoid mechanical damage to the components populated on M100PF it is strongly recommended not to apply mechanical force on the Ball Grid Array (BGA) components. The BGA components are marked as shaded in the figure below:



RESOURCES**3.1 Components****3.1.1 FPGA**

The Polarfire FPGA on the M100PF comes in the FCG484 (23x23, 1.0 mm) package and up provides to 244 User I/O (96 HSIO, 148 GPIO) and 8 XCVRs.

Features	MPF100T	MPF200T	MPF300T
Logic Elements (4 LUT + DFF)	109K	192K	300K
Math Blocks (18x18 MACC)	336	588	924
LSRAM Blocks (20K Bit)	352	616	952
uSRAM Blocks (64x12)	1008	1764	2772
Total RAM Mbits	7.6 Mbits	13.3 Mbits	20.6 Mbits
uPROM Kbits	297 Kbits	297 Kbits	459 Kbits
User DLL's / PLL's	8	8	8

For more information about the Polarfire FPGA please refer to the [Microchip documentation](#).

3.1.2 DDR3-RAM

The M100PF is equipped with 2 pieces of Samsung K4B4G1646E resulting in up to 2 GB of DDR3 memory. The memory interface is clocked at 400 MHz using the 1.5V DDR3 standard. For low power applications it is possible to set the RAM to DDR3L mode at 1.35V and reconfigure the PMIC to provide this voltage.

Function	FPGA Pin	Function	FPGA Pin
DDR3_A0	U17	DDR3_A1	T17
DDR3_A2	W16	DDR3_A3	V16
DDR3_A4	Y16	DDR3_A5	AA16
DDR3_A6	R16	DDR3_A7	T16
DDR3_A8	Y14	DDR3_A9	W14
DDR3_A10	AB12	DDR3_A11	AA12
DDR3_A12	AB13	DDR3_A13	AA13
DDR3_A14	Y13	DDR3_A15	W13
DDR3_DQ0	R15	DDR3_DQ1	U13
DDR3_DQ2	T13	DDR3_DQ3	U15
DDR3_DQ4	V15	DDR3_DQ5	T11
DDR3_DQ6	R12	DDR3_DQ7	U14
DDR3_DQ8	Y9	DDR3_DQ9	V10
DDR3_DQ10	V9	DDR3_DQ11	R10
DDR3_DQ12	R9	DDR3_DQ13	U9
DDR3_DQ14	U8	DDR3_DQ15	T8
DDR3_DQ16	Y8	DDR3_DQ17	AA8
DDR3_DQ18	AB7	DDR3_DQ19	AA7
DDR3_DQ20	W8	DDR3_DQ21	W7
DDR3_DQ22	AA6	DDR3_DQ23	Y6
DDR3_DQ24	AB4	DDR3_DQ25	AB3
DDR3_DQ26	W6	DDR3_DQ27	V6
DDR3_DQ28	AB2	DDR3_DQ29	AA2
DDR3_DQ30	AA3	DDR3_DQ31	Y3

Function	FPGA Pin	Function	FPGA Pin
DDR3_DQS0_N	T12	DDR3_DQS0_P	R13
DDR3_DQS1_N	U10	DDR3_DQS1_P	T10
DDR3_DQS2_N	AB5	DDR3_DQS2_P	AA5
DDR3_DQS3_N	Y5	DDR3_DQS3_P	Y4
DDR3_DM0	V14	DDR3_DM1	T7
DDR3_DM2	V7	DDR3_DM3	W4
DDR3_BA0	AA10	DDR3_BA1	AA11
DDR3_BA2	AB10	DDR3_RAS_N	Y11
DDR3_CAS_N	W12	DDR3_WE_N	V12
DDR3_CS_N	AB9	DDR3_CKE	AB8
DDR3_ODT	Y10	DDR3_RESET_N	W11
DDR3_REF_CLK_N	AA15	DDR3_REF_CLK_P	Y15
DDR3_CK_N	AA17	DDR3_CK_P	AB17

3.1.3 eMMC Flash

M100PF features up to 64 GB of eMMC Flash using Micron MTFC4GACAANA-4M IT.

Function	FPGA Pin
RSTN	B7
CMD	D8
CLK	P6
DAT0	A7
DAT1	A6
DAT2	D9
DAT3	E9
DAT4	A8
DAT5	B8
DAT6	B13
DAT7	B12

3.1.4 SPI NOR Flash

The [MT25QU01GBBB8E12](#) SPI NOR Flash provides 128 MiB of non-volatile storage. On power-up the SPI NOR is connected to the FPGA, allowing the FPGA to load one of multiple configuration images stored on the SPI Flash. See [SPI Configuration and Programming](#) for more.

Function	FPGA Pin as master (connected to SPI Flash)	FPGA Pin as slave (connected to PIC)
SPI_EN	H10	H10
IO_CFG	G9	G9
SCK	G3	G3
SDI	G10	G5
SDO	G5	G10
nSS	G4	G4

3.1.5 PMIC

Power on the M100PF is controlled by a factory programmed Dialog [DA9063L-00](#) PMIC. It is accessible by the PIC via I2C on address 0x5A.

3.1.6 IO-Expander

A [PCAL6408ABS](#) 8-bit IO-Expander controls the SPI configuration, the JTAG Test-Reset and 2 reset signals. It is accessible from PIC via I2C at address 0x20. On power-up all GPIO pins of the IO-Expander are configured as inputs, weak pull-up and pull-down resistors ensure that the signals are at their default value. To modify the signals, change the corresponding pins to output and update their value.

Bit	Default	Connection	Description
0x01	1	PF_SPI_EN	Enable FPGA connection to SPI
0x02	1	PF_IO_CFG	Enable SPI Flash connection to SPI
0x04	0	PIC_SPI_EN	Enable PIC connection to SPI
0x08	0	--	Not connected
0x10	1	JTAG_TRSTN	JTAG Test Reset Signal
0x20	1	PF_FF	Disable Polarfire Flash Freeze
0x40	1	PF_RESET_N	Resets Polarfire when pulled low
0x80	1	PMIC_nRESET	Resets Power when pulled low

For a list of valid SPI configurations see [SPI Configuration and Programming](#).

3.1.7 PIC Microcontroller

The M100PF features a Microchip [PIC16F1454](#) microcontroller, which is connected to USB, via SPI and UART to FPGA and SPI Flash and to the PIC I2C bus as a master, serving as a USB-to-I2C bridge. Additionally it can be used to program the FPGA or to update the configuration stored in the SPI NOR Flash. The most recent firmware can be found on Github: <https://github.com/ARIES-Embedded>

3.1.8 RTCC

The Microchip [MCP794xx](#) Real-Time-Clock-Calender with integrated EEPROM uses an on-board 32.768 kHz crystal. The RTCC is connected to I2C using address 0x6F, the EEPROM uses address 0x57.

Function	FPGA Pin	Description
RTC_MFP	J9	RTC multi function pin

3.1.9 SERDES

M100PF provides 8 SERDES lanes each with up to 12.7 Gbps datarate.

Function	FPGA Pin	Connector	Function	FPGA Pin	Connector
SERDES_0_RX0_P	M22	9 (J2 A)	SERDES_0_RX0_N	M21	11 (J2 A)
SERDES_0_TX0_P	P22	15 (J2 A)	SERDES_0_TX0_N	P21	17 (J2 A)
SERDES_0_RX1_P	T22	21 (J2 A)	SERDES_0_RX1_N	T21	23 (J2 A)
SERDES_0_TX1_P	V22	27 (J2 A)	SERDES_0_TX1_N	V21	29 (J2 A)
SERDES_0_RX2_P	W20	33 (J2 A)	SERDES_0_RX2_N	W19	35 (J2 A)
SERDES_0_TX2_P	Y22	39 (J2 A)	SERDES_0_TX2_N	Y21	41 (J2 A)
SERDES_0_RX3_P	AA20	45 (J2 A)	SERDES_0_RX3_N	AA19	47 (J2 A)
SERDES_0_TX3_P	AB22	51 (J2 A)	SERDES_0_TX3_N	AB21	53 (J2 A)
SERDES_1_RX0_P	A20	10 (J2 A)	SERDES_1_RX0_N	A19	12 (J2 A)
SERDES_1_TX0_P	B22	16 (J2 A)	SERDES_1_TX0_N	B21	18 (J2 A)
SERDES_1_RX1_P	C20	22 (J2 A)	SERDES_1_RX1_N	C19	24 (J2 A)
SERDES_1_TX1_P	D22	28 (J2 A)	SERDES_1_TX1_N	D21	30 (J2 A)
SERDES_1_RX2_P	F22	34 (J2 A)	SERDES_1_RX2_N	F21	36 (J2 A)
SERDES_1_TX2_P	H22	40 (J2 A)	SERDES_1_TX2_N	H21	42 (J2 A)
SERDES_1_RX3_P	L20	46 (J2 A)	SERDES_1_RX3_N	L19	48 (J2 A)
SERDES_1_TX3_P	K22	52 (J2 A)	SERDES_1_TX3_N	K21	54 (J2 A)

3.2 SPI Configuration and Programming

FPGA, PIC and SPI Flash are connected on a shared SPI interface. Each component can be enabled and disabled by writing to the PCAL6408ABS I2C-IO-Expander device at address 0x20. By default the PIC SPI is disabled and the FPGA is connected to the SPI NOR Flash as master. This allows the FPGA to load configuration images stored on the Flash. After altering the SPI Configuration via [IO-Expander](#), the PIC microcontroller can update the Flash with the user's image or even directly program the FPGA. For more information about programming the Polarfire FPGA see the [PolarFire FPGA Programming User Guide \(UG0714\)](#).

The following SPI configurations are valid:

Hex	PIC_SPI_EN	PF_IO_CFG	PF_SPI_EN	Polarfire SPI Mode	SPI Connection
x6	1	1	0	disable	PIC -> SPI Flash
x5	1	0	1	SPI slave	PIC -> Polarfire
x3	0	1	1	SPI master (default)	Polarfire -> SPI Flash

If the FPGA is configured as SPI slave, then its data directions are swapped.

3.3 Clocking

The clocking scheme on the M100PF is generated by an IDT 5P49V6965 Clock Generator (PLL). Its base is sourced from a 25 MHz oscillator to generate the required clocks for the board's components. The IDT 5P49V6965 is accessible from FPGA on the I2C 1 bus at address 0xD4 for reconfiguration. The Polarfire FPGA itself provides an internal 2 MHz and an internal 160 MHz oscillator. A 32.768 KHz crystal on the board provides the required frequency for the RTCC.

3.4 I2C

The following devices on the I2C bus (I2C PIC) are accessible through the PIC microcontroller:

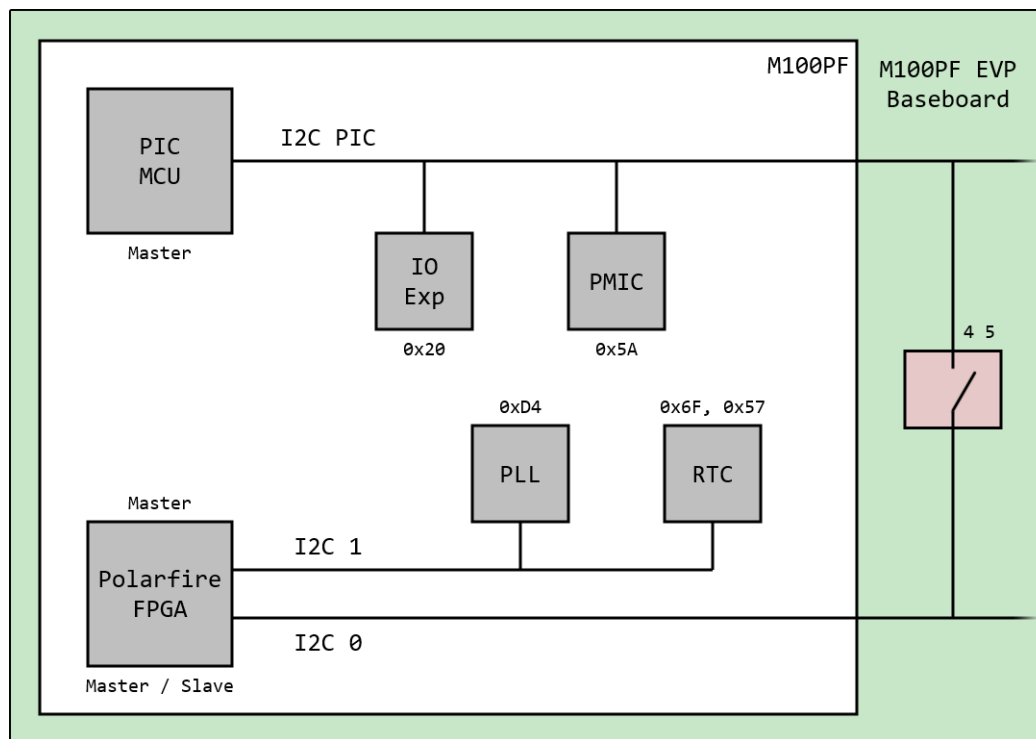
I2C PIC		
Ad- dress	Device	Description
0x20	PCAL6408ABS IO-Expander	Used for configuration of the SPI connection and to issue a reset signal to the Polarfire or PMIC.
0x5A	DA9063L-00 PMIC	Allows reconfiguration of voltage levels around the board.
Master	PIC	

The Polarfire FPGA is connected to I2C bus 0 (I2C 0) as master or slave and to I2C bus 1 (I2C 1) as master.

I2C 1		
Ad- dress	Device	Description
0xD4	5P49V6965 Clock Generator	Allows reconfiguration of the clocks present on M100PF
0x57	MCP794xx	EEPROM of the RTCC
0x6F	MCP794xx	Real Time Clock Calendar
Master	Polarfire FPGA	Connected to FPGA Pins J4 (SCL) and H4 (SDA)

Function	FPGA Pin	Connector
PIC_SDA	--	165 (J2 C)
PIC_SCL	--	167 (J2 C)
I2C0_SDA	H6	126 (J2 C)
I2C0_SCL	H5	139 (J2 C)
I2C1_SDA	H4	--
I2C1_SCL	J4	--

The following figure provides an overview of the I2C busses:



The M100PFEVP Baseboard allows the user to connect the busses I2C PIC and I2C 0 together by closing switch S1 pin 4 and 5.

Note that the PIC currently does not support multi-master communication.

3.5 JTAG

The M100PFEVP Baseboard provides a JTAG header for the FlashPro programmer to program the FPGA using Microchip's standard tools. The PCAL6408ABS IO-Expander is connected to Test-Reset via bit 0x10.

Function	FPGA Pin	Connector
TCK	F8	6 (J1 A)
TMS	F7	10 (J1 A)
TDI	G8	8 (J1 A)
TDO	F6	4 (J1 A)
TRSTB	G7	2 (J1 A)
VIO	1.8V	12 (J1 A)

3.6 UART

The FPGA and PIC microcontroller are connected via UART providing access to the FPGA from the host PC. The PIC uses the CDC-ACM interface to communicate with the host. On the Linux Operating System it is visible as `/dev/ttyACMx` device.

Function	FPGA Pin
UART_TX	N2
UART_RX	P2

Furthermore two additional UART are routed to the connector.

Function	FPGA Pin	Connector
UART0_TX	K8	Pin 132 (J2 C)
UART0_RX	J8	Pin 138 (J2 C)
UART1_TX	K6	Pin 75 (J1 B)
UART1_RX	J7	Pin 77 (J1 B)

These signals refer to the functionality available on the M100PFEVP baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

3.7 Pin Out

3.7.1 CAN

Function	FPGA Pin	Connector
CAN0_TX	F17	129 (J2 C)
CAN0_RX	G17	137 (J2 C)
CAN1_TX	F16	135 (J2 C)
CAN1_RX	F15	130 (J2 C)

These signals refer to the functionality available on the M100PFEVP baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

3.7.2 Ethernet

Function	FPGA Pin	Connector	Function	FPGA Pin	Connector
ETH0_MDIO	A17	115 (J2 B)	ETH1_MDIO	P7	164 (J1 C)
ETH0_MDC	B15	112 (J2 B)	ETH1_MDC	N8	161 (J1 C)
ETH0_GTXCLK	B14	113 (J2 B)	ETH1_GTXCLK	P4	159 (J1 C)
ETH0_TX_EN	C17	114 (J2 B)	ETH1_TX_EN	T3	172 (J1 C)
ETH0_TXD0	C16	106 (J2 B)	ETH1_TXD0	T2	174 (J1 C)
ETH0_TXD1	A16	107 (J2 B)	ETH1_TXD1	P3	163 (J1 C)
ETH0_TXD2	A15	108 (J2 B)	ETH1_TXD2	N4	171 (J1 C)
ETH0_TXD3	H13	105 (J2 B)	ETH1_TXD3	R4	166 (J1 C)
ETH0_RXC	G14	118 (J2 B)	ETH1_RXC	R5	110 (J1 B)
ETH0_RXD0	G15	110 (J2 B)	ETH1_RXD0	R8	169 (J1 C)
ETH0_RXD1	H15	116 (J2 B)	ETH1_RXD1	P9	170 (J1 C)
ETH0_RXD2	D17	111 (J2 B)	ETH1_RXD2	R6	168 (J1 C)
ETH0_RXD3	D16	109 (J2 B)	ETH1_RXD3	P6	173 (J1 C)
ETH0_RX_DV	E16	117 (J2 B)	ETH1_RX_DV	P8	165 (J1 C)

These signals refer to the functionality available on the M100PFEVP baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

3.7.3 SD Card

Function	FPGA Pin	Connector
SD_CLK	A2	33 (J1 A)
SD_DAT0	C12	35 (J1 A)
SD_DAT1	C11	37 (J1 A)
SD_DAT2	C9	27 (J1 A)
SD_DAT3	B10	29 (J1 A)
SD_CMD	B9	31 (J1 A)
SD_DETECT	C10	39 (J1 A)

These signals refer to the functionality available on the M100PFEVP baseboard. When using a custom baseboard the connections can be used as GPIO, however for some signals there may be resistors present.

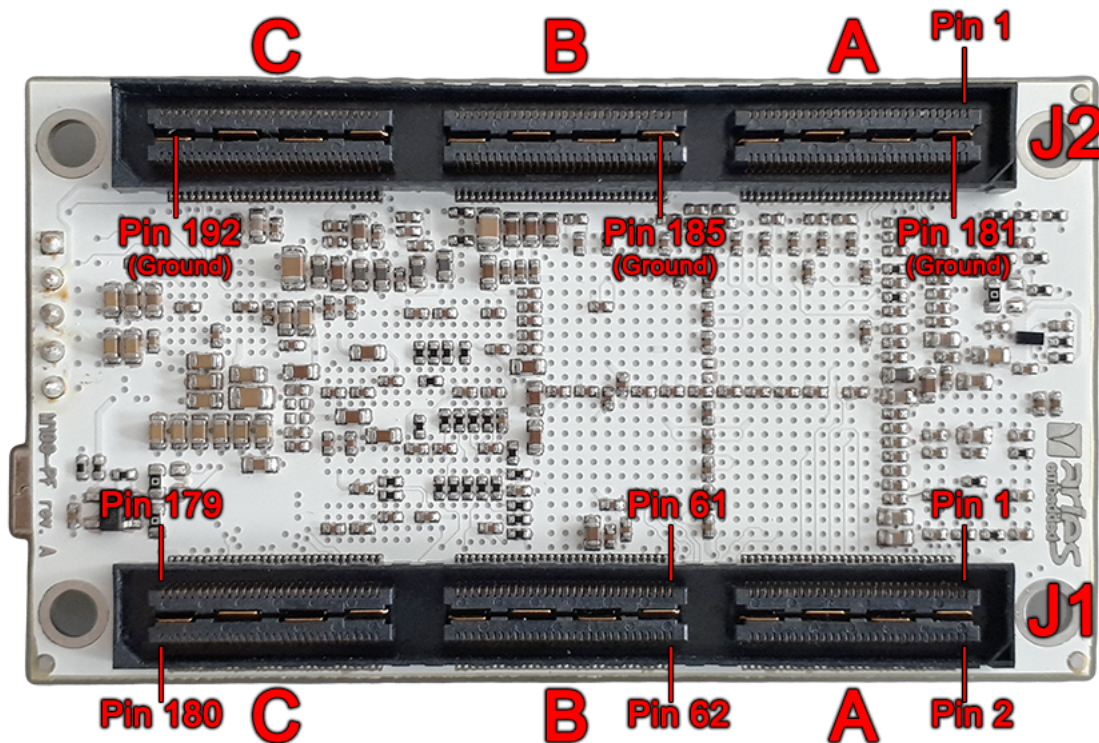
3.7.4 GPIO

The following pins are available for GPIO:

FPGA	Connector		FPGA	Connector		FPGA	Connector		FPGA	Connector
A3	30 (J1 A)		D11	149 (J2 C)		F12	147 (J2 C)		L7	80 (J2 B)
A5	54 (J1 A)		D12	153 (J2 C)		F13	131 (J2 C)		L8	156 (J2 C)
A12	41 (J1 A)		D13	145 (J2 C)		G2	64 (J1 B)		M2	72 (J1 B)
A13	15 (J1 A)		D14	92 (J2 B)		G12	152 (J2 C)		M3	134 (J2 C)
B2	38 (J1 A)		E3	34 (J1 A)		G13	154 (J2 C)		M4	122 (J2 C)
B3	36 (J1 A)		E4	50 (J1 A)		H1	74 (J1 B)		M5	133 (J2 C)
B4	56 (J1 A)		E5	40 (J1 A)		H2	66 (J1 B)		M7	90 (J2 B)
B5	47 (J1 A)		E6	60 (J1 A)		J1	76 (J1 B)		M8	136 (J2 C)
B17	17 (J1 A)		E8	45 (J1 A)		J2	68 (J1 B)		M9	128 (J2 C)
C2	28 (J1 A)		E10	146 (J2 C)		J3	144 (J2 C)		N1	133 (J1 C)
C4	46 (J1 A)		E11	70 (J2 B)		K1	78 (J1 B)		N5	123 (J2 C)
C5	49 (J1 A)		E13	143 (J2 C)		K3	150 (J2 C)		N6	127 (J2 C)
C6	51 (J1 A)		E14	79 (J2 B)		K4	93 (J2 B)		N7	121 (J2 C)
C7	53 (J1 A)		F1	112 (J1 B)		K5	97 (J2 B)		P1	131 (J1 C)
C14	89 (J2 B)		F2	160 (J1 C)		L1	167 (J1 C)		R1	120 (J1 B)
C15	96 (J2 B)		F3	52 (J1 A)		L2	70 (J1 B)		R3	115 (J1 B)
D3	32 (J1 A)		F5	42 (J1 A)		L3	125 (J2 C)		T1	118 (J1 B)
D4	48 (J1 A)		F10	155 (J2 C)		L5	172 (J2 C)		T5	113 (J1 B)
D6	58 (J1 A)		F11	71 (J2 B)		L6	94 (J2 B)		T6	162 (J1 C)
D7	55 (J1 A)									

3.7.5 Samtec Connector

M100PF uses two Samtec QSH-090-01-F-D-A connectors to supply its signals to a baseboard.



Below are tables with the pins of the connectors and their corresponding function.

3.7.6 Connector J1

Connector J1 A							
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	3.3V	2	JTAG_TRSTN	31	SD_CMD	32	GPIO_D3
3	3.3V	4	JTAG_TDO	33	SD_CLK	34	GPIO_E3
5	3.3V	6	JTAG_TCK	35	SD_DATA0	36	GPIO_B3
7	3.3V	8	JTAG_TDI	37	SD_DATA1	38	GPIO_B2
9	3.3V	10	JTAG_TMS	39	SD_DETECT	40	GPIO_E5
11	3.3V	12	JTAG_VIO	41	GPIO_A12	42	GPIO_F5
13	--	14	--	43	--	44	--
15	GPIO_A13	16	--	45	GPIO_E8	46	GPIO_C4
17	GPIO_B17	18	--	47	GPIO_B5	48	GPIO_D4
19	--	20	--	49	GPIO_C5	50	GPIO_E4
21	--	22	--	51	GPIO_C6	52	GPIO_F3
23	--	24	--	53	GPIO_C7	54	GPIO_A5
25	3.3V	26	--	55	GPIO_D7	56	GPIO_B4
27	SD_DATA2	28	GPIO_C2	57	--	58	GPIO_D6
29	SD_DATA3	30	GPIO_A3	59	--	60	GPIO_E6
181	Ground Plate	182	Ground Plate	183	Ground Plate	184	Ground Plate

Connector J1 B							
Pin	Function	Pin	Function	Pin	Function	Pin	Function
61	--	62	--	91	--	92	--
63	--	64	GPIO_G2	93	--	94	--
65	--	66	GPIO_H2	95	--	96	--
67	--	68	GPIO_J2	97	--	98	--
69	--	70	GPIO_L2	99	--	100	--
71	--	72	GPIO_M2	101	--	102	--
73	--	74	GPIO_H1	103	--	104	--
75	UART1_TX	76	GPIO_J1	105	--	106	--
77	UART1_RX	78	GPIO_K1	107	--	108	--
79	--	80	--	109	--	110	ETH1_RXC
81	--	82	--	111	--	112	GPIO_F1
83	--	84	--	113	GPIO_T5	114	--
85	--	86	--	115	GPIO_R3	116	--
87	--	88	--	117	--	118	GPIO_T1
89	--	90	--	119	--	120	GPIO_R1
185	Ground Plate	186	Ground Plate	187	Ground Plate	188	Ground Plate

Connector J1 C							
Pin	Function	Pin	Function	Pin	Function	Pin	Function
121	--	122	--	151	--	152	--
123	--	124	--	153	--	154	--
125	--	126	--	155	--	156	--
127	--	128	--	157	--	158	--
129	--	130	--	159	ETH1_GTXCLK	160	GPIO_F2
131	GPIO_P1	132	--	161	ETH1_MDC	162	GPIO_T6
133	GPIO_N1	134	--	163	ETH1_TXD1	164	ETH1_MDIO
135	--	136	--	165	ETH1_RX_DV	166	ETH1_TXD3
137	--	138	--	167	GPIO_L1	168	ETH1_RXD2
139	--	140	--	169	ETH1_RXD0	170	ETH1_RXD1
141	--	142	--	171	ETH1_TXD2	172	ETH1_TX_EN
143	--	144	--	173	ETH1_RXD3	174	ETH1_TXD0
145	--	146	--	175	--	176	--
147	--	148	--	177	3.3V	178	3.3V
149	--	150	--	179	3.3V	180	3.3V
189	Ground Plate	190	Ground Plate	191	Ground Plate	192	Ground Plate

3.7.7 Connector J2

Connector J2 A							
Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	GND	2	GND	31	GND	32	GND
3	XCVR0_REF_CLK_P	4	XCVR1_REF_CLK_P	33	RX2_P	34	RX6_P
5	XCVR0_REF_CLK_N	6	XCVR1_REF_CLK_N	35	RX2_N	36	RX6_N
7	GND	8	GND	37	GND	38	GND
9	RX0_P	10	RX4_P	39	TX2_P	40	TX6_P
11	RX0_N	12	RX4_N	41	TX2_N	42	TX6_N
13	GND	14	GND	43	GND	44	GND
15	TX0_P	16	TX4_P	45	RX3_P	46	RX7_P
17	TX0_N	18	TX4_N	47	RX3_N	48	RX7_N
19	GND	20	GND	49	GND	50	GND
21	RX1_P	22	RX5_P	51	TX3_P	52	TX7_P
23	RX1_N	24	RX5_N	53	TX3_N	54	TX7_N
25	GND	26	GND	55	GND	56	GND
27	TX1_P	28	TX5_P	57	--	58	--
29	TX1_N	30	TX5_N	59	--	60	--
181	Ground Plate	181	Ground Plate	181	Ground Plate	181	Ground Plate

Connector J2 B							
Pin	Function	Pin	Function	Pin	Function	Pin	Function
61	3.3V	62	3.3V	91	BOOT_MODE	92	GPIO_D14
63	--	64	--	93	GPIO_K4	94	GPIO_L6
65	--	66	--	95	--	96	GPIO_C15
67	--	68	--	97	GPIO_K5	98	--
69	--	70	GPIO_E11	99	--	100	--
71	GPIO_F11	72	--	101	--	102	--
73	--	74	--	103	3.3V	104	3.3V
75	3.3V	76	3.3V	105	ETH0_TXD3	106	ETH0_TXD0
77	--	78	--	107	ETH0_TXD1	108	ETH0_TXD2
79	GPIO_E14	80	GPIO_L7	109	ETH0_RXD3	110	ETH0_RXD0
81	--	82	--	111	ETH0_RXD2	112	ETH0_MDC
83	--	84	--	113	ETH0_GTXCLK	114	ETH0_TX_EN
85	--	86	--	115	ETH0_MDIO	116	ETH0_RXD1
87	--	88	--	117	ETH0_RX_DV	118	ETH0_RXC
89	GPIO_C14	90	GPIO_M7	119	3.3V	120	3.3V
185	Ground Plate	186	Ground Plate	187	Ground Plate	188	Ground Plate

Connector J2 C							
Pin	Function	Pin	Function	Pin	Function	Pin	Function
121	GPIO_N7	122	GPIO_M4	151	--	152	GPIO_G12
123	GPIO_N5	124	--	153	GPIO_D12	154	GPIO_G13
125	GPIO_L3	126	I2C0_SDA	155	GPIO_F10	156	GPIO_L8
127	GPIO_N6	128	GPIO_M9	157	3.3V	158	3.3V
129	CAN0_TX	130	CAN1_RX	159	POR_N	160	OCLK_P
131	GPIO_F13	132	UART0_TX	161	VBAT	162	OCLK_N
133	GPIO_M5	134	GPIO_M3	163	3.3V	164	--
135	CAN1_TX	136	GPIO_M8	165	PIC_SDA	166	--
137	CAN0_RX	138	UART0_RX	167	PIC_SCL	168	--
139	I2C0_SCL	140	3.3V	169	PMIC_TP	170	--
141	3.3V	142	3.3V	171	TP6	172	GPIO_L5
143	GPIO_E13	144	GPIO_J3	173	TP7	174	CLK25_3
145	GPIO_D13	146	GPIO_E10	175	3.3V	176	3.3V
147	GPIO_F12	148	--	177	3.3V	178	3.3V
149	GPIO_D11	150	GPIO_K3	179	3.3V	180	3.3V
189	Ground Plate	190	Ground Plate	191	Ground Plate	192	Ground Plate

3.8 Schematics

Schematics for the M100PF may be obtained on request.