MAX22203

65V, 3.8A Dual Brushed or Single Stepper Motor Driver with Integrated Current-Sense

General Description

The MAX22203 is a dual 65V, $3.8A_{MAX}$ H-Bridge with PWM inputs and accurate Current Drive Regulation (CDR). Each H-Bridge can be controlled individually and has a very low typical R_{ON} (high-side + low-side) of 0.3Ω, resulting in high driving efficiency and low heat generation. The MAX22203 can be used to drive two Brushed DC motors or a single Stepper motor.

The integrated CDR can limit the start up or stall the current of a Brushed DC motor or control the phase current for stepper operation.

The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS), eliminating the bulky external power resistors (normally required for this function) and compared with a configurable threshold current (I_{TRIP}). The I_{TRIP} threshold can be set independently for the two full bridges by connecting the external resistors to pins REFA and REFB.

The maximum output current per H-Bridge is I_{MAX} = 3.8A and is limited by the Overcurrent Protection (OCP) circuit. This current can be driven for very short transients and is aimed to effectively drive small capacitive loads. The maximum user-configurable current regulation threshold is I_{TRIP_MAX} = 3A. The maximum RMS current (I_{RMS}) per H-Bridge is $2A_{RMS}$ on a standard JEDEC 4-layer board. The maximum RMS current can be limited by thermal considerations and depends on the thermal characteristic of the application (PCB ground planes, heat sinks, forced air ventilation, etc).

The MAX22203 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected. During Thermal Shutdown and Undervoltage Lockout, the driver is tristated until normal operating conditions are restored.

The MAX22203 is packaged into a small TQFN38 5mm x 7mm and TSSOP38 9.7mm x 4.4mm packages.

Applications

- Brushed DC Motor Driver
- Stepper Motor Driver
- Solenoid Driver
- Latched Valves

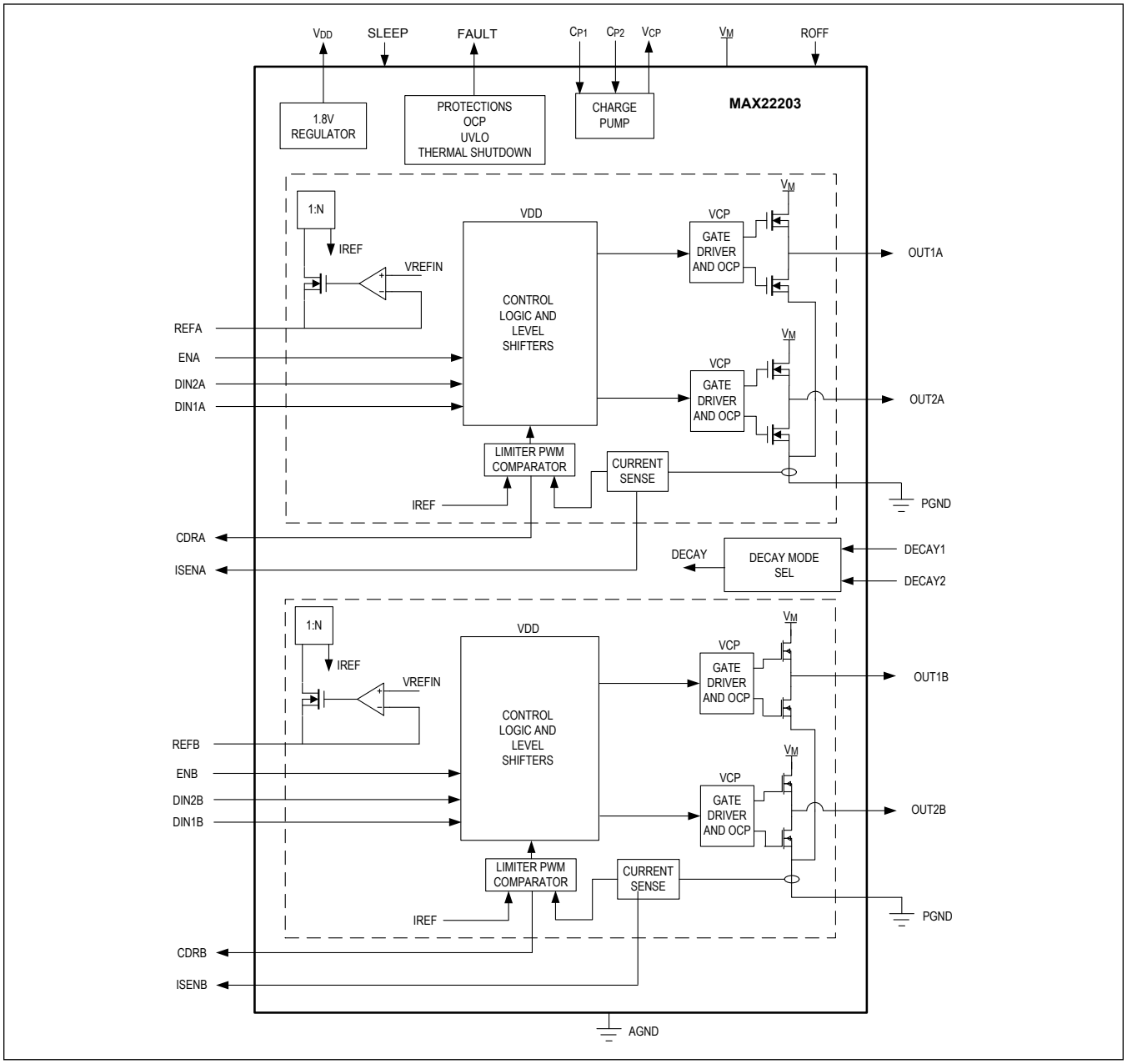
Benefits and Features

- Two H-Bridges with 65V Maximum Operating Voltage
  - Total R_{ON} (High-Side + Low-Side): 300mΩ typical (T_A = 25°C)
- Current Ratings Per H-Bridge (Typical at 25°C):
  - I_{MAX} = 3.8A (Impulsive Current for Driving Capacitive Loads)
  - I_{TRIP_MAX} = 3A (Maximum Current Setting for Internal Current Drive Regulation)
  - $I_{RMS} = 2A_{RMS}$
- Integrated Current Drive Regulation (CDR)
  - Internal Current Sensing (ICS) Eliminates External Bulky Resistors and Improves Efficiency
  - Current Drive Regulation Monitor Output Pins (CDRA and CDRB)
  - Multiple Decay Modes (Slow, Mixed, Fast)
  - Fixed Off Time Configurable with External Resistance.
- Current-Sense Output (Current Monitor)
- Fault Indicator Pin ($\overline{FAULT}$)
- Protections
  - Overcurrent Protection for Each Individual Channel (OCP)
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown (TSD) T_J = +165°C
- Available in TQFN38 5mm x 7mm and TSSOP38 9.7mm x 4.4mm Packages

***Ordering Information* appears at end of data sheet.**

19-101012; Rev 1; 5/24

Simplified Block Diagram



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Absolute Maximum Ratings

V_M to GND ..... -0.3V to +70V
V_{DD} to GND..... -0.3V to min (+2.2V, V_M + 0.3V)
PGND to GND ..... -0.3V to +0.3V
OUT_ ..... -0.3 to (V_M + 0.3V)
V_{CP} to GND..... (V_M - 0.3V) to min (+74V, V_M + 6V)
C_{P2} to GND ..... (V_M - 0.3V) to (V_{CP} + 0.3V)
C_{P1} to GND ..... -0.3V to (V_M + 0.3V)
FAULT to GND ..... -0.3V to 6V
CDR_ to GND..... -0.3V to 6V
REF_ to GND ..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ROFF to GND ..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
ISEN_ to GND..... -0.3V to min (+2.2V, V_{DD} + 0.3V)
DIN_ to GND..... -0.3V to 6V
EN_ to GND ..... -0.3V to 6V
DECAY_ to GND..... -0.3V to 6V
SLEEP to GND ..... -0.3V to min (+70V, V_M + 0.3V)
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

38-Pin TSSOP (9.7mm x 4.4mm)

Package Code	U38E+3C
Outline Number	21-0714
Land Pattern Number	90-0435
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	45ºC/W
Junction to Case (θ_{JC})	1ºC/W

38-Pin TQFN (5mm x 7mm)

Package Code	T3857-1C
Outline Number	21-0172
Land Pattern Number	90-0076
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	38ºC/W
Junction to Case (θ_{JC})	1ºC/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28ºC/W
Junction to Case (θ_{JC})	1ºC/W

For the latest package outline information and land patterns (footprints), go to *Package Index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.

Electrical Characteristics

(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ, $R_{REF\_}$ = from 12kΩ to 72kΩ, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization, typical values are at V_M = 36V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_M		4.5		65	V
Sleep-Mode Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic low			20	µA
Quiescent Current Consumption	I_{VM}	$\overline{SLEEP}$ = logic high			5	mA
1.8V Regulator Output Voltage	V_{VDD}	V_M = +4.5V, I_{LOAD} = 20mA		1.8		V
V_{DD} Current Limit	$I_{VDD(LIM)}$	V_{DD} shorted to GND	18			mA
Charge-Pump Voltage	V_{CP}			V_M + 2.7		V
LOGIC LEVEL INPUTS/OUTPUTS						
Input Voltage Level—High	V_{IH}		1.2			V
Input Voltage Level—Low	V_{IL}				0.65	V
Input Hysteresis	V_{HYS}			110		mV
Pull-Down Current	I_{PD}	Logic supply (V_L) = +3.3V	16	34	60	µA
Open-Drain Output Logic-Low Voltage	V_{OL}	I_{LOAD} = 5mA			0.4	V
Open-Drain Output Logic-High Leakage Current	I_{OH}	V_{PIN} = +3.3V	-1		+1	µA
$\overline{SLEEP}$ Voltage Level High	$V_{IH(\overline{SLEEP})}$		0.9			V
$\overline{SLEEP}$ Voltage Level Low	$V_{IL(\overline{SLEEP})}$				0.6	V
$\overline{SLEEP}$ Pull-Down Input Resistance	$R_{PD(\overline{SLEEP})}$		0.8	1.5		MΩ
OUTPUT SPECIFICATIONS						
Output On-Resistance Low-Side	$R_{ON(LS)}$			150	270	mΩ
Output On-Resistance High-Side	$R_{ON(HS)}$			150	300	mΩ
Output Leakage	I_{LEAK}	Driver off	-12		+12	µA
Dead Time	t_{DEAD}			100		ns
Output Slew Rate	SR			300		V/µs
PROTECTION CIRCUITS						
Overcurrent Protection Threshold	I_{OCP}		3.8			A
Overcurrent Protection Blanking Time	t_{OCP}			2.2	3.5	µs
Autoretry OCP Time	t_{RETRY}			3		ms
UVLO Threshold on V_M	V_{UVLO}	V_M rising	3.75	4	4.25	V

Electrical Characteristics (continued)

(V_M = from +4.5V to +65V, R_{ROFF} = from 15kΩ to 120kΩ, $R_{REF\_}$ = from 12kΩ to 72kΩ, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization, typical values are at V_M = 36V and T_A = +25°C.)

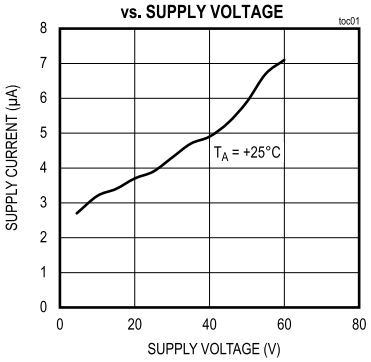
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Threshold on V_M Hysteresis	$V_{UVLOHYS}$			0.12		V
Thermal-Protection Threshold Temperature	T_{SD}	Temperature rising until $\overline{FAULT}$ pin goes low		+155		°C
Thermal-Protection Temperature Hysteresis	T_{SD_HYST}	Temperature falling until $\overline{FAULT}$ pin goes high		20		°C
CURRENT REGULATION						
REF_ Pin Resistor Range	R_{REF}		12		72	KΩ
REF Output Voltage	V_{REF}			900		mV
I_{TRIP}	KI			36		KV
Current Trip Regulation Accuracy (*Note 1*)	DITRIP1	I_{TRIP} from 1.75A to 3A	-5		5	%
	DITRIP2	I_{TRIP} from 500mA to 1.75A	-10		+10	
Fixed OFF – Time Internal	t_{OFF}	ROFF shorted to V_{DD}	16	20	24	µs
Fixed OFF – Time Constant	KTOFF	R_{ROFF} from 15KΩ to 120KΩ		0.667		µs/kΩ
PWM Blanking time	t_{BLK}			2.5		µs
CURRENT-SENSE MONITOR						
ISEN_ Voltage Range	V_{ISEN}	Voltage range at ISEN_ pin	0		1.1	V
Current-Monitor Scaling Factor	KISEN	Set the I_{ISEN} output-current equation in the *Current-Sense Output (CSO)—Current Monitor* section		7500		A/A
Current Monitor Accuracy (*Note 1*)	DKISEN1	I_{OUT} from 1.1A to 3A	-5		+5	%
	DKISEN2	I_{OUT} from 500mA to 1.1A	-10		+10	
Current Monitor Accuracy	DKISEN3	I_{OUT} from 250mA to 500mA	-15		+15	%
Settling Time	t_S	$I_{FS} = I_{MAX}$		0.5		µs
FUNCTIONAL TIMING						
Sleep Time	t_{SLEEP}	$\overline{SLEEP}$ = logic 1 to logic 0 for OUT_ to become three-state		40		µs
Wake-Up Time from Sleep	t_{WAKE}	$\overline{SLEEP}$ = logic 0 to logic 1 to resume normal operation			2.7	ms
Enable Time	t_{EN}	Time from EN_ pin rising edge to driver on			0.6	µs
Disable Time	t_{DIS}	Time from EN_ pin falling edge to driver off			1.4	µs

Note 1: Guaranteed by design, not production tested.

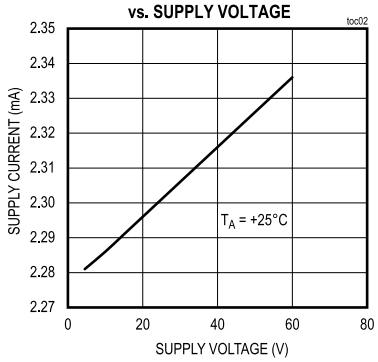
Typical Operating Characteristics

(V_M = +4.5V to +60V; T_A = +25°C, unless otherwise noted.)

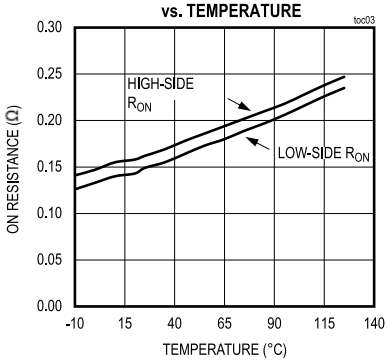
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



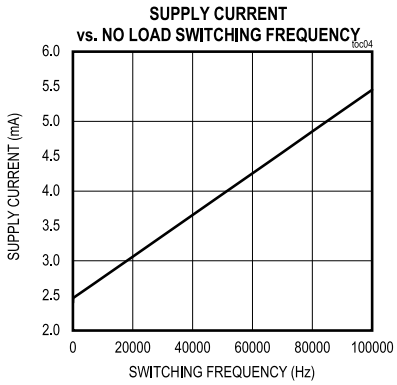
QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



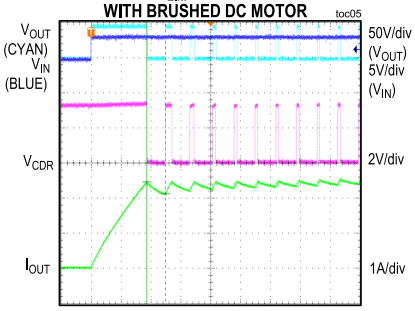
ON RESISTANCE vs. TEMPERATURE



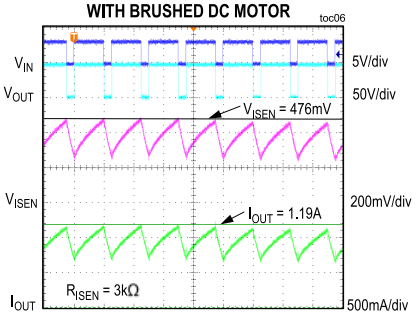
SUPPLY CURRENT vs. NO LOAD SWITCHING FREQUENCY



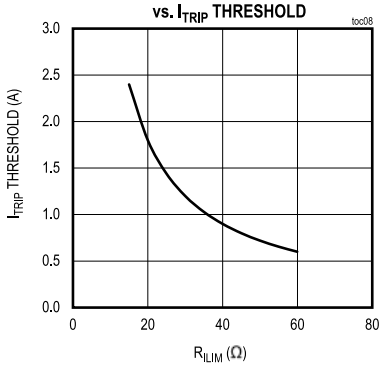
INRUSH CURRENT LIMIT (ZOOMED) 2.4A I_{LIM} THRESHOLD WITH BRUSHED DC MOTOR



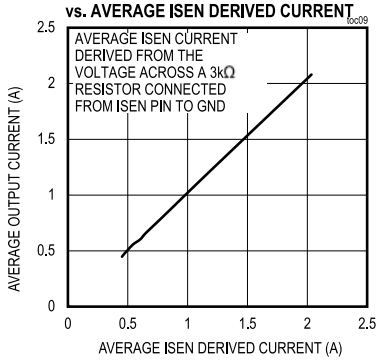
LOAD CURRENT AND ISEN VOLTAGE AT 20kHz PWM AND SLOW DECAY WITH BRUSHED DC MOTOR



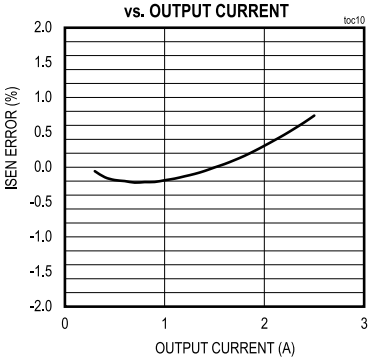
R_{ILIM} RESISTANCE vs. I_{TRIP} THRESHOLD



AVERAGE OUTPUT CURRENT vs. AVERAGE ISEN DERIVED CURRENT

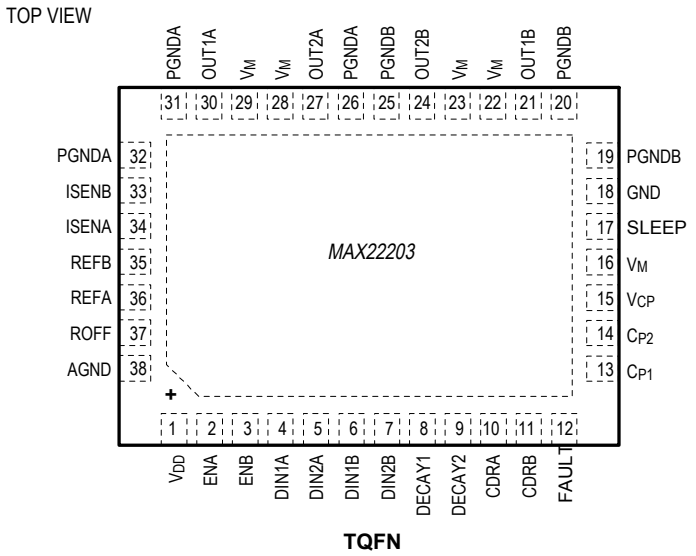


ISEN ERROR vs. OUTPUT CURRENT



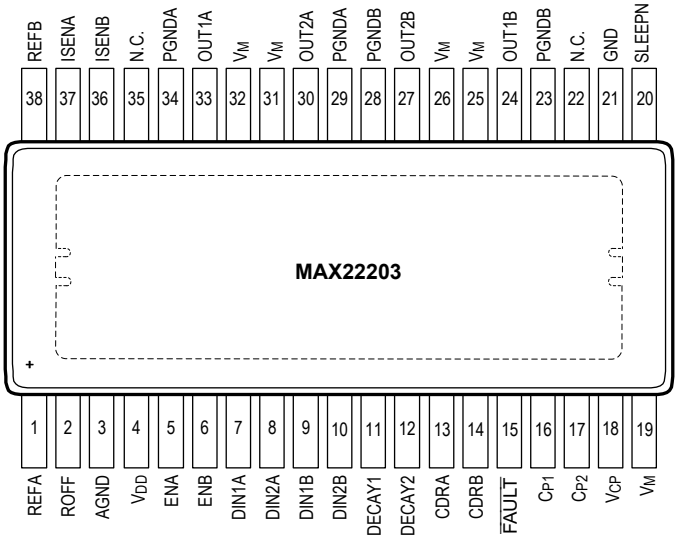
Pin Configurations

TQFN Pin Configuration



TQFN

TSSOP Pin Configuration



TSSOP38

Pin Description

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
16, 22, 23, 28, 29	19, 25, 26, 31, 32	V_M	Supply Voltage Input. Connect at least 1µF surface-mounted device plus 10µF electrolytic bypass capacitors to GND. Higher values can be considered depending on application requirements.	Supply
15	18	V_{CP}	Charge-Pump Output. Connect a 5V, 1µF capacitor between V_{CP} and V_M as close as possible to the device.	Output
13	16	C_{P1}	Charge-Pump Flying Capacitor Pin 1. Connect a V_M-rated 22nF capacitor between C_{P1} and C_{P2} as close as possible to the device.	Output
14	17	C_{P2}	Charge-Pump Flying Capacitor Pin 2. Connect a V_M-rated 22nF capacitor between C_{P1} and C_{P2} as close as possible to the device.	Output
1	4	V_{DD}	1.8V Linear Regulator Output. Bypass V_{DD} to GND with a 5V, 2.2µF capacitor connected close to the device.	Analog Output
17	20	$\overline{SLEEP}$	Active-Low Sleep Pin.	Logic Input
21, 24, 27, 30	24, 27, 30, 33	OUT1B, OUT2B, OUT2A, OUT1A, respectively	Driver outputs.	Output
12	15	$\overline{FAULT}$	Active-Low, Open-Drain, Output Fault Indicator. $\overline{FAULT}$ goes low to indicate that one or more of the protection mechanisms has been activated. Connect a 2kΩ pull-up resistor from $\overline{FAULT}$ to the microcontroller supply voltage.	Open-Drain Output

Pin Description (continued)

PIN		NAME	FUNCTION	TYPE
TQFN	TSSOP			
33, 34	36, 37	ISEN_	Current-Sense Output Monitor. Connect a resistor to GND (see the Current-Sense Output (CSO)—Current Monitor section).	Output
2, 3	5, 6	EN_	Logic Input Pin. Enable Pin.	Logic Input
4, 5, 6, 7	7, 8, 9, 10	DIN_	CMOS PWM Input.	Logic Input
8, 9	11, 12	DECAY_	Logic Input. Set the Decay Mode.	Logic Input
10, 11	13, 14	CDR_	Open-Drain Output - Current Drive Regulator. Add a pullup resistor to the controller supply voltage. The pullup resistor value depends on the application requirements. Values between 1KΩ to 5KΩ meet the requirements for most applications.	Open Drain Output
36	1	REFA	Programmable Current Analog Input. Connect a resistor from R_{EFA} to GND to set the current regulation threshold for Full Bridge A.	Analog Input
35	38	REFB	Programmable Current Analog Input. Connect a resistor from REFB to GND to set the current regulation threshold for Full Bridge B.	Analog Input
37	2	ROFF	t_{OFF} Programmable Off Time Pin. Connect ROFF to V_{DD} to use the internal fixed t_{OFF} time. Connect a resistor R_{ROFF} from ROFF to GND to set the fixed OFF time to a desired value.	Analog Input
18, 38	3, 21	GND	Analog Ground. Connect to ground plane.	GND
19, 20, 25, 26, 31, 32	23, 28, 29, 34	PGND	Power GND. Connect to ground plane.	GND
EP	EP	EP	Exposed Pad. Connect to GND.	GND

Detailed Description

The MAX22203 is a Dual 65V, $3.8A_{MAX}$ H-Bridge. It can be used to drive two Brushed DC motors or a Single Stepper Motor. The H-Bridge FETs have very low impedance, resulting in high driving efficiency and low heat. The typical total R_{ON} (high-side + low-side) is 0.3Ω. Each H-Bridge can be individually PWM controlled with three logic inputs (DIN1, DIN2, and EN).

The MAX22203 features an accurate Current Drive Regulation (CDR), which can be used to limit the start-up current of a Brushed DC motor or to control the phase current for stepper operation. The bridge output current is sensed by a non-dissipative Integrated Current Sensing (ICS) and it is then compared with the desired threshold current. As soon as the bridge current exceeds the threshold I_{TRIP}, the device enforces the decay for a fixed OFF time (t_{OFF}).

The non-dissipative ICS eliminates the bulky external power resistors, which are normally required for this function, resulting in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

A current proportional to the internally sensed motor current is output to an external pin (ISEN). By connecting an external resistor to this pin, a voltage proportional to the motor current is generated. The voltage built-up on such external resistor can be input into the controller ADC whenever the motor control algorithm requires the current/torque information.

Also, two open-drain output pins (CDRA, CDRB) are asserted every time the internal current regulation takes control of the driver. This allows the external controller to monitor the activity of the internal current loop.

The maximum output current per H-Bridge is $I_{MAX} = 3.8A_{MAX}$ and is limited by the Overcurrent Protection (OCP) circuit. This current can be driven for very short transients and is aimed to effectively drive small capacitive loads.

The maximum user-configurable current regulation threshold is I_{TRIP_MAX} = 3A. Current thresholds can be set independently for the two full bridges by connecting the external resistors to pins REFA and REFB.

The maximum RMS current per H-Bridge is $I_{RMS} = 2A_{RMS}$ on a standard JEDEC 4-layer board. Since this current is limited by thermal considerations, the actual maximum RMS current depends on the thermal characteristic of the application (PCB ground planes, heatsinks, forced air ventilation, etc).

The MAX22203 features Overcurrent Protection (OCP), Thermal Shutdown (TSD), and Undervoltage Lockout (UVLO). An open-drain active low $\overline{FAULT}$ pin is activated every time a fault condition is detected.

During Thermal Shutdown and Undervoltage Lockout, the driver is tristated until normal operating conditions are restored.

Sleep Mode ($\overline{SLEEP}$ Pin)

The $\overline{SLEEP}$ pin can be driven low to place the device into the lowest power consumption mode possible, with all outputs three-stated, the internal circuits biased off, and the charge pump disabled. A pull-down resistor should be connected between $\overline{SLEEP}$ and GND to ensure the part is disabled whenever this pin is not actively driven. Driving the $\overline{SLEEP}$ pin high wakes up the device and returns it to normal mode. t_{WAKE} is 2.7ms (max).

PWM Control

When an H-Bridge is Enabled (EN_ = Logic High) and the H-Bridge current is below the configured current limit, the average output voltage can be controlled by DIN1_ and DIN2_ logic input pins using PWM techniques. Setting Enable logic low causes the output to enter a high impedance mode and the motor to coast. The Enable input pin frequency must not exceed 1KHz and cannot be used for PWM control.

Table 1 shows the control Truth Table.

Table 1. MAX22203 Truth Table

EN_	DIN1_	DIN2_	OUT1_	OUT2_	DESCRIPTION
0	X	X	High-Z	High-Z	H-Bridge Disabled. High Impedance (HiZ)
1	0	0	L	L	Brake Low; Slow Decay
1	1	0	H	L	Current from OUT2 to OUT1
1	0	1	L	H	Current from OUT1 to OUT2
1	1	1	H	H	Brake High; Slow Decay

PWM techniques can be used to control the output duty cycle and hence to implement motor speed control. Typically, for brushed DC motor drivers, Slow Decay is preferred as it results in less ripple and higher efficiency. With this approach, during the OFF phase, both the low side FETs are activated effectively grounding the motor winding terminals. The current built-up into the motor winding slowly decays. This decay is often referred to as Slow Decay. Alternatively, Fast Decay can also be implemented by reversing the bridge during the OFF phase.

Current-Sense Output (CSO)—Current Monitor

Currents proportional to the internally-sensed motor currents are output to pins ISENA and ISENB for H-bridge A and B, respectively. The current is sensed when one of the two low side FETs sinks the output current and it is therefore meaningful for both during the energizing (t_{ON}) phase and during the Slow Decay phase (Brake). In Fast Decay, the current is not monitored and ISEN outputs a zero current. The following equation shows the relationship between the current sourced at ISEN and the output current.

$$I_{ISEN}(A) = \frac{I_{OUT}(A)}{K_{ISEN}}$$

Equation - ISEN Output Current

in which K_{ISEN} represents the current scaling factor between the output current and its replica at pin ISEN. K_{ISEN} is typically 7500 A/A. For instance, if the instantaneous output current is 2A, the current sourced at ISEN is 266µA.

Figure 1 shows an idealized behavior of the ISEN current when Slow or Fast Decay are used. Blanking times, delays, and rise/fall edges are ignored.

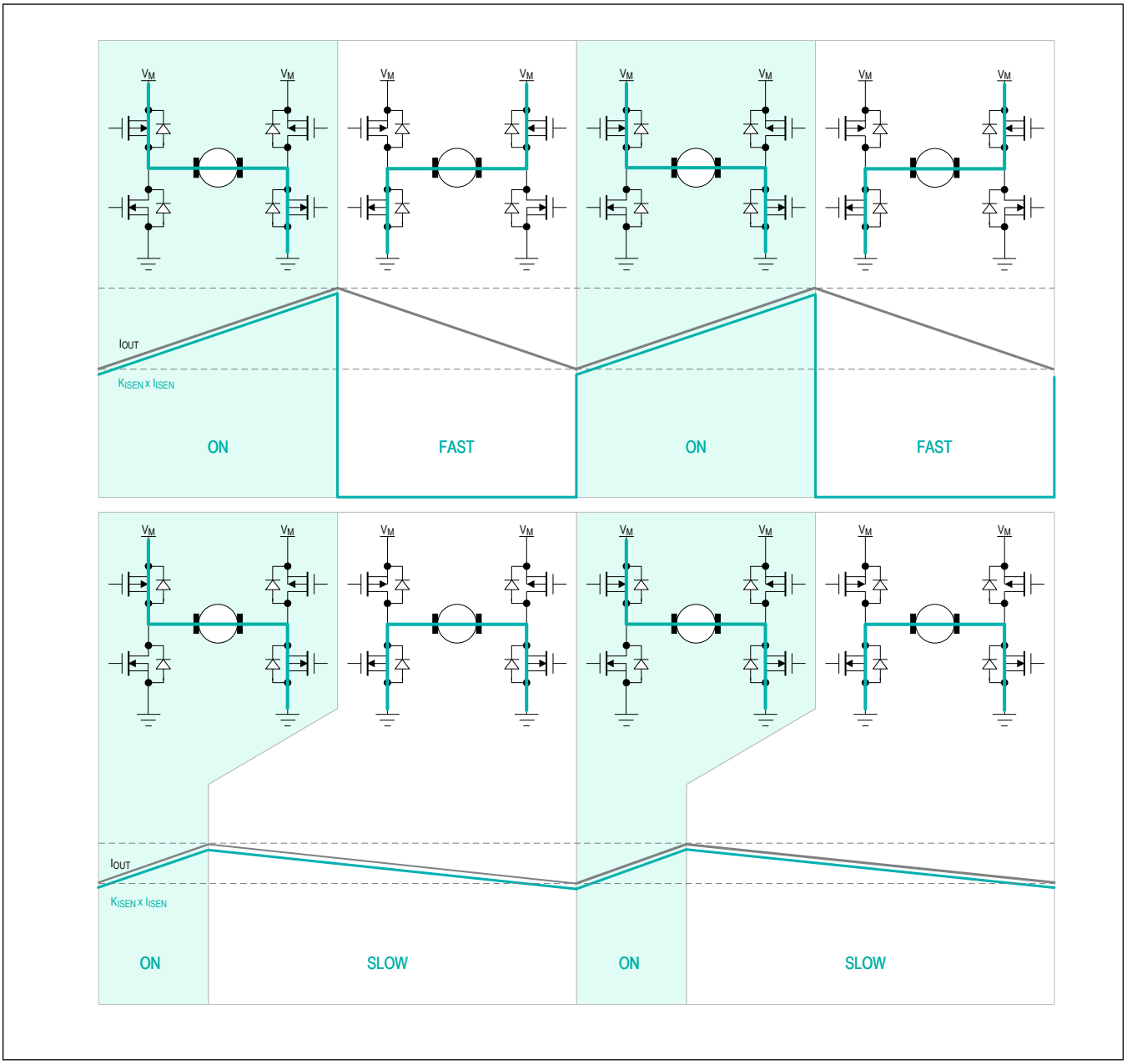


Figure 1. ISEN Current

By connecting an external signal resistor, R_{ISEN}, between ISEN and GND, a voltage proportional to the motor current is generated. The voltage built-up on R_{ISEN} can be input into the ADC of an external controller in applications in which the motor control algorithm requires the current/torque information. The following equation shows the design formula to calculate R_{ISEN} once the ADC full scale voltage (V_{FS}) and the maximum operating current (I_{MAX}) is known:

$$R_{ISEN}(\Omega) = K_{ISEN} \times \frac{V_{FS}(V)}{I_{MAX}(A)}$$

Equation - R_{ISEN} Setting

For example, if the ADC operates up to 1V FS and the maximum operating output current is 2A, then R_{ISEN} is 7500 x 1V/2A = 3.75KΩ.

The R_{ISEN} value also sets the output impedance of the Current-Sense Output circuit (ISEN output impedance). Normally, the input impedance of the ADC is much higher than R_{ISEN}, enabling a direct connection to the ISEN pin without attenuation. If a low input impedance ADC is used, a preamplifier (buffer) is required.

The Current-Sense Output circuit bandwidth and step response performances (see *Specifications*) ensure the current monitor tracks the driver current in motor drive applications.

Current Drive Regulation

The MAX22203 features embedded Current Drive Regulation (CDR).

The embedded current drive regulation provides an accurate control of the current flowing into the motor windings.

The bridge current is sensed by a non-dissipative Integrated Current Sensing (ICS) circuit and it is then compared with the threshold current (I_{TRIP}). As soon as the bridge current exceeds the threshold, the device enforces the decay for a fixed OFF-time (t_{OFF}). The device supports different decay modes as described in the following paragraphs.

Once t_{OFF} elapses, the driver is re-enabled for the next PWM cycle. During current regulation, the PWM duty cycle and frequency depend on the supply voltage, on the motor inductance, and on motor speed and load conditions.

The t_{OFF} duration can be configured with an external resistor connected to the ROFF pin.

Integrated Current-Sense (ICS)

A non-dissipative current sensing is integrated. This feature eliminates the bulky external power resistors normally required for this function. This feature results in a dramatic space and power saving compared with mainstream applications based on the external sense resistor.

Setting the Current Regulation Threshold – Pin REF

Connect resistors from REFA and REFB to GND to set the current regulation thresholds for Full Bridge A and Full Bridge B respectively (I_{TRIPA}, I_{TRIPB}) .

The equation below shows the typical I_{TRIP} current as a function of the $R_{REF\_}$ shunt resistor connected to pin REF_. The proportionality constant K_I is typically 36KV. The external resistor $R_{REF\_}$ can range between 12KΩ and 72KΩ, which correspondents to I_{TRIP} setting ranging from about 3A down to 0.5A.

$$I_{TRIP} = \frac{K_I(KV)}{R_{REF}(K\Omega)}$$

Setting the Fixed OFF_TIME (t_{OFF})

The current regulation circuit is based on a constant t_{OFF} PWM control. When the bridge current exceeds the target I_{TRIP} current, an OFF phase begins and Decay modes are activated. The OFF phase has a fixed time duration (t_{OFF}). t_{OFF} can be configured to a desired value by connecting an external resistor (R_{ROFF}) to pin ROFF. When the ROFF pin is shorted to V_{DD}, the t_{OFF} time is internally set at a fixed value (20µs typical).

By connecting an external resistor to the pin ROFF, configure t_{OFF} as shown in the following equation, in which R_{ROFF} is an external resistor connected to the ROFF pin (in KΩ) and KT_{OFF} is an internal constant equal to 0.667µs/KΩ.

$$t_{OFF}(\mu s) = R_{ROFF} \times K_{TOFF}$$

t_{OFF} can be programmed from a range of 10µs to 80µs.

CDR Open-Drain Output

The CDR_ pins are active-low open-drain outputs, which are asserted during the fixed t_{OFF} decay interval enforced by the integrated current drive regulation loop. An external controller monitoring the CDR_ pins can determine if the integrated current drive regulation loop has taken control of the driver overwriting the status of the PWM logic inputs (DIN1, DIN2).

The CDR_ signals can be used by an external controller for several reasons and provides information about the actual load during current regulation. For example, in the use case where the PWMs are permanently held in the Forward or Reverse mode, control of the motor current is entrusted to the internal Current Drive Regulation loop and the CDR_ pin status directly reflects the driver output status. In this example, the duty cycle of the CDR_ pin can be used to detect stall conditions.

A pullup resistor must be connected from the CDR_ pins to the controller voltage supply. The pullup resistor choice depends on the PCB line capacitance, PWM frequency, and power consumption. Values between 1KΩ to 5KΩ satisfy the requirement for most applications.

The time diagram in Figure 2 shows the behavior of this function when the motor spins in the forward direction respectively with DIN2 held firmly High (Case A) or when DIN2 is toggling (Case B and C).

The CDR output is asserted only when the slow decay mode is forced by the internal CDR.

Notice that any PWM transitions resets the fixed OFF Time of the CDR circuit. In Case B, the actual Slow Decay Interval is longer than t_{OFF}, whereas in Case C, the actual Slow Decay interval is shorter.

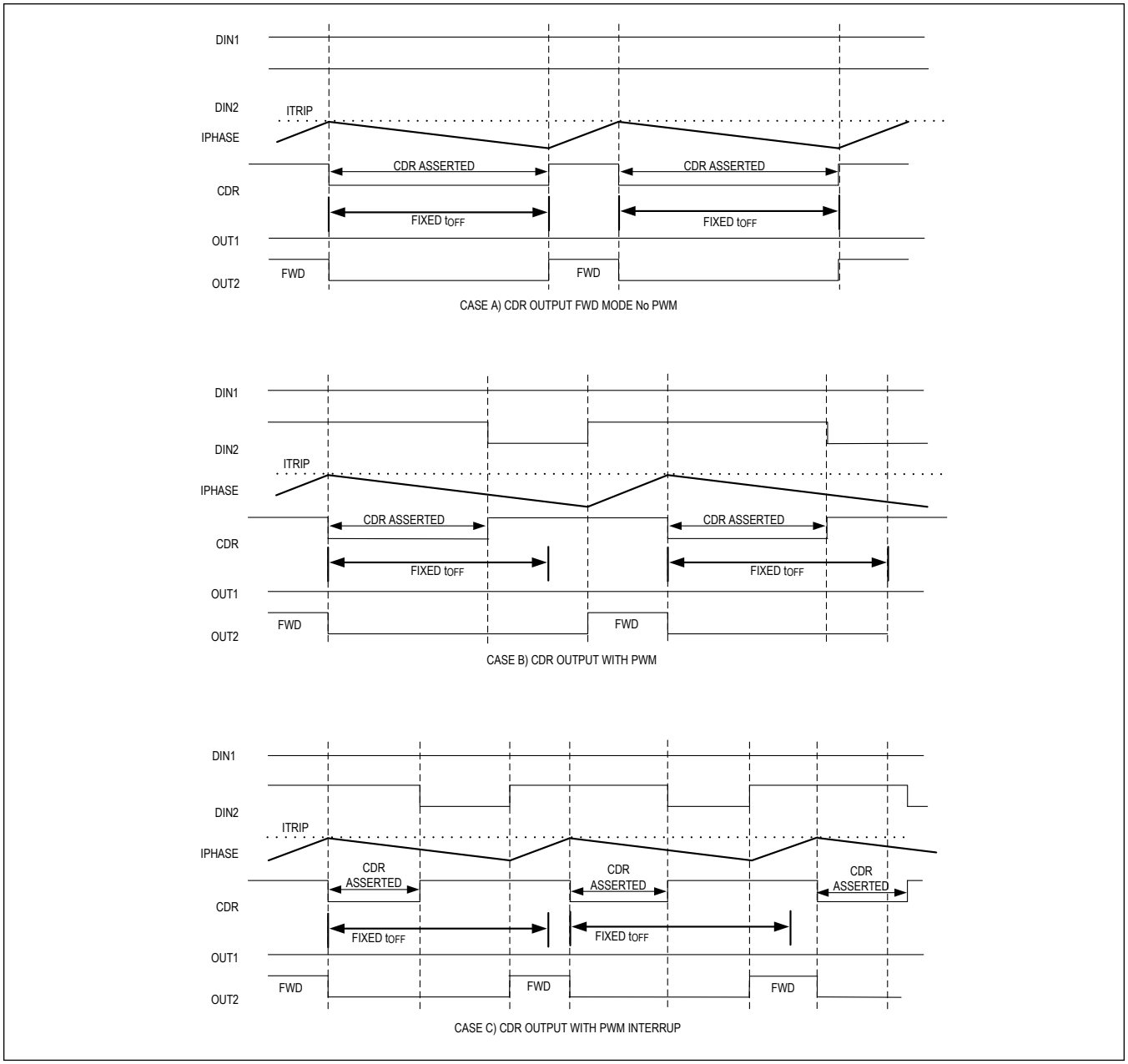


Figure 2. CDR Monitor Timing Diagram

Operating Modes

During PWM chopping, the driver output alternates the Energizing (ON) and Decay phases. The MAX22203 supports different Decay modes. Slow Decay, Fast Decay, and different combinations between Slow and Fast.

Figure 3 shows the current path in the three different modes of operation.

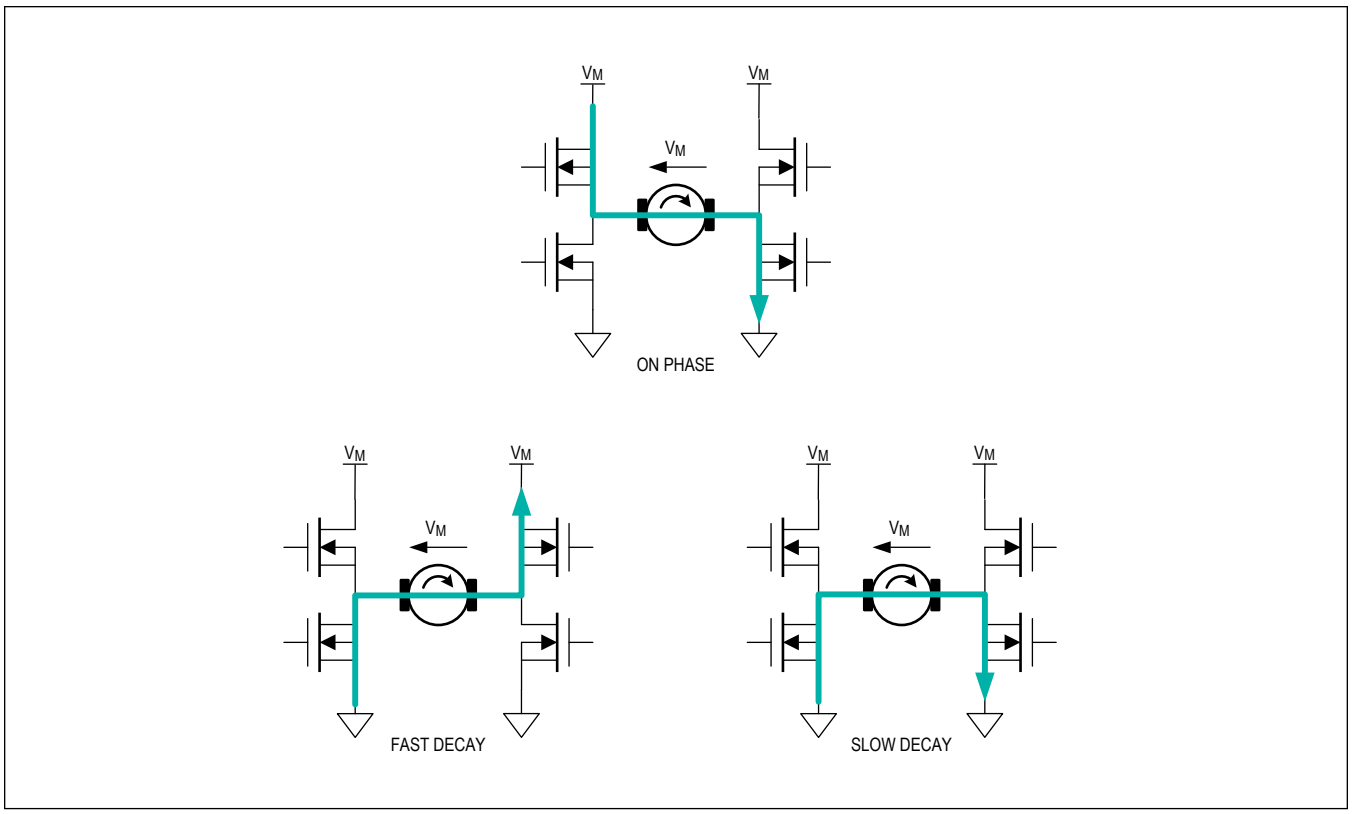


Figure 3. Current Flow During ON and Decay Modes

Setting the Decay Mode

Two logic input pins allow to set the Decay Mode during t_{OFF}. The MAX22203 supports Slow, Fast, and Mixed Decay modes.

Table 2 shows the Truth Table for the Decay selection.

Table 2. Decay Mode Truth Table

DECAY2	DECAY1	DECAY MODE
0	0	SLOW
0	1	MIXED 30% FAST*/70% SLOW
1	0	MIXED 60% FAST*/40% SLOW
1	1	FAST*

*To prevent reversal of current during fast decay, outputs go to the high-impedance state as the current approaches 0A.

Fault Protection

Overcurrent Protection (OCP)

An OCP protects the device against short circuits to the rails (supply voltage and ground) and across the load terminals. The OCP threshold is set at 3.8A minimum. If the output current is larger than the OCP threshold for longer than the OCP blanking time, an OCP event is detected. When an OCP event is detected, the H-Bridge is immediately disabled, and a fault indication is output on the pin $\overline{FAULT}$. The H-Bridge is kept in a high impedance mode for 3ms (see t_{RETRY} specification). The H-Bridge is then re-enabled according to the current state. If the short circuit is still present, this cycle repeats. Otherwise, normal operation resumes. Avoid prolonged operation under the short-circuit failure mode as a prolonged OCP auto-retry affects the device reliability.

Thermal Shutdown

If the die temperature exceeds T_{SD} = +155°C (typ), all output pins (OUT1A, OUT2A, OUT1B, and OUT2B) are three-stated and the $\overline{FAULT}$ pin is driven low. The $\overline{FAULT}$ pin remains low and the outputs are placed in three-state mode until the die temperature falls by the hysteresis amount of 20°C (typ), after which the $\overline{FAULT}$ pin is driven high and the outputs are re-enabled.

Undervoltage-Lockout Protection (UVLO)

When the V_M supply voltage is below the UVLO threshold, all OUT_ outputs are three-stated and the $\overline{FAULT}$ pin is driven low. The OUT_ outputs automatically return to their current state (defined by EN_ and DIN_) when the V_M supply voltage exceeds the UVLO threshold (max) and $\overline{FAULT}$ is driven high.

Applications Information

Recommended Layout

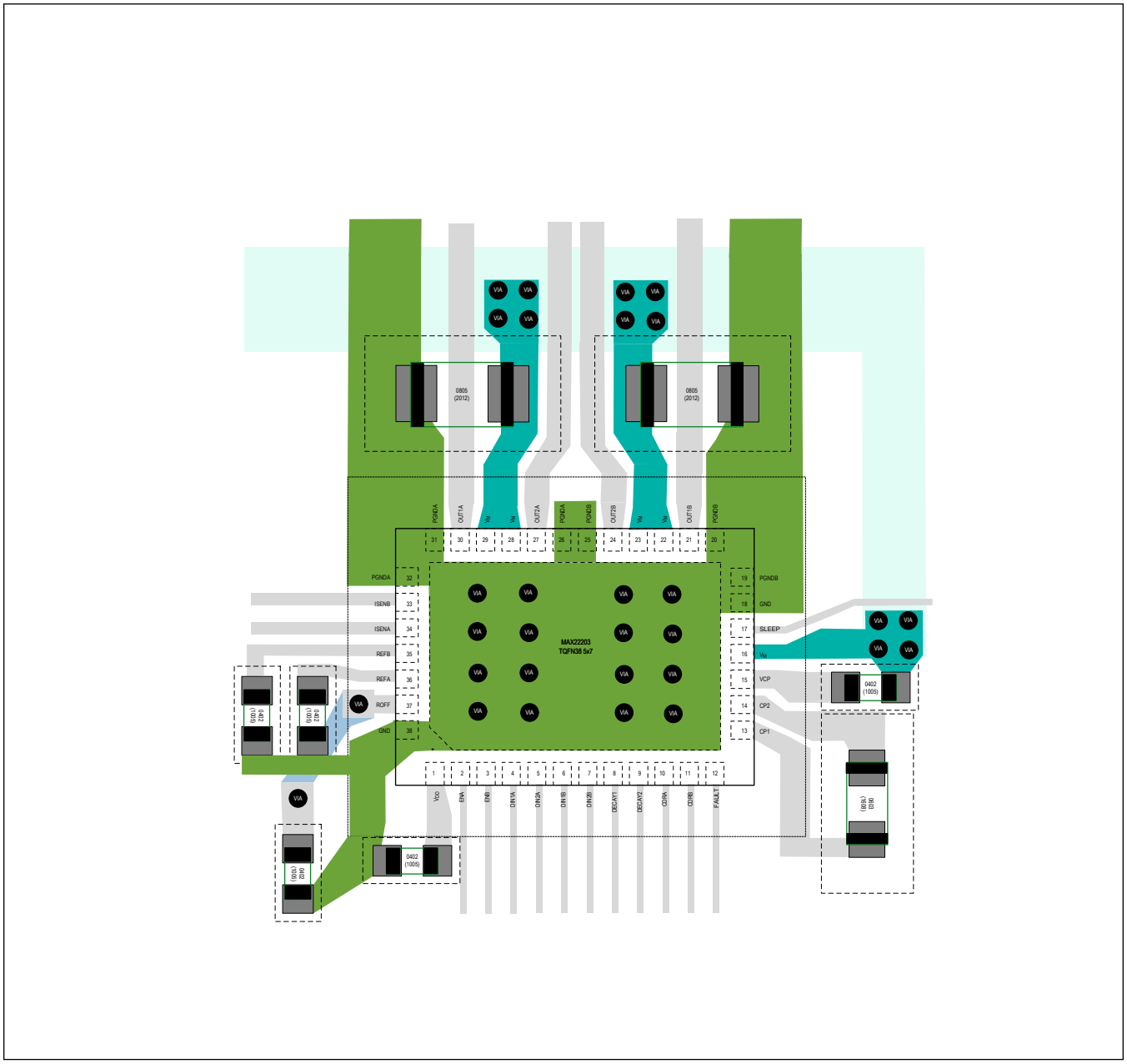
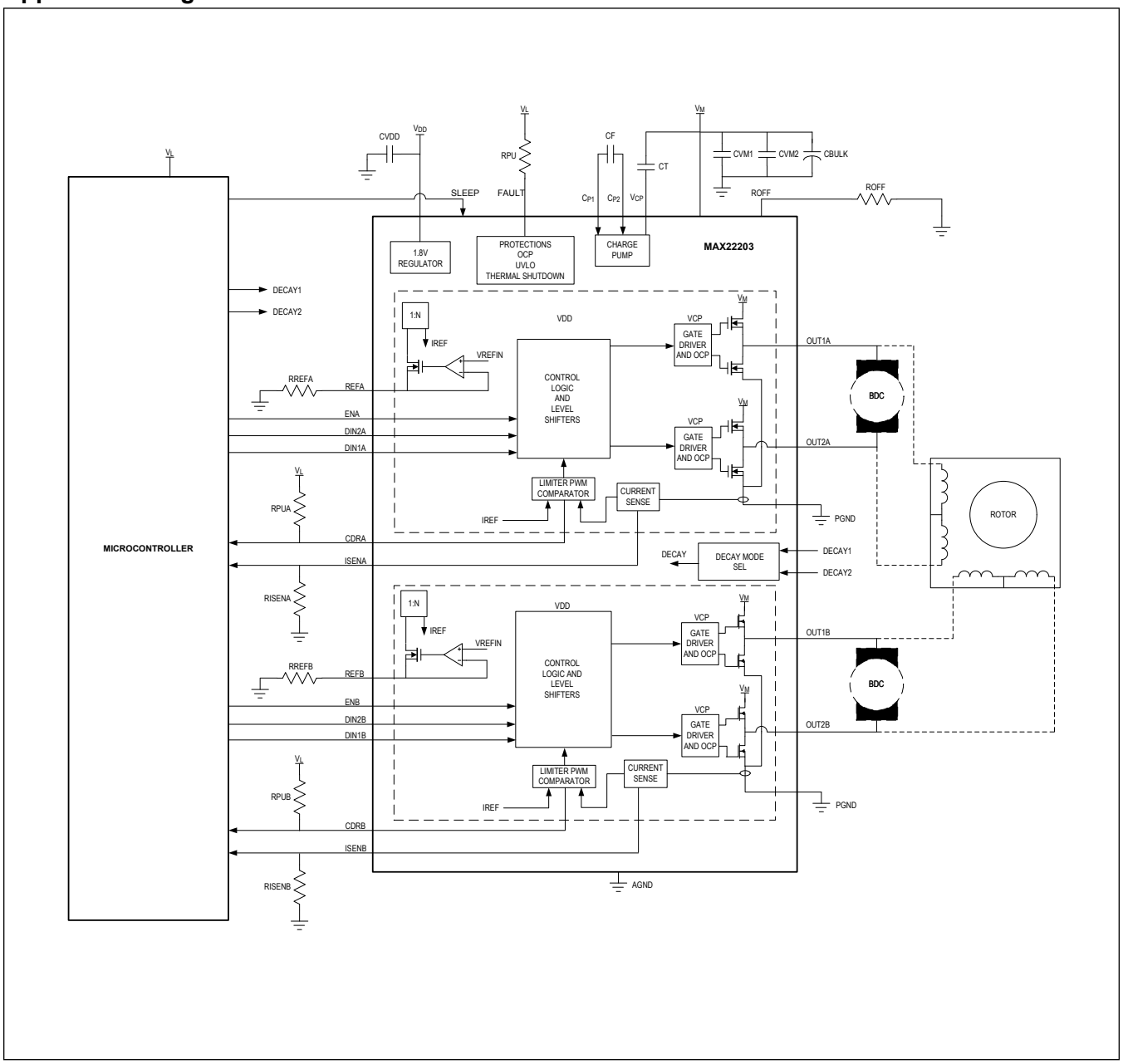


Figure 4. Recommended Layout

Typical Application Circuits

Application Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX22203ATU+	-40°C to +125°C	38-TQFN
MAX22203ATU+T	-40°C to +125°C	38-TQFN
MAX22203AUU+	-40°C to +125°C	38-TSSOP
MAX22203AUU+T	-40°C to +125°C	38-TSSOP

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/21	Initial release	—
1	5/24	Updated the *General Description*, *Benefits and Features*, *Absolute Maximum Ratings, Package Information*, *Electrical Characteristics*, *Typical Operating Characteristics*, *Pin Configurations*, *Pin Description*, *Detailed Description*, and *Ordering Information* sections	1, 6-13, 15-19, 22