Low−Voltage CMOS Octal D−Type Flip−Flop Flow Through Pinout

With 5 V−Tolerant Inputs and Outputs (3−State, Non−Inverting)

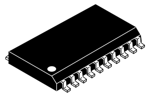
MC74LCX574

The MC74LCX574 is a high performance, non−inverting octal D−type flip−flop operating from a 1.65 to 5.5 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX574 inputs to be safely driven from 5.0 V devices.

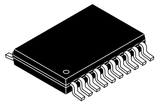
The MC74LCX574 consists of 8 edge−triggered flip−flops with individual D−type inputs and 3−state true outputs. The buffered clock and buffered Output Enable ($\overline{OE}$) are common to all flip−flops. The eight flip−flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW−to−HIGH Clock (CP) transition. With the $\overline{OE}$ LOW, the contents of the eight flip−flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. The $\overline{OE}$ input level does not affect the operation of the flip−flops. The LCX574 flow through design facilitates easy PC board layout.

Features

- Designed for 1.65 to 5.5 V V_{CC} Operation
- 5 V Tolerant − Interface Capability With 5 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When V_{CC} = 0 V
- LVTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability at 3 V
- Near Zero Static Supply Current in All Three Logic States (10 µA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 100 mA
- ESD Performance:
  - Human Body Model >2000 V
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

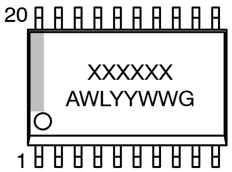


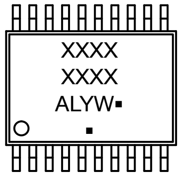
SOIC−20 WB
DW SUFFIX
CASE 751D−05



TSSOP−20
DT SUFFIX
CASE 948E

MARKING DIAGRAM





A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

January, 2025 − Rev. 12

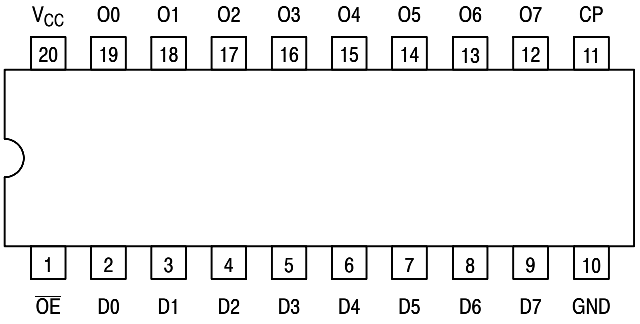


Figure 1. Pinout: 20–Lead (Top View)

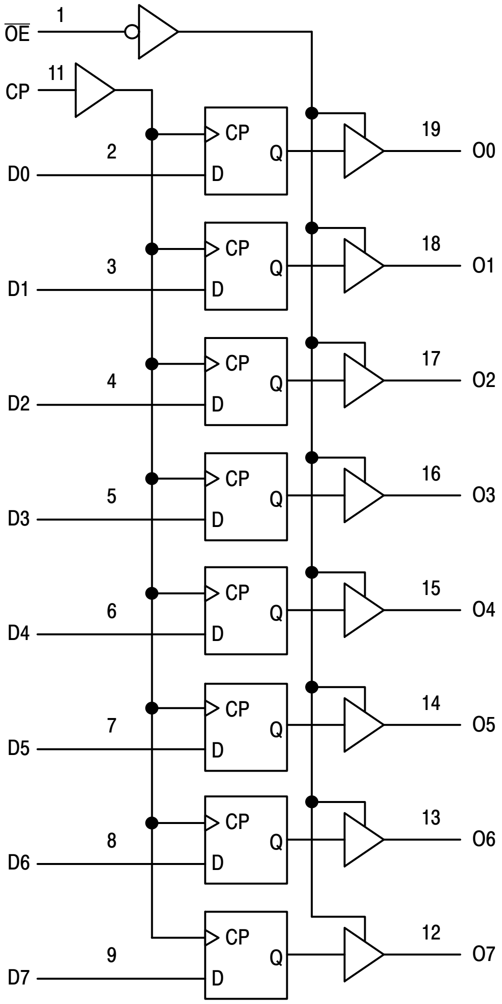


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
$\overline{OE}$ CP	Output Enable Input Clock Pulse Input
D0–D7	Data Inputs
O0–O7	3–State Outputs

TRUTH TABLE

INPUTS			INTERNAL LATCHES	OUTPUTS	
$\overline{OE}$	CP	Dn	Q	On	OPERATING MODE
L L	↑ ↑	l h	L H	L H	Load and Read Register
L	‡	X	NC	NC	Hold and Read Register
H	‡	X	NC	Z	Hold and Disable Outputs
H H	↑ ↑	l h	L H	Z Z	Load Internal Register and Disable Outputs

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low–to–High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low–to–High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
Z = High Impedance State
↑ = Low–to–High Transition
‡ = Not a Low–to–High Transition; For I_{CC} Reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage (Note 1)		−0.5 to +6.5	V
V_O	DC Output Voltage (Note 1)	Active-Mode (High or Low State)	−0.5 to V_{CC} + 0.5	V
		Tri-State Mode	−0.5 to +6.5	
		Power-Down Mode (V_{CC} = 0 V)	−0.5 to +6.5	
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC-20W	96	°C/W
		TSSOP-20	150	
P_D	Power Dissipation in Still Air	SOIC-20W	1302	mW
		TSSOP-20	833	
MSL	Moisture Sensitivity	SOIC-20W All Other Packages	Level 3 Level 1	–
F_R	Flammability Rating Oxygen Index: 28 to 34		UL 94 V-0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	> 2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating	1.65	3.3	5.5	V
		Data Retention Only	1.5	3.3	5.5	
V_I	Digital Input Voltage		0	–	5.5	V
V_O	Output Voltage	Active Mode (High or Low State)	0	–	V_{CC}	V
		Tri-State Mode	0	–	5.5	
		Power Down Mode (V_{CC} = 0 V)	0	–	5.5	
T_A	Operating Free-Air Temperature		−55	–	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V	0	–	20	nS/V
		V_{CC} = 2.3 V to 2.7 V	0	–	20	
		V_I from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0	–	10	
		V_{CC} = 4.5 V to 5.5 V	0	–	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = –40 °C to +85 °C		T_A = –55 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 x V_{CC}		0.65 x V_{CC}		V
			2.3 to 2.7	1.7		1.7		
			2.7 to 3.6	2.0		2.0		
			4.5 to 5.5	0.7 x V_{CC}		0.7 x V_{CC}		
V_{IL}	Low-Level Input Voltage		1.65 to 1.95		0.35 x V_{CC}		0.35 x V_{CC}	V
			2.3 to 2.7		0.7		0.7	
			2.7 to 3.6		0.8		0.8	
			4.5 to 5.5		0.3 x V_{CC}		0.3 x V_{CC}	
V_{OH}	High-Level Output Voltage	$V_I = V_{IH}$ or V_{IL}						V
		I_{OH} = –100 μA	1.65 to 5.5	V_{CC} – 0.1	–	V_{CC} – 0.1	–	
		I_{OH} = –4 mA	1.65	1.2	–	1.2	–	
		I_{OH} = –8 mA	2.3	1.8	–	1.8	–	
		I_{OH} = –12 mA	2.7	2.2	–	2.2	–	
		I_{OH} = –16 mA	3.0	2.4	–	2.4	–	
		I_{OH} = –24 mA	3.0	2.2	–	2.2	–	
		I_{OH} = –32 mA	4.5	3.8		3.8		
V_{OL}	Low-Level Output Voltage	$V_I = V_{IH}$ or V_{IL}						V
		I_{OL} = 100 μA	1.65 to 5.5	–	0.1	–	0.1	
		I_{OL} = 4 mA	1.65	–	0.45	–	0.45	
		I_{OL} = 8 mA	2.3	–	0.6	–	0.6	
		I_{OL} = 12 mA	2.7	–	0.4	–	0.4	
		I_{OL} = 16 mA	3.0	–	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	–	0.55	–	0.55	
		I_{OL} = 32 mA	4.5		0.6		0.6	
I_I	Input Leakage Current	V_I = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I_{OZ}	3-State Output Leakage Current	$V_I = V_{IH}$ or V_{IL}, V_O = 0 V to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	3.6	–	10	–	10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} – 0.6$ V	2.3 to 3.6	–	500	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These values of V_I are used to test DC electrical characteristics only.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = –40 °C to +85 °C		T_A = –55 °C to +125 °C		Unit
				Min	Max	Min	Max	
f_{MAX}	Propagation Delay	Waveform 1	1.65 to 1.95	90	–	90	–	ns
			2.3 to 2.7	100	–	100	–	
			2.7	150	–	150	–	
			3.0 to 3.6	150	–	150	–	
			4.5 to 5.5	150	–	150	–	
t_{PLH}, t_{PHL}	Propagation Delay, CP to On	Waveform 1	1.65 to 1.95	–	15.0	–	15.0	ns
			2.3 to 2.7	–	10.5	–	10.5	
			2.7	–	9.5	–	9.5	
			3.0 to 3.6	–	8.5	–	8.5	
			4.5 to 5.5	–	6.0	–	6.0	
t_{PZH}, t_{PZL}	Output Enable Time	Waveform 2	1.65 to 1.95	–	15.0	–	15.0	ns
			2.3 to 2.7	–	10.5	–	10.5	
			2.7	–	9.5	–	9.5	
			3.0 to 3.6	–	8.5	–	8.5	
			4.5 to 5.5	–	6.0	–	6.0	
t_{PHZ}, t_{PLZ}	Output Enable Time	Waveform 2	1.65 to 1.95	–	10.0	–	10.0	ns
			2.3 to 2.7	–	7.8	–	7.8	
			2.7	–	7.0	–	7.0	
			3.0 to 3.6	–	6.5	–	6.5	
			4.5 to 5.5	–	4.5	–	4.5	
t_s	Setup Time, Dn to CP	Waveform 1	1.65 to 1.95	4.0	–	4.0	–	ns
			2.3 to 2.7	4.0	–	4.0	–	
			2.7	2.5	–	2.5	–	
			3.0 to 3.6	2.5	–	2.5	–	
			4.5 to 5.5	2.5	–	2.5	–	
t_h	Hold Time, Dn to CP	Waveform 1	1.65 to 1.95	2.0	–	2.0	–	ns
			2.3 to 2.7	2.0	–	2.0	–	
			2.7	1.5	–	1.5	–	
			3.0 to 3.6	1.5	–	1.5	–	
			4.5 to 5.5	1.5	–	1.5	–	
t_W	Pulse Width, HIGH or Low	Waveform 3	1.65 to 1.95	4.0	–	4.0	–	ns
			2.3 to 2.7	4.0	–	4.0	–	
			2.7	3.3	–	3.3	–	
			3.0 to 3.6	3.3	–	3.3	–	
			4.5 to 5.5	3.3	–	3.3	–	
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 6)		1.65 to 1.95	–	–	–	–	ns
			2.3 to 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 to 3.6	–	1.0	–	1.0	
			4.5 to 5.5	–	–	–	–	

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

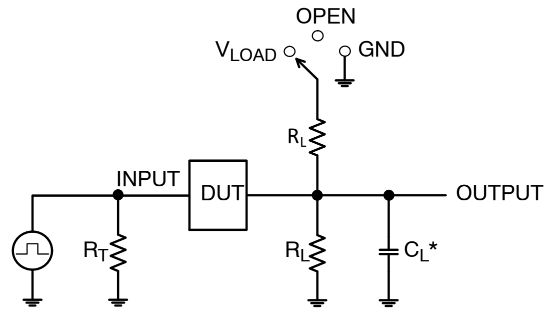
DYNAMIC SWITCHING CHARACTERISTICS

			T_A = +25°C			
Symbol	**Characteristic**	**Condition**	**Min**	**Typ**	**Max**	**Units**
V_{OLP}	Dynamic LOW Peak Voltage (Note 7)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V
V_{OLV}	Dynamic LOW Valley Voltage (Note 7)	V_{CC} = 3.3 V, C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V		0.8		V

7. Number of outputs defined as “n”. Measured with “n−1” outputs switching from HIGH−to−LOW or LOW−to−HIGH. The remaining output is measured in the LOW state.

CAPACITIVE CHARACTERISTICS

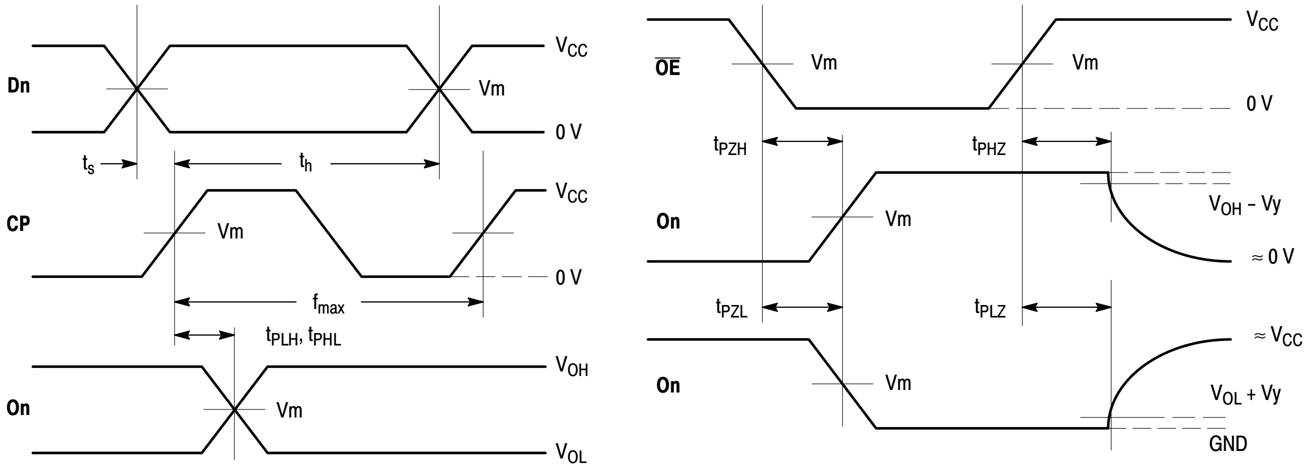
Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	25	pF



Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

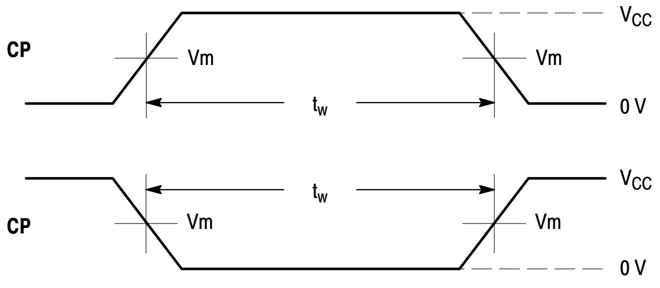
C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit



WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES
$t_R = t_F = 2.5$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns

WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.5$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns



WAVEFORM 3 – PULSE WIDTH
$t_R = t_F = 2.5$ ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \leq 0.8$ V, $V_{OH} \geq 2.0$ V

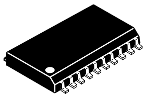
Figure 4. AC Waveforms

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74LCX574DWR2G	LCX574	SOIC−20 (Pb−Free)	1000 / Tape & Reel
MC74LCX574DTR2G	LCX 574	TSSOP−20 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

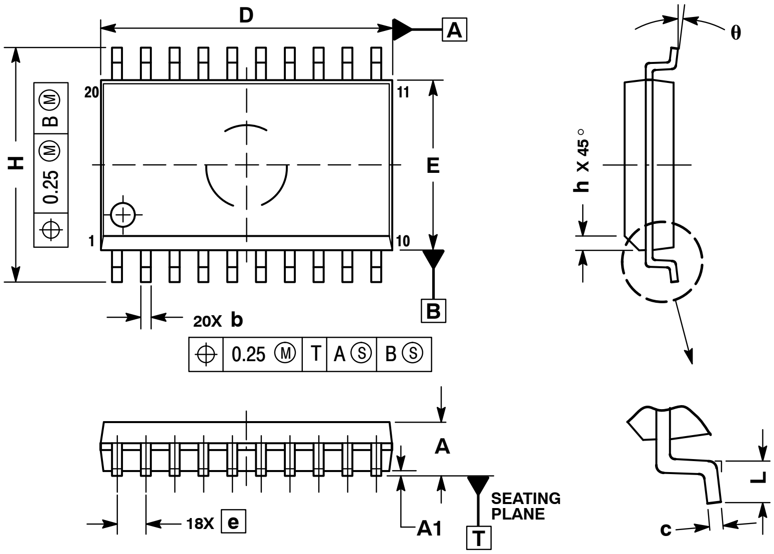


SCALE 1:1

SOIC−20 WB

CASE 751D−05
ISSUE H

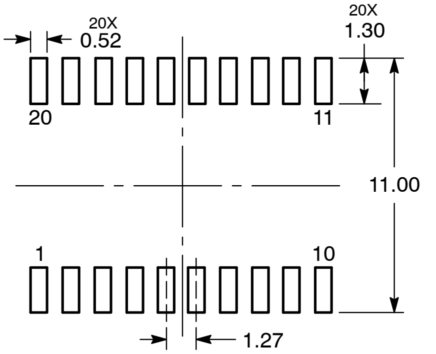
DATE 22 APR 2015



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

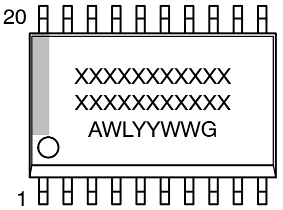
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

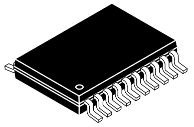
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

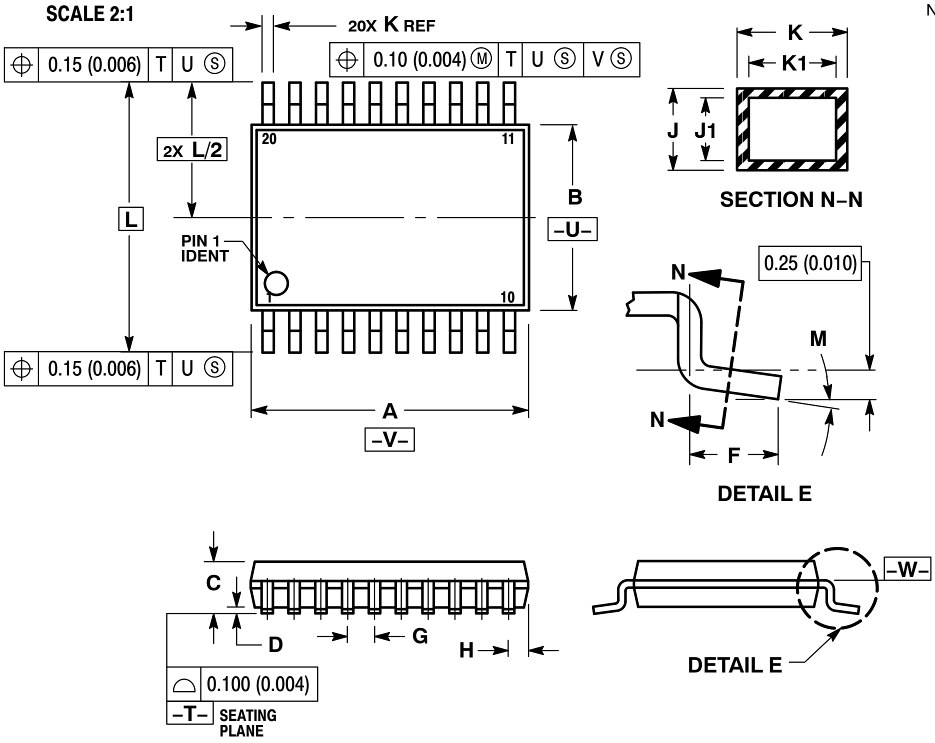
DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−20 WB**	**PAGE 1 OF 1**



SCALE 2:1

TSSOP−20 WB
CASE 948E
ISSUE D

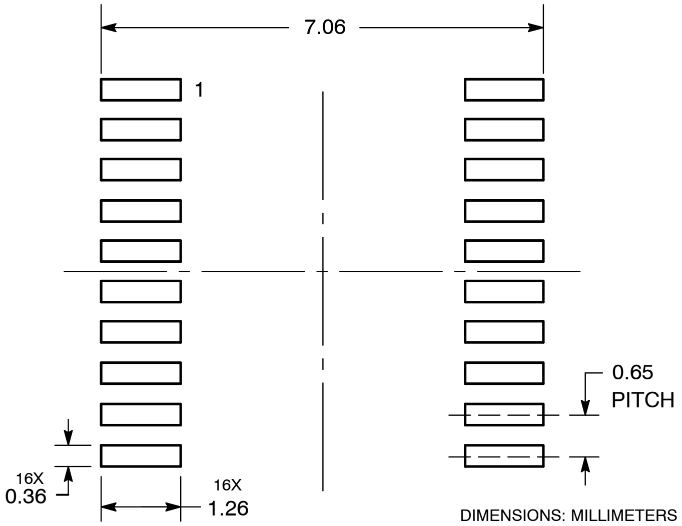
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT*



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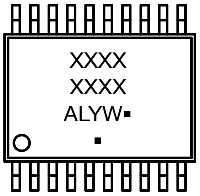
GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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