FEATURES

- TI AM62Ax Application Processor
  - Up to Quad Arm Cortex-A53 MPU at up to 1.4 GHz
  - 32 KB L1 Program Cache per Core
  - 32 KB L1 Data Cache per Core
  - 512 KB Shared L2 Cache
  - JTAG Emulation/Debug
- Single Core Arm Cortex-R5F MCU at up to 800 MHz with 256 KB SRAM
- Deep Learning Accelerator
  - C7x floating point, up to 40 GFLOPS
  - Matrix Multiply Accelerator, up to 2 TOPs (8b)
  - 32 KB L1 Dcache, 64 KB L1 ICache
  - 1.24 MB L2 SRAM
- Vision Processing Accelerator with Image Signal Processing blocks
- AM62Ax Processor Choices
  - AM62A74 (Quad Core, 2 TOPS)
  - AM62A72 (Dual Core, 2 TOPS)
  - AM62A34 (Quad Core, 1 TOPS)
  - AM62A32 (Dual Core, 1 TOPS)
  - AM62A31 (Single Core, 1 TOPS)
- Up To 16 GB LPDDR4 CPU RAM
  - 32 bits wide, 14.9 GB/sec transfer rate
- Up to 128 GB eMMC FLASH
  - 8 bits wide, HS200 speed
- Up to 256 MB Octal SPI NOR FLASH
- Video Encode/Decode Acceleration
- Arm Cortex-R5F processor for boot, resource, and power management.
- Watchdog Timer and Real Time Clock
- Secure Boot
- Crypto Hardware Accelerators (AES, SHA, DRBG, PKA)

STANDARD DDR4 SO-DIMM-260 INTERFACE

- 2 10/100/1000 Mbps EMACs
- 1 MIPI CSI 1.3 Camera Input, 4 lanes up to 2.5 Gbps
- 1 Display Output, up to 2048x1080@60fps
- 3 CAN ports
- 7 UARTs
- 2 USB 2.0 Dual Role Device Ports
- 3 multi-Channel MCASPs
- 2 4 lane MMC/SD/SDIO
- 3 SPI, 3 I2C, GPIO
- eHRPWM, eQEP
- Single 3.3V Input Power Supply
- Compatible with MitySOM-AM62x SOM

APPLICATIONS

- Embedded Instrumentation
- Embedded Artificial Intelligence
- Industrial Automation
- Industrial Instrumentation
- Medical Instrumentation
- Embedded Camera Applications
- Human machine interaction
- Robots
- ADAS & driver monitoring

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity / Interface Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Linux Kernel

DESCRIPTION

The MitySOM-AM62A series of highly configurable, small form-factor processor cards features one of Texas Instruments Sitara AM62Ax Processors. The module includes (optional) eMMC FLASH, (optional) Octal or Quad SPI NOR FLASH, and LPDDR4 RAM memory subsystems. A MitySOM-AM62A provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

The onboard AM62Ax processor provides up to a Quad Core Cortex-A53 64-bit RISC processor with a NEON SIMD coprocessor. This microprocessor unit (MPU) can run a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux.

In addition to the Cortex-A53, the AM62Ax family also offers a Single Core Arm Cortex-R5F MCU at up to 800 MHz as well as a deep learning accelerator engine that is based on a single C7x DSP core. The Cortex-R5F runs independently of the main Cortex-A53 MPU complex and has access to all the on-chip peripherals as well as all external memory and can be used for any purpose. Typical applications for the R5F might include managing an EtherCAT master interface, providing safety critical software operation or real-time handling of attached peripherals, etc.

The deep learning accelerator provides a C7x floating point DSP at up to 40 GFLOPS paired with a Matrix Multiple Accelerator that supports up to 2 TOPS (8b) for artificial intelligence (AI) applications. Coupled with on-chip Vision Processing Accelerators and camera Image Signal Processing, the AM62Ax processor is a good fit for edge AI applications.

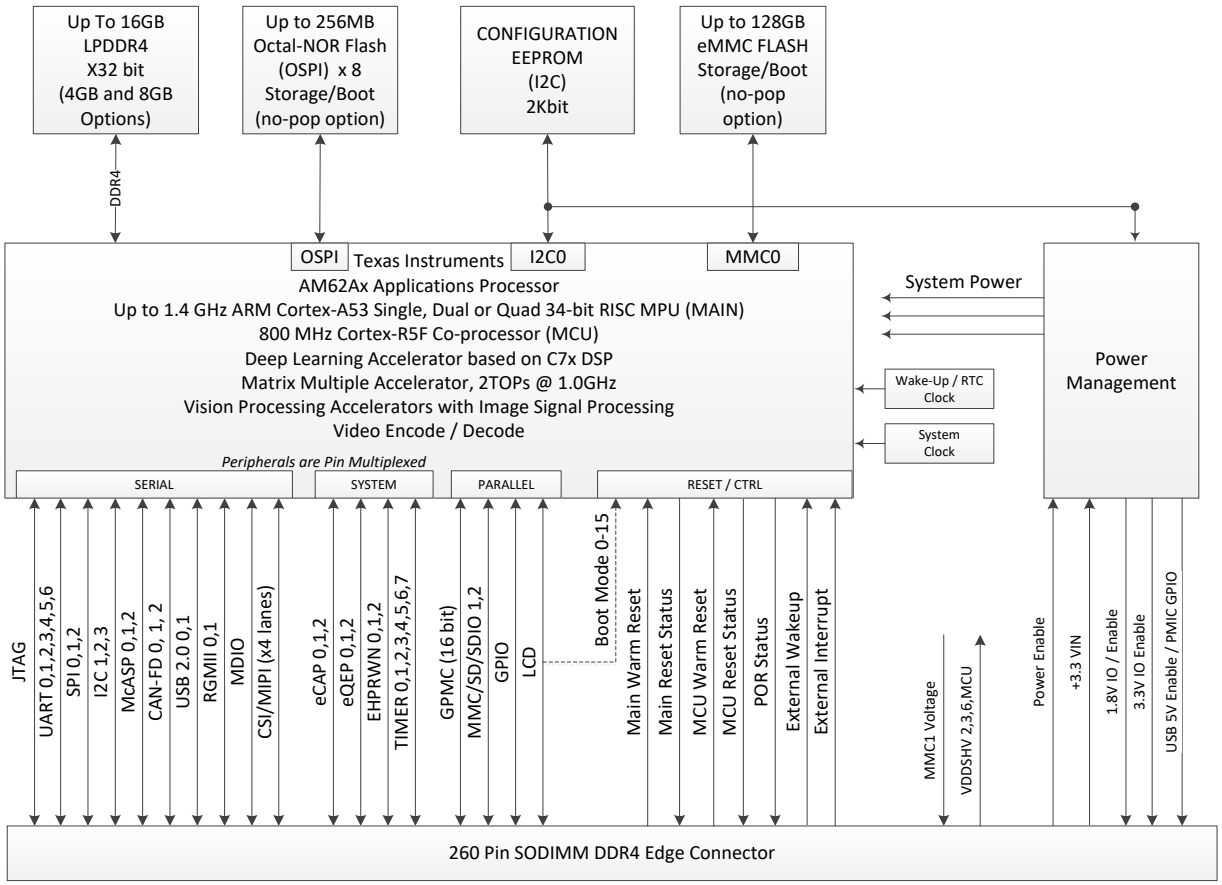

Figure 1 MitySOM-AM62A Block Diagram

Figure 1 provides a top level block diagram of the MitySOM-AM62A processor card. As shown in the figure, the primary interface to the MitySOM-AM62A is through a standard DDR4 SO-DIMM-260 card edge interface. The interface provides power, synchronous serial connectivity, and many other interfaces provided by the Sitara processor. Details of the SO-DIMM-260 connector interface are included in the SO-DIMM-260 Interface Description, below.

MitySOM-AM62A Onboard DDR Memory Options

The AM62Ax processor includes one dedicated 32 bit LPDDR4 SDRAM memory interface. The MitySOM-AM62A includes up to 16 GB of LPDDR4 RAM integrated on board the module. The memory bus interface is capable of burst transfer rates of 14930 MB / second.

MitySOM-AM62A Onboard Storage Memory

eMMC FLASH (Optional)

Up to 128GB of on-board eMMC FLASH memory is connected to the AM62Ax processor using the MMC0 interface peripheral. The eMMC FLASH memory is typically used to store the following types of data:

- Bootloaders
- ARM Linux embedded root file-system
- runtime ARM software
- runtime application data (non-volatile storage)

NOR FLASH (Optional)

Up to 256 MB of on-board Octal or Quad SPI NOR FLASH memory is connected to the AM62Ax using the OSPI/QSPI peripheral interface. The AM62Ax provides additional SPI interfaces with both interfaces available on the SO-DIMM connector. This memory may be desirable for applications requiring more reliable/tolerant storage or faster access times.

Configuration EEPROM

The MitySOM-AM62A contains a (minimum) 256 x 8-bit EEPROM that is used to hold configuration data for the module. The EEPROM is connected to the AM62Ax using the I2C0 interface at address 1010XXXb (0x50 to 0x57). This EEPROM is not available for customer use.

External Interfaces

The AM62Ax makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications. A list of the interfaces/functions that are available to the user via the edge connector interface is provided below.

- 2 Universal Serial Bus (USB) 2.0 High-Speed port supporting host/peripheral/dual role mode
- 3 Controller-Area Network (CAN) ports with Can-FD support
- 3 Multichannel Audio Serial Ports (McASP)
- 2 Industrial Gigabit Ethernet MAC's (10/100/1000 Mbps)
- 2 SD/SDIO 4-bit ports supporting UHS-I
- 1 24 bit RGB display driver
- 1 MIPI Camera Serial Interface (CSI-Rx), 4 Lane with DPHY.
- 3 Enhanced Capture (eCAP) Modules
- 3 Enhanced PWM (ePWM) modules
- 3 32-bit Enhanced Quadrature Pulse Encoder (eQPE) modules
- 4 Timers
- 3 Serial Peripheral (SPI) ports
- 7 Universal Asynchronous Receive/Transmit (UART) ports
- 3 Inter-Integrated Circuit (I2C) ports (I2C1, I2C2, & I2C3)
- General Purpose Memory Controller (GPMC) interface
- JTAG/Debugger port

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

Software and Application Development Support

Users of the AM62Ax are encouraged to develop applications using the MitySOM-AM62A software development kit provided by Critical Link LLC. The SDK is an expansion of the TI platform support package for the AM62Ax and includes a Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

Growth Options

The AM62Ax has been designed to support several upgrade options. These options include various speed grades, number of available Cortex-A53 cores, memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact a Critical Link sales representative.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc	3.5 V
Storage Temperature Range	-65°C to 80°C

OPERATING CONDITIONS

Commercial Temperature Range	0°C to 70°C
Industrial Temperature Range	-40°C to 85°C

SO-DIMM-260 Interface Description

The primary interface connector for the MitySOM-AM62A is the DDR4 SO-DIMM card edge interface which contains 5 types of signals:

- Power input (P)
- Power Output (PO)
- Dedicated signals mapped to the on-board Power Management device (PM)
- Dedicated signals mapped to the AM62Ax device (I/O)
- Multi-function signals mapped to the AM62Ax device (I/O/IO)
- Unconnected pins on the edge interface are noted with a "-" symbol

Table 1 contains a summary of the MitySOM-AM62A pin mapping.

Table 1 SO-DIMM Pin-Out

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
1	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
2	P	LED_RTN	7	-	-	-	-	-	-	-	-	-	-	-
3	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
4	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
5	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
6	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
7	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
8	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
9	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
10	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
11	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
12	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
13	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
14	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
15	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
16	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
17	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
18	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
19	P	+3.3V VIN	2	-	-	-	-	-	-	-	-	-	-	-
20	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
21	O	VDD_3V3_ENABLE	2,8	-	+3.3V VIN	-	-	-	-	-	-	-	-	-
22	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
23	PO	VDD_1V8	2	-	-	-	-	-	-	-	-	-	-	-
24	P	GND	-	-	-	-	-	-	-	-	-	-	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
25	PO	VDD_1V8	2	-	-	-	-	-	-	-	-	-	-	-
26	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
27	PO	VDD_1V8	2	-	-	-	-	-	-	-	-	-	-	-
28	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
29	PO	VDD_1V8	2	-	-	-	-	-	-	-	-	-	-	-
30	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
31	P	VDDSHV2	-	-	VDDSHV2	-	-	-	-	-	-	-	-	-
32	A	VMON_VSYS	5	H12	+1V Max	-	-	-	-	-	-	-	-	-
33	P	VDDSHV2	-	-	VDDSHV2	-	-	-	-	-	-	-	-	-
34	P	VDDSHV_MCU	-	-	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
35	P	VDDSHV3	-	-	VDDSHV3	-	-	-	-	-	-	-	-	-
36	P	VDDSHV_MCU	-	-	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
37	P	VDDSHV3	-	-	VDDSHV3	-	-	-	-	-	-	-	-	-
38	P	VDDSHV6	-	-	VDDSHV6	-	-	-	-	-	-	-	-	-
39	P	VDDSHV3	-	-	VDDSHV3	-	-	-	-	-	-	-	-	-
40	I	PMIC_PBn	3	-	-	-	-	-	-	-	-	-	-	-
41	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
42	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
43	-	-	-	-	-	-	-	-	-	-	-	-	-	-
44	-	-	-	-	-	-	-	-	-	-	-	-	-	-
45	-	-	-	-	-	-	-	-	-	-	-	-	-	-
46	-	-	-	-	-	-	-	-	-	-	-	-	-	-
47	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
48	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
49	-	-	-	-	-	-	-	-	-	-	-	-	-	-
50	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
51	-	-	-	-	-	-	-	-	-	-	-	-	-	-
52	-	-	-	-	-	-	-	-	-	-	-	-	-	-
53	-	-	-	-	-	-	-	-	-	-	-	-	-	-
54	-	-	-	-	-	-	-	-	-	-	-	-	-	-
55	-	-	-	-	-	-	-	-	-	-	-	-	-	-
56	-	-	-	-	-	-	-	-	-	-	-	-	-	-
57	-	-	-	-	-	-	-	-	-	-	-	-	-	-
58	-	-	-	-	-	-	-	-	-	-	-	-	-	-
59	-	-	-	-	-	-	-	-	-	-	-	-	-	-
60	-	-	-	-	-	-	-	-	-	-	-	-	-	-
61	-	-	-	-	-	-	-	-	-	-	-	-	-	-
62	-	-	-	-	-	-	-	-	-	-	-	-	-	-
63	-	-	-	-	-	-	-	-	-	-	-	-	-	-
64	-	-	-	-	-	-	-	-	-	-	-	-	-	-
65	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
66	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
67	I	CSI0_RXN3	-	AB11	D-PHY	-	-	-	-	-	-	-	-	-
68	O	VCC_5V0_EN	8,9	-	-	-	-	-	-	-	-	-	-	-
69	I	CSI0_RXP3	-	AB10	D-PHY	-	-	-	-	-	-	-	-	-
70	O	USB1_DRVVBUS	-	D19	+3.3VIO	-	-	-	-	-	-	GPIO1_51	-	-
71	I	CSI0_RXN2	-	AA13	D-PHY	-	-	-	-	-	-	-	-	-
72	IO	USB1_DP	-	Y10	USB-PHY	-	-	-	-	-	-	-	-	-
73	I	CSI0_RXP2	-	AA12	D-PHY	-	-	-	-	-	-	-	-	-
74	IO	USB1_DM	-	Y11	USB-PHY	-	-	-	-	-	-	-	-	-
75	I	CSI0_RXP1	-	Y14	D-PHY	-	-	-	-	-	-	-	-	-
76	I	USB1_VBUS_DETECT	4	V6	+3.3VIO	-	-	-	-	-	-	-	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
77	I	CSI0_RXN1	-	Y13	D-PHY	-	-	-	-	-	-	-	-	-
78	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
79	I	CSI0_RXP0	-	W13	D-PHY	-	-	-	-	-	-	-	-	-
80	O	USB0_DRVVBUS	-	C20	+3.3VIO	-	-	-	-	-	-	-	-	-
81	I	CSI0_RXN0	-	W12	D-PHY	-	-	-	-	-	-	-	-	-
82	IO	USB0_DM	-	AA10	USB-PHY	-	-	-	-	-	-	-	-	-
83	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
84	IO	USB0_DP	-	AA9	USB-PHY	-	-	-	-	-	-	-	-	-
85	I	CSI0_RXCLKP	-	AB13	D-PHY	-	-	-	-	-	-	-	-	-
86	I	USB0_VBUS_DETECT	4	V8	+3.3VIO	-	-	-	-	-	-	-	-	-
87	I	CSI0_RXCLKN	-	AB14	D-PHY	-	-	-	-	-	-	-	-	-
88	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
89	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
90	IO	RGMII1_RD3	-	V14	VDDSHV2	-	-	-	-	-	-	GPIO0_84	-	-
91	IO	RGMII2_TD1	-	Y18	VDDSHV2	RMII2_TXD1	MCASP2_ACLKR	-	-	MCASP2_AXR8	-	GPIO0_90	-	-
92	IO	RGMII1_RD2	-	W15	VDDSHV2	PR0_UART0_RTSn	-	-	-	-	-	GPIO0_83	-	-
93	IO	RGMII2_TD0	-	AA19	VDDSHV2	RMII2_TXD0	MCASP2_AXR6	-	-	-	-	GPIO0_89	-	-
94	IO	RGMII1_RD0	-	AB16	VDDSHV2	RMII1_RXD0	-	-	-	-	-	GPIO0_81	-	-
95	IO	RGMII2_TX_CTL	-	Y19	VDDSHV2	RMII2_TX_EN	MCASP2_AXR4	-	-	-	-	GPIO0_87	-	-
96	IO	RGMII1_RD1	-	V15	VDDSHV2	RMII1_RXD1	-	-	-	-	-	GPIO0_82	-	-
97	IO	RGMII2_TD3	-	W17	VDDSHV2	-	MCASP2_ACLKX	-	-	PR0_ECAP0_SYNC_OUT	PR0_UART0_CTSn	GPIO1_0	EQEP2_S	-
98	IO	RGMII1_RX_CTL	-	AA15	VDDSHV2	RMII1_RX_ER	-	-	-	-	-	GPIO0_79	-	-
99	IO	RGMII2_TXC	-	AB19	VDDSHV2	RMII2_CRS_DV	MCASP2_AXR5	-	-	-	-	GPIO0_88	-	-
100	IO	RGMII1_RXC	-	AA16	VDDSHV2	RMII1_REF_CLK	PR0_UART0_CTSn	-	-	-	-	GPIO0_80	-	-
101	IO	RGMII2_TD2	-	AA18	VDDSHV2	-	MCASP2_AFSX	-	-	PR0_ECAP0_IN_APWM_OUT	-	GPIO0_91	EQEP2_I	-
102	IO	RGMII1_TD2	-	Y16	VDDSHV2	PR0_UART0_RXD	-	-	-	-	-	GPIO0_77	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
103	IO	RGMII2_RD2	-	AB21	VDDSHV2	-	MCASP2_AXR0	-	-	PR0_UART0_RXD	-	GPIO1_5	EQEP2_A	-
104	IO	RGMII1_TD3	-	AA17	VDDSHV2	PR0_UART0_TXD	-	-	-	-	-	GPIO0_78	-	-
105	IO	RGMII2_RD1	-	Y20	VDDSHV2	RMII2_RXD1	MCASP2_AFSR	-	-	MCASP2_AXR7	-	GPIO1_4	-	-
106	IO	RGMII1_TXC	-	AB17	VDDSHV2	RMII1_CRS_DV	-	-	-	-	-	GPIO0_74	-	-
107	IO	RGMII2_RD3	-	AB20	VDDSHV2	-	AUDIO_EXT_REFCLK0	-	-	PR0_UART0_TXD	-	GPIO1_6	EQEP2_B	-
108	IO	RGMII1_TX_CTL	-	W16	VDDSHV2	RMII1_TX_EN	-	-	-	-	-	GPIO0_73	-	-
109	IO	RGMII2_RX_CTL	-	W18	VDDSHV2	RMII2_RX_ER	MCASP2_AXR3	-	-	-	-	GPIO1_1	-	-
110	IO	RGMII1_TD0	-	Y17	VDDSHV2	RMII1_TXD0	-	-	-	-	-	GPIO0_75	-	-
111	IO	RGMII2_RD0	-	AA21	VDDSHV2	RMII2_RXD0	MCASP2_AXR2	-	-	-	PR0_UART0_RTSn	GPIO1_3	-	-
112	IO	RGMII1_TD1	-	V16	VDDSHV2	RMII1_TXD1	-	-	-	-	-	GPIO0_76	-	-
113	IO	RGMII2_RXC	-	AA20	VDDSHV2	RMII2_REF_CLK	MCASP2_AXR1	-	-	PR0_ECAP0_SYNC_IN	-	GPIO1_2	-	-
114	IO	MDIO0_MDC	-	V12	VDDSHV2	-	-	-	-	-	-	GPIO0_86	-	-
115	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
116	IO	MDIO0_MDIO	-	V13	VDDSHV2	-	-	-	-	-	-	GPIO0_85	-	-
117	IO	VOUT0_PCLK	-	AA22	VDDSHV3	GPMC0_A19	-	-	UART2_CTSn	-	-	GPIO0_64	PR0_ECAP0_IN_APWM_OUT	-
118	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
119	IO	VOUT0_VSYNC	-	V17	VDDSHV3	GPMC0_A18	-	-	UART2_RTSn	-	-	GPIO0_63	-	-
120	IO	VOUT0_DATA15	-	Y22	VDDSHV3	GPMC0_A15	-	-	UART4_CTSn	-	-	GPIO0_60	-	-
121	IO	VOUT0_HSYNC	-	T18	VDDSHV3	GPMC0_A16	-	-	UART3_RTSn	-	-	GPIO0_61	-	-
122	IO	VOUT0_DATA11	-	W21	VDDSHV3	GPMC0_A11	-	-	UART6_CTSn	-	-	GPIO0_56	-	-
123	IO	VOUT0_DE	-	U17	VDDSHV3	GPMC0_A17	-	-	UART3_CTSn	-	-	GPIO0_62	-	-
124	IO	VOUT0_DATA14	-	Y21	VDDSHV3	GPMC0_A14	-	-	UART4_RTSn	-	-	GPIO0_59	-	-
125	IO	VOUT0_DATA7	-	V21	VDDSHV3	GPMC0_A7	-	-	UART5_TXD	-	-	GPIO0_52	-	-
126	IO	VOUT0_DATA13	-	W19	VDDSHV3	GPMC0_A13	-	-	UART5_CTSn	-	-	GPIO0_58	-	-
127	IO	VOUT0_DATA6	-	V22	VDDSHV3	GPMC0_A6	-	-	UART5_RXD	-	-	GPIO0_51	-	-
128	IO	VOUT0_DATA9	-	V18	VDDSHV3	GPMC0_A9	-	-	UART6_TXD	-	-	GPIO0_54	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
129	IO	VOUT0_DATA5	-	U18	VDDSHV3	GPMC0_A5	-	-	UART4_TXD	-	-	GPIO0_50	-	-
130	IO	VOUT0_DATA12	-	W20	VDDSHV3	GPMC0_A12	-	-	UART5_RTSn	-	-	GPIO0_57	-	-
131	IO	VOUT0_DATA4	-	T19	VDDSHV3	GPMC0_A4	-	-	UART4_RXD	-	-	GPIO0_49	-	-
132	IO	VOUT0_DATA8	-	V19	VDDSHV3	GPMC0_A8	-	-	UART6_RXD	-	-	GPIO0_53	-	-
133	IO	VOUT0_DATA3	-	U19	VDDSHV3	GPMC0_A3	-	-	UART3_TXD	-	-	GPIO0_48	-	-
134	IO	VOUT0_DATA10	-	W22	VDDSHV3	GPMC0_A10	-	-	UART6_RTSn	-	-	GPIO0_55	-	-
135	IO	VOUT0_DATA2	-	U20	VDDSHV3	GPMC0_A2	-	-	UART3_RXD	-	-	GPIO0_47	-	-
136	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
137	IO	VOUT0_DATA1	-	U21	VDDSHV3	GPMC0_A1	-	-	UART2_TXD	-	-	GPIO0_46	-	-
138	IO	GPMC0_WAIT1	-	R17	VDDSHV3	VOUT0_EXTPCLK	GPMC0_A21	UART6_RXD	-	-	-	GPIO0_38	EQEP2_I	-
139	IO	VOUT0_DATA0	-	U22	VDDSHV3	GPMC0_A0	-	-	UART2_RXD	-	-	GPIO0_45	-	-
140	IO	GPMC0_WAIT0	-	R18	VDDSHV3	-	MCASP1_AFSX	-	-	-	TRC_DATA12	GPIO0_37	-	-
141	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
142	IO	GPMC0_AD7	1	P21	VDDSHV3	-	-	MCASP2_AXR11	-	-	RC_DATA5	GPIO0_22	-	-
143	IO	GPMC0_AD15	1	T21	VDDSHV3	VOUT0_DATA23	UART5_TXD	MCASP2_ACLKR	-	-	TRC_DATA19	GPIO0_30	UART2_RTSn	-
144	IO	GPMC0_AD5	1	P18	VDDSHV3	-	-	MCASP2_AXR9	-	-	TRC_DATA3	GPIO0_20	-	-
145	IO	GPMC0_AD14	1	T20	VDDSHV3	VOUT0_DATA22	UART5_RXD	MCASP2_AFSR	-	-	TRC_DATA20	GPIO0_29	UART2_CTSn	-
146	IO	GPMC0_AD6	1	P19	VDDSHV3	-	-	MCASP2_AXR10	-	-	TRC_DATA4	GPIO0_21	-	-
147	IO	GPMC0_AD13	1	R21	VDDSHV3	VOUT0_DATA21	UART4_TXD	MCASP2_ACLKX	-	-	TRC_DATA21	GPIO0_28	-	-
148	IO	GPMC0_AD1	1	N20	VDDSHV3	-	-	MCASP2_AXR5	-	-	TRC_CTL	GPIO0_16	-	-
149	IO	GPMC0_AD11	1	R22	VDDSHV3	VOUT0_DATA19	UART3_TXD	MCASP2_AXR3	-	-	TRC_DATA23	GPIO0_26	-	-
150	IO	GPMC0_AD2	1	N19	VDDSHV3	-	-	MCASP2_AXR6	-	-	TRC_DATA0	GPIO0_17	-	-
151	IO	GPMC0_AD12	1	T22	VDDSHV3	VOUT0_DATA20	UART4_RXD	MCASP2_AFSX	-	-	TRC_DATA22	GPIO0_27	-	-
152	IO	GPMC0_AD3	1	N18	VDDSHV3	-	-	MCASP2_AXR7	-	-	TRC_DATA1	GPIO0_18	-	-
153	IO	GPMC0_AD10	1	R20	VDDSHV3	VOUT0_DATA18	UART3_RXD	MCASP2_AXR2	-	-	-	GPIO0_25	OBSCLK0	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
154	IO	GPMC0_AD0	1	N21	VDDSHV3	-	-	MCASP2_AXR4	-	-	TRC_CLK	GPIO0_15	-	-
155	IO	GPMC0_AD8	1	P22	VDDSHV3	VOUT0_DATA16	UART2_RXD	MCASP2_AXR0	-	-	-	GPIO0_23	-	-
156	IO	GPMC0_AD4	1	N17	VDDSHV3	-	-	MCASP2_AXR8	-	-	TRC_DATA2	GPIO0_19	-	-
157	IO	GPMC0_AD9	1	R19	VDDSHV3	VOUT0_DATA17	UART2_TXD	MCASP2_AXR1	-	-	-	GPIO0_24	-	-
158	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
159	IO	GPMC0_BE1n	-	M18	VDDSHV3	-	-	MCASP2_AXR12	-	-	TRC_DATA11	GPIO0_36	-	-
160	IO	GPMC0_CSn0	-	M19	VDDSHV3	-	-	MCASP2_AXR14	-	-	TRC_DATA15	GPIO0_41	-	-
161	IO	GPMC0_BE0n_CLE	-	L19	VDDSHV3	-	MCASP1_ACLKX	-	-	-	TRC_DATA10	GPIO0_35	-	-
162	IO	GPMC0_DIR	-	K18	VDDSHV3	PR0_ECAP0_IN_APWM_OUT	-	MCASP2_AXR13	-	-	TRC_DATA14	-	EQEP2_S	-
163	IO	GPMC0_OEn_REn	-	L17	VDDSHV3	-	MCASP1_AXR1	-	-	-	TRC_DATA8	GPIO0_33	-	-
164	IO	GPMC0_ADVn_ALE	-	L18	VDDSHV3	-	MCASP1_AXR2	-	-	-	TRC_DATA7	GPIO0_32	-	-
165	IO	GPMC0_WEn	-	K19	VDDSHV3	-	MCASP1_AXR0	-	-	-	TRC_DATA9	GPIO0_34	-	-
166	IO	GPMC0_CSn1	-	M21	VDDSHV3	-	-	MCASP2_AXR15	-	-	TRC_DATA16	GPIO0_42	-	-
167	IO	GPMC0_CSn3	-	M20	VDDSHV3	I2C2_SDA	GPMC0_A20	UART4_TXD	MCASP1_AXR5	-	TRC_DATA18	GPIO0_44	MCASP1_ACLKR	-
168	IO	GPMC0_CSn2	-	M22	VDDSHV3	I2C2_SCL	MCASP1_AXR4	UART4_RXD	-	-	TRC_DATA17	GPIO0_43	MCASP1_AFSR	-
169	IO	GPMC0_WPn	-	K17	VDDSHV3	AUDIO_EXT_REFCLK1	GPMC0_A22	UART6_TXD	-	-	TRC_DATA13	GPIO0_39	-	-
170	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
171	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
172	PO	VDDSHV_SDIO	-	-	-	-	-	-	-	-	-	-	-	-
173	IO	MMC2_CLK	-	H22	VDDSHV6	MCASP1_ACLKR	MCASP1_AXR5	UART6_RXD	-	-	-	GPIO0_69	-	-
174	IO	GPMC0_CLK	-	N22	VDDSHV3	-	MCASP1_AXR3	GPMC0_FCLK_MUX	-	-	TRC_DATA6	GPIO0_31	-	-
175	IO	MMC2_DAT2	-	F20	VDDSHV6	MCASP1_AXR2	-	UART5_TXD	-	-	-	GPIO0_66	-	-
176	I	VSEL_SD	8	-	-	-	-	-	-	-	-	-	-	-
177	IO	MMC2_DAT3	-	G21	VDDSHV6	MCASP1_AXR3	-	UART5_RXD	-	-	-	GPIO0_65	-	-
178	IO	MMC1_CLK	-	E22	VDDSHV_SDIO	-	TIMER_IO4	UART3_RXD	-	-	-	GPIO1_46	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
179	IO	MMC2_CMD	-	G22	VDDSHV6	MCASP1_AFSR	MCASP1_AXR4	UART6_TXD	-	-	-	GPIO0_70	-	-
180	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
181	IO	MMC2_DAT1	-	F21	VDDSHV6	MCASP1_AXR1	-	-	-	-	-	GPIO0_67	-	-
182	IO	MMC1_DAT3	-	D22	VDDSHV_SDIO	CP_GEMAC_CPTS0_TS_COMP	TIMER_IO0	UART2_RXD	-	-	-	GPIO1_42	-	-
183	IO	MMC2_DAT0	-	E20	VDDSHV6	MCASP1_AXR0	-	-	-	-	-	GPIO0_68	-	-
184	IO	MMC1_DAT2	-	C22	VDDSHV_SDIO	CP_GEMAC_CPTS0_TS_SYNC	TIMER_IO1	UART2_TXD	-	-	-	GPIO1_43	-	-
185	IO	MMC2_SDWP	-	E21	VDDSHV6	MCASP1_AFSX	-	UART4_TXD	-	-	-	GPIO0_72	-	-
186	IO	MMC1_DAT0	-	B22	VDDSHV_SDIO	CP_GEMAC_CPTS0_HW2TSPUSH	TIMER_IO3	UART2_CTSn	ECAP2_IN_APWM_OUT	-	-	GPIO1_45	-	-
187	IO	MMC2_SDCD	-	F22	VDDSHV6	MCASP1_ACLKX	-	UART4_RXD	-	-	-	GPIO0_71	-	-
188	IO	MMC1_CMD	-	C21	VDDSHV_SDIO	-	TIMER_IO5	UART3_TXD	-	-	-	GPIO1_47	-	-
189	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
190	IO	MMC1_DAT1	-	D21	VDDSHV_SDIO	CP_GEMAC_CPTS0_HW1TSPUSH	TIMER_IO2	UART2_RTSn	ECAP1_IN_APWM_OUT	-	-	GPIO1_44	-	-
191	IO	MCASP0_ACLKX	-	A19	+3.3VIO	SPI2_CS1	ECAP2_IN_APWM_OU	-	-	-	-	GPIO1_11	EQEP1_A	-
192	IO	MMC1_SDCD	-	E18	+3.3VIO	UART6_RXD	TIMER_IO6	UART3_RTSn	-	-	-	GPIO1_48	-	-
193	IO	MCASP0_ACLKR	-	A21	+3.3VIO	SPI2_CLK	UART1_TXD	-	-	-	EHRPWM0_B	GPIO1_14	EQEP1_I	-
194	IO	MMC1_SDWP	-	D18	+3.3VIO	UART6_TXD	TIMER_IO7	UART3_CTSn	-	-	-	GPIO1_49	-	-
195	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
196	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
197	IO	MCASP0_AXR3	-	C19	+3.3VIO	SPI2_D0	UART1_CTSn	UART6_RXD	PR0_IEP0_EDIO_DATA_IN_OUT28	ECAP1_IN_APWM_OUT	PR0_UART0_RXD	GPIO1_7	EQEP0_A	-
198	IO	MCASP0_AFSX	-	A20	+3.3VIO	SPI2_CS3	AUDIO_EXT_REFCLK	-	-	-	-	GPIO1_12	EQEP1_B	-
199	IO	MCASP0_AXR2	-	B19	+3.3VIO	SPI2_D1	UART1_RTSn	UART6_TXD	PR0_IEP0_EDIO_DATA_IN_OU	ECAP2_IN_APWM_OUT	PR0_UART0_TXD	GPIO1_8	EQEP0_B	-
200	IO	MCASP0_AFSR	-	B21	+3.3VIO	SPI2_CS0	UART1_RXD	EHRPWM0_A	-	-	-	GPIO1_13	EQEP1_S	-
201	IO	MCASP0_AXR1	-	B18	+3.3VIO	SPI2_CS2	ECAP1_IN_APWM_O	-	-	PR0_UART0_RXD	EHRPWM1_A	GPIO1_9	EQEP0_S	-
202	IO	EXT_REFCLK1	-	B16	+3.3VIO	SYNC1_OUT	SPI2_CS3	SYSCLKOUT0	TIMER_IO4	CLKOUT0	CP_GEMAC_CPTS0_RFT_CLK	GPIO1_30	ECAP0_IN_APWM_OUT	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
203	IO	MCASP0_AXR0	-	B20	+3.3VIO	PR0_ECAP0_IN_APWM_OUT	AUDIO_EXT_REFCLK0	-	-	PR0_UART0_TXD	EHRPWM1_B	GPIO1_10	EQEP0_I	-
204	I	EXTINTn	-	F17	+3.3VIO	-	-	-	-	-	-	GPIO1_31	-	-
205	IO	I2C1_SCL	-	C17	+3.3VIO	UART1_RXD	TIMER_IO0	SPI2_CS1	EHRPWM0_SYNCI	-	-	GPIO1_28	EHRPWM2_A	MMC2_SDCD
206	IO	MCAN0_RX	-	C18	+3.3VIO	UART5_TXD	TIMER_IO3	SYNC3_OUT	UART1_RIn	EQEP2_S	PR0_UART0_TXD	GPIO1_25	MCASP2_AXR1	EHRPWM_TZn_IN4
207	IO	I2C1_SDA	-	E17	+3.3VIO	UART1_TXD	TIMER_IO1	SPI2_CLK	EHRPWM0_SYNCO	-	-	GPIO1_29	EHRPWM2_B	MMC2_SDWP
208	IO	MCAN0_TX	-	B17	+3.3VIO	UART5_RXD	TIMER_IO2	SYNC2_OUT	UART1_DTRn	EQEP2_I	PR0_UART0_RXD	GPIO1_24	MCASP2_AXR0	EHRPWM_TZn_IN3
209	IO	SPI0_D1	-	E15	+3.3VIO	CP_GEMAC_CPTS0_HW2TSPUSH	EHRPWM_TZn_IN0	-	-	-	-	GPIO1_19	-	-
210	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
211	IO	SPI0_D0	-	B15	+3.3VIO	CP_GEMAC_CPTS0_HW1TSPUSH	EHRPWM1_B	-	-	-	-	GPIO1_18	-	-
212	IO	UART0_RTSn	-	C15	+3.3VIO	SPI0_CS3	I2C3_SDA	UART2_TXD	TIMER_IO7	AUDIO_EXT_REFCLK1	PR0_ECAP0_IN_APWM_OUT	GPIO1_23	MCASP2_ACLKX	MMC2_SDWP
213	IO	SPI0_CS1	-	C16	+3.3VIO	CP_GEMAC_CPTS0_TS_COMP	EHRPWM0_B	ECAP0_IN_APWM_OUT	-	-	-	GPIO1_16	-	EHRPWM_TZn_IN5
214	IO	UART0_RXD	-	E14	+3.3VIO	ECAP1_IN_APWM_OUT	SPI2_D0	EHRPWM2_A	-	-	-	GPIO1_20	-	-
215	IO	SPI0_CS0	-	D16	+3.3VIO	-	EHRPWM0_A	-	-	-	PR0_ECAP0_SYNC_IN	GPIO1_15	-	-
216	IO	UART0_TXD	-	D15	+3.3VIO	ECAP2_IN_APWM_OUT	SPI2_D1	EHRPWM2_B	-	-	-	GPIO1_21	-	-
217	IO	SPI0_CLK	-	A17	+3.3VIO	CP_GEMAC_CPTS0_TS_SYNC	EHRPWM1_A	-	-	-	-	GPIO1_17	-	-
218	IO	UART0_CTSn	-	F14	+3.3VIO	SPI0_CS2	I2C3_SCL	UART2_RXD	TIMER_IO6	AUDIO_EXT_REFCLK0	PR0_ECAP0_SYNC_OUT	GPIO1_22	MCASP2_AFSX	MMC2_SDCD
219	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
220	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
221	IO	MCU_RESETSTATz	-	D14	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_21	-	-
222	IO	EMU0	-	C13	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
223	I	MCU_RESETz	-	C12	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
224	O	TDO	-	C14	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
225	O	RESETSTATz	-	F19	+3.3VIO	-	-	-	-	-	-	-	-	-
226	I	EMU_RSTn	-	-	-	-	-	-	-	-	-	-	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
227	I	RESET_REQz	-	E19	+3.3VIO	-	-	-	-	-	-	-	-	-
228	IO	EMU1	-	E10	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
229	O	PORz_OUT	-	F18	+3.3VIO	-	-	-	-	-	-	-	-	-
230	I	TMS	-	B14	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
231	IO	MCU_I2C0_SDA	-	D9	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_18	-	-
232	I	TDI	-	A16	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
233	IO	MCU_I2C0_SCL	-	E12	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_17	-	-
234	I	TRSTn	-	F15	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
235	IO	MCU_SPI0_D1	-	B12	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_4	-	-
236	I	TCK	-	A14	VDDSHV_MCU	-	-	-	-	-	-	-	-	-
237	IO	MCU_SPI0_D0	-	A15	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_3	-	-
238	P	VPP	6	-	-	-	-	-	-	-	-	-	-	-
239	IO	MCU_SPI0_CS0	-	E11	VDDSHV_MCU	-	-	-	WKUP_TIMER_IO1	-	-	MCU_GPIO0_0	-	-
240	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
241	IO	MCU_SPI0_CS1	-	C11	VDDSHV_MCU	MCU_OBSCLK0	MCU_SYSCLKOUT0	MCU_EXT_REFCLK0	MCU_TIMER_IO1	-	-	MCU_GPIO0_1	-	-
242	IO	MCU_UART0_RTSn	-	D10	+3.3VIO	MCU_TIMER_IO1	-	MCU_SPI1_D1	-	-	-	MCU_GPIO0_8	-	-
243	IO	MCU_SPI0_CLK	-	B13	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_2	-	-
244	IO	MCU_UART0_CTSn	-	B11	+3.3VIO	MCU_TIMER_IO0	-	MCU_SPI1_D0	-	-	-	MCU_GPIO0_7	-	-
245	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
246	IO	MCU_UART0_RXD	-	D8	+3.3VIO	-	-	-	-	-	-	MCU_GPIO0_5	-	-
247	IO	WKUP_I2C0_SCL	-	D13	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_19	-	-
248	IO	MCU_UART0_TXD	-	F8	+3.3VIO	-	-	-	-	-	-	MCU_GPIO0_6	-	-
249	IO	WKUP_I2C0_SDA	-	E13	VDDSHV_MCU	-	-	-	-	-	-	MCU_GPIO0_20	-	-
250	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
251	IO	WKUP_UART0_RXD	-	C9	+3.3VIO	-	MCU_SPI0_CS2	-	-	-	-	MCU_GPIO0_9	-	-

Pin	Type	Signal (Option 0)	Notes	AM62x Pin	Power / Domain	Signal Option 1	Signal Option 2	Signal Option 3	Signal Option 4	Signal Option 5	Signal Option 6	Signal Option 7	Signal Option 8	Signal Option 9
252	IO	MCU_MCAN1_TX	-	D7	+3.3VIO	MCU_TIMER_IO 2	-	MCU_SPI1_CS1	MCU_EXT_REF CLK0	-	-	MCU_GPIO0_15	-	-
253	IO	WKUP_UART0_TXD	-	E9	+3.3VIO	-	MCU_SPI1_CS2	-	-	-	-	MCU_GPIO0_10	-	-
254	IO	MCU_MCAN1_RX	-	B9	+3.3VIO	MCU_TIMER_IO 3	MCU_SPI0_CS2	MCU_SPI1_CS2	MCU_SPI1_CLK	-	-	MCU_GPIO0_16	-	-
255	IO	WKUP_UART0_CTSn	-	C10	+3.3VIO	WKUP_TIMER_I O0	-	MCU_SPI1_CS0	-	-	-	MCU_GPIO0_11	-	-
256	IO	MCU_MCAN0_RX	-	E8	+3.3VIO	MCU_TIMER_IO 0	MCU_SPI1_CS3	-	-	-	-	MCU_GPIO0_14	-	-
257	IO	WKUP_UART0_RTSn	-	C8	+3.3VIO	WKUP_TIMER_I O1	-	MCU_SPI1_CLK	-	-	-	MCU_GPIO0_12	-	-
258	IO	MCU_MCAN0_TX	-	C7	+3.3VIO	WKUP_TIMER_I O0	MCU_SPI0_CS3	-	-	-	-	MCU_GPIO0_13	-	-
259	P	GND	-	-	-	-	-	-	-	-	-	-	-	-
260	P	GND	-	-	-	-	-	-	-	-	-	-	-	-

Note 1: GPMC_AD[0..15] are strapped during power on reset as the BOOTMODE[0..15] pins. GPMC_AD[3..15] must be pulled up or pulled down while the PORz_OUT signal is asserted to VDDSHV3 or GND in order to select the proper boot device and configuration. See the AM62Ax Technical Reference Manual for more information. GPMC_AD0, GPMCA_AD1, and GPMC_AD2 are set to logic 1, 1, 0 (respectively) on the SOM using 10K pullup/pulldown resistors to select a 25 MHz input clock frequency.

Note 2: Please reference Table 2 for information on the maximum current supply of these voltage outputs.

Note 3: PMIC_PBn is tied to pin 25 of the TPS65219 PMIC. It must be pulled to VIN to power on the SOM.

Note 4: USB0_VBUS_DETECT and USB1_VBUS_DETECT are not 5V compliant and should not be connected directly to the VBUS signal of a USB circuit. The voltage must be reduced to be compliant with a 3.3V IO input. See the AM62Ax Technical Reference Manual for more information.

Note 5: VMON_VSYS may be used for an external power supply monitor. It has a valid range of 0 to 1V and the threshold is 0.45V. If it is not used, it should be tied to GND.

Note 6 : VPP should be 1.8V, used for programming AM62Ax Crypto Keys. VPP should only be powered after VDD_1V8 is available and immediately prior to attempts to program the keys using AM62Ax software. Otherwise, tie to GND.

Note 7: LED_RTN should normally be connected to ground and serves as the current return path for the SOM Power Good LED. For power sensitive applications, it should be disconnected to reduce current consumption when the SOM is powered off or sleeping.

Note 8: VD_SEL, VDD_3V3_ENABLE, and VCC_5V0_EN include 4.7K pullup resistors to +3.3V

Note 9: The VCC_5V0_EN pin is connected to PMIC GPO1 as an open drain output (tied to +3.3V) and may be used as a general purpose 3.3V output pin.

ELECTRICAL CHARACTERISTICS

Table 2: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Voltage supply, volt input.		3.2	3.3	3.5	Volts
I_{VIO_1P8}	Max current draw[2]	1.8 volt IO output			1500	mA
$I_{3.3}$	Quiescent Current draw[1]	3.3 volt input	-	TBS	-	mA
$I_{3.3\text{-}max}$	Max current draw[1]	3.3 volt input	-	TBS	TBS	mA
FCPU	CPU internal clock Frequency (PLL output)		200	1250	1400	MHz
FEMIF	GPMC bus frequency		-	133	-	MHz

1. Power utilization of the MitySOM-AM62A is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external LPDDR4 RAM utilization.
2. The MitySOM-AM62A module provides both 1.8V output supplies from the module. These outputs are sequenced from the PMIC and the maximum power output specified should not be exceeded as these supplies also power the module itself.

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 3: Standard Model Numbers

Model	A53 Cores	Max Cortex-A53 Speed	NN Performance	NOR Flash	eMMC	DDR4 RAM	Operating Temp
62A74-TX-XXD-RI	4	1400 MHz[1]	2 TOPS	N/A	N/A	2G	-40C to 85C
62A74-TX-X9D-RC	4	1400 MHz[1]	2 TOPS	N/A	32G	2G	0C to 70C
62A74-TX-XAE-RI	4	1400 MHz[1]	2 TOPS	N/A	64G	4G	-40C to 85C

[1] Initial versions of SOMs using the "T" speed grade processor may be limited to 1250 MHz, for details see the MitySOM-AM62A System on Module (SOM) Revision history and Errata on the Critical Link support site.

MODULE FAMILY MODEL NUMBER GUIDE

If a module suitable for your specific application is not found in Figure 2 please reference the following MitySOM-AM62A model number decoder for configuring a custom module. Please contact Critical Link via info@criticallink.com to determine pricing, lead-time and availability of a custom module.

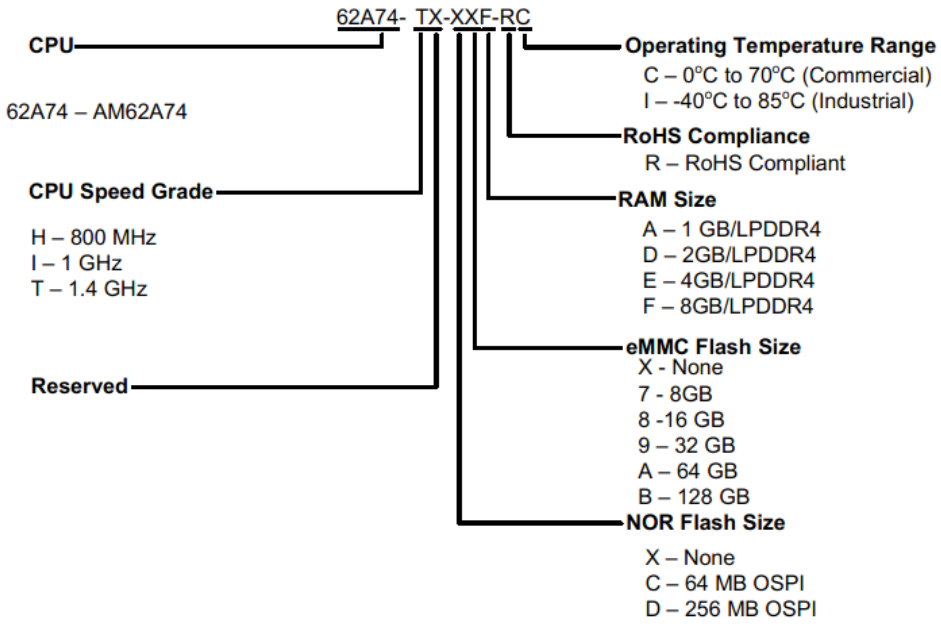

Figure 2 MitySOM-AM62A Model Number Scheme

MECHANICAL INTERFACE

A mechanical outline of the MitySOM-AM62A is illustrated in Figure 3, below. Provisions for an M2 screw have been included for the side of the board away from the DDR4 SO-DIMM edge connector if heavy vibration environments are expected. A full STEP model of the SOM may be downloaded from the Critical Link support site.

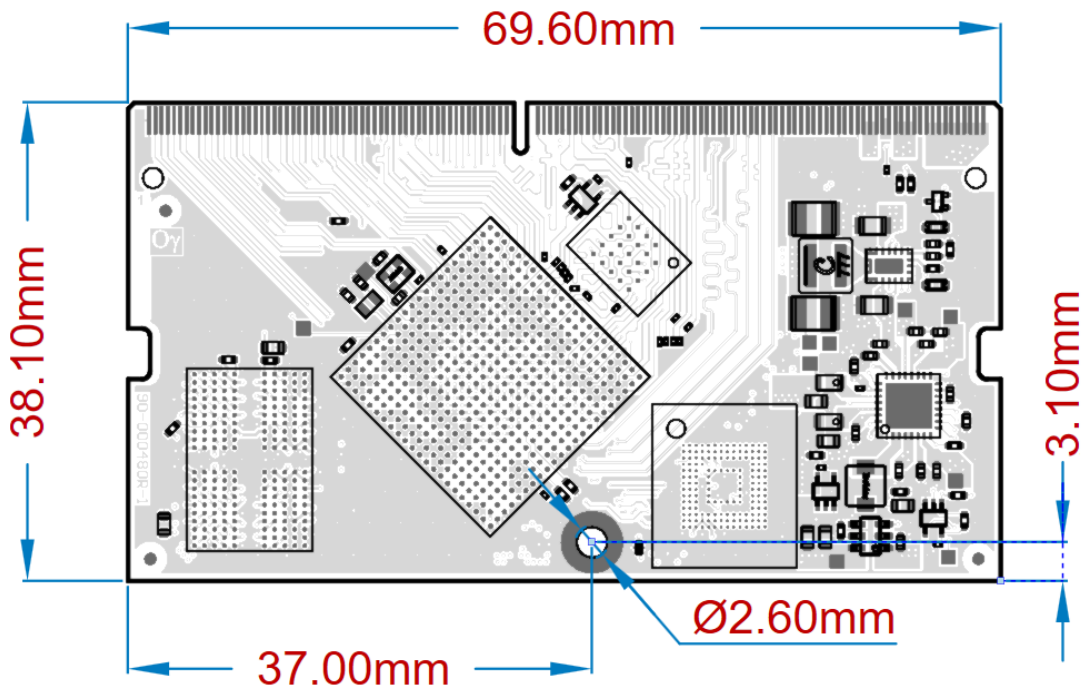

Figure 3 MitySOM-AM62A Mechanical Outline (View From Top)

REVISION HISTORY

Date	Rev	Change Description
10-MAR-2023	1A	Draft Spec
27-NOV-2023	1B	Updated Table 3, Standard Model Numbers
05-APR-2024	2A	Fixed headers. Updated signal names in Table 1 for pins 99, 101 and 103. Updated ball connection in Table 1 for pins 247, 249 and 255.
07-JUN-2024	2B	Corrected pin mux options for pins 99, 101 and 103.
11-OCT-2024	2C	Added note about T speed grade limitations on initial modules under Table 3.