FEATURES

- Altera Cyclone 10 LP – U484 FPGA
  - Up To 80K Logic Elements (LE)
  - 4 Phase Locked Loops (PLLs)
  - Up to 500Mhz Global Clock
  - Up To 2.7Mb Embedded Memory
  - Up To 244 DSP Blocks
  - Up To 6 FPGA PLLs
  - Single Event Upset (SEU) detection

- **Memory**
  - Up To 32MB HyperRAM at 200 MB/sec
  - Up To 32MB QPSI NOR FLASH

- Highly Flexible IO
  - 180 Direct Connect FPGA IO pins
  - 38 True and 28 Emulated LVDS pairs
  - 3 groups of FPGA banks, each providing 64 pins with configurable VCCIO
  - 3 PLL clock output pairs
  - 12 FPGA clock input pins
  - 1.2, 1.8, 2.5, 3.3 LVCMOS, LVDS, various SSTL and HSTL standards supported

- Integrated Power Management
  - Single +5V Input for on-board needs
  - User defined Bank IO Voltage

- JTAG Interface Available on Edge Connector

- **On-Board 50 MHz clock**

- **Mechanical**
  - 260-Pin Card Edge Connector
  - Small 70mm (2.75”) x 30mm (1.2”) size

- **Configuration Status and General-Purpose Tri-Color LEDs**

APPLICATIONS

- Embedded Co-Processor
- Test and Measurement
- Embedded Instrumentation
- Industrial Automation and Control
- Industrial Instrumentation
- System IO expansion
- Motion Control

BENEFITS

- Low Power and Low Cost FPGA Solution
- Rapid Development / Deployment
- Multiple Connectivity and I/O Options
- Support for NIOS II Softcore
  - 30 to 190 DMIPS

DESCRIPTION

The MitySOM-C10L series of highly configurable, small form-factor System-on-Modules (SoM) feature an Altera Cyclone 10 Low Power field programmable gate array (FPGA) and include on-board power supplies, NOR FLASH and a HyperRAM memory subsystems. Using an NIOS II Softcore processor, the MitySOM-C10L provides a complete and flexible CPU infrastructure for a low cost integrated embedded system.

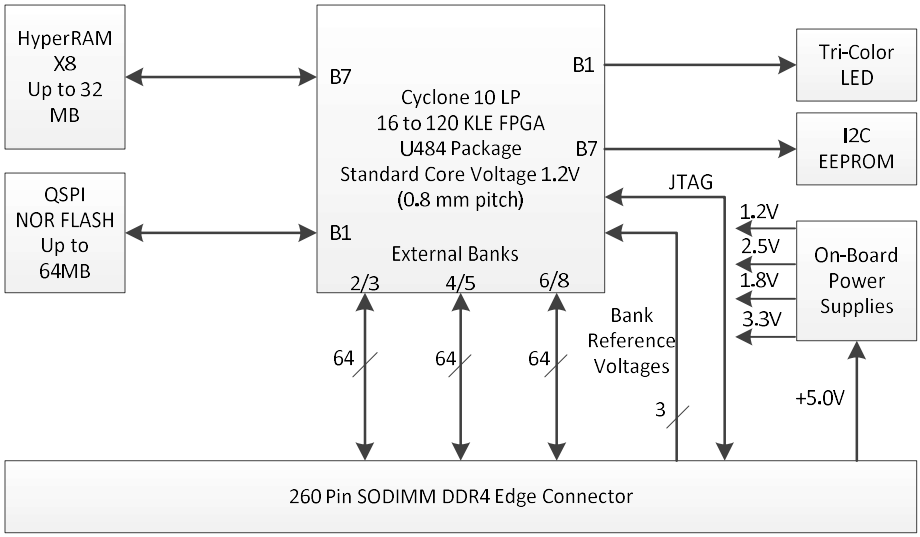


Figure 1 MitySOM-C10L Block Diagram

Figure 1 provides a top-level block diagram of the MitySOM-C10L processor card. As shown in the figure, the interface to the MitySOM-C10L is through a 260-Pin card edge interface. Details of the edge connector interface are included in the Card Edge Interface Description section.

MitySOM-C10L Onboard Storage

HyperRAM Memory

The MitySOM-C10L includes one dedicated 8-bit HyperRAM memory interface. A maximum of 32GB of HyperRAM is supported by standard MitySOM-C10L modules. The HyperRAM interface can be run at up to 200 Mbps.

This HyperRAM memory may be utilized by the standard FPGA fabric or may be integrated with a NIOS II processor subsystem via Avalon high speed interfaces internal to the Cyclone 10 LP.

See Table 8: Standard Model Numbers for additional details.

NOR FLASH

A maximum of 32MB (1 x 32MB) of on-board NOR FLASH memory is connected to the Cyclone 10 LP via the Active Serial (AS) Configuration serial peripheral interface. This is a reliable flash memory that is used as the primary configuration media for the Cyclone 10 LP. The NOR FLASH memory may also be used at runtime for storing NIOS II executable code and/or user non-volatile data. The NOR FLASH write protect signal may be controlled via the Cyclone 10 LP.

I2C EEPROM

An on-board 2 KB I^2C Electrically Erasable Programmable Read-Only Memory (EEPROM) is included on the MitySOM-C10L. The EEPROM includes factory configuration information including assigned serial number, part number, and model number information. The EEPROM write protect signal may be controlled by the Cyclone 10 LP.

MitySOM-C10L Debug Support

The JTAG interface signals for the Cyclone 10 LP FPGA have been brought out to the SODIMM DDR4 card edge connector. This allows customers to decide whether the interface should be exposed on their custom carrier cards. The on-board MitySOM-C10L SPI NOR FLASH, used to hold the FPGA configuration bitstream, may be programmed via the JTAG interface. In addition, the JTAG interface may be used for in-circuit debugging using standard Intel Quartus Signal Tap logic analyzer and probing tools.

General Status LEDs

There are three light emitting diodes (LEDs) on the MitySOM-C10L module. Two of them are on/off status LEDs tied to a specific condition and the other is controlled by FPGA fabric IO pins. The LEDs are identified in Figure 4.

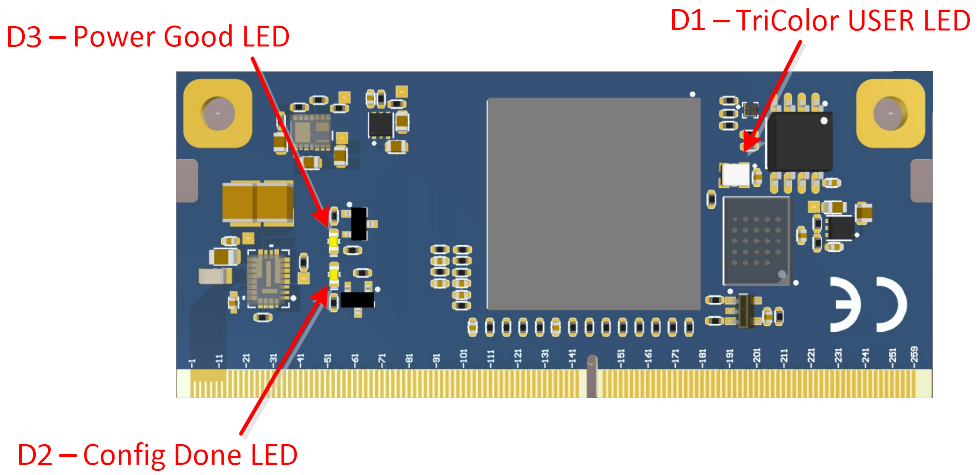


Figure 2 MitySOM-C10L LED positions

Power OK

D3 indicates the MitySOM-5CSx on-module +3.3V and +1.2V switched mode supplies are operating.

Configuration Debug

D2 indicates that FPGA configuration is not complete by lighting a yellow LED. Once the configuration is complete, D2 should turn off.

User Tri-Color LED

The MitySOM-C10L includes a tri-color LED, D3. Each of the RGB LED cathodes is tied directly to an IO pin on the Cyclone 10 LP FPGA. Users may use this LED as they see fit for their application.

External Interface Connections

GPIO

The MitySOM-C10L routes 192 pins of the Cyclone 10 LP FPGA directly to the edge connector interface. The 192 pins are grouped into 3 groups of 64 pins. Each group of pins is associated with 2 FPGA banks; group 1 includes FPGA Banks 2 and 3, group 2 includes FPGA Banks 4 and 5, and group 3 includes FPGA Banks 6 and 8. For each of the groups, a corresponding pair of VCCIO pins are brought to the edge connector to allow setting the IO voltage for the given group. This allows using different IO standards requiring as many as 3 IO voltage levels in a single design.

The MitySOM-C10L FPGA IO mapping has been made with vertical migration in mind. A completed design using the 16 KLE density option will work with the MitySOM-C10L 80 KLE density modules. No adjustments to IO planning should be required.

JTAG

The Cyclone 10 LP JTAG signals (TDI, TDO, TMS, TCK) as well as the 2.5V reference voltage necessary for interfacing to a standard Intel USB Blaster JTAG POD have been routed to the DDR4 edge connector. The TDI and TMS signals are pulled up on board and the TCK signal is pulled down on the SOM in order to support leaving these signals disconnected if desired. The JTAG interface supports programming the Cycle 10 LP bitstream and may be used to program the on-board SPI NOR FLASH using the FPGA as a proxy controller.

Configuration Status / Control

The MitySOM-C10L exposes the CONFIG_DONE signal from the FPGA on pin 24 of the DDR4 edge connector. The CONFIG_DONE signal is low when the FPGA is not configured and +VCCIO_G3 (user supplied input voltage on the DDR4 edge connector) when the FPGA is successfully configured. The signal is pulled up to VCCIO_G3 with a 10K resistor on the SOM.

Also exposed is the nCONFIG signal input on the FPGA, on pin 24. The nCONFIG signal is pulled high to +3.3V on the MitySOM_C10L. The nCONFIG signal may be pulled and held low for at least 0.5 us to reset the FPGA and reset the configuration sequence. See the Intel Cyclone 10 LP Core Fabric and General Purpose I/Os Handbook for more details.

Application Development Support

Users of the MitySOM-C10L are encouraged to develop applications using the MitySOM-C10L development kit provided by Critical Link LLC.

Growth Options

The MitySOM-C10L has been designed to support several upgrade options. These options include a range of speed grades, HyperRAM memory density, SPI NOR FLASH density, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact a Critical Link sales representative.

Absolute Maximum Ratings

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Table 1: Absolute Maximum Ratings

Maximum Supply Voltage (+5VIN)	5.5V
Storage Temperature Range	-55°C to 150°C

Operating Conditions

The following are the minimum temperature ratings for the components that are installed on a MitySOM-C10L. For specifications not contained in this table please contact a Critical Link sales representative. Please see the Thermal Management section below concerning ambient/operating temperature recommendations.

Table 2: Module Component Temperature Ratings (minimum)

Temperature Range	Component Ratings
Commercial (-RC)	0ºC to 70ºC
Industrial (-RI)	-40ºC to 85ºC

Thermal Management

The MitySOM-C10L module requires careful consideration of thermal management. Depending on fabric load, thermal management may be required for operation at elevated temperatures.

Thermal management is a system level issue that must be addressed in conjunction with the overall system design. Some systems may have available airflow with limited space for a heat sink; others may have room for a heat sink with or without the possibility for additional airflow. As a result, the approach taken for thermal management is a design consideration that must be addressed by the overall system designers when integrating the MitySOM-C10L into a product.

Every product is different, and it is advisable to perform thorough testing to ensure that the product will meet desired performance and longevity specifications. We recommend that customers utilize Altera's Early Power Estimator (EPE) for the Cyclone 10 LP. This utility will assist in estimating the potential power usage of the processor for a given application. Details can be found on the PowerPlay EPE page at Intel.com.

Card-Edge Interface Description

The primary interface connector for the MitySOM-C10L is the 260-pin card edge interface which contains 4 types of signals:

- Power (**P**) Input to the module
  - This can be Main Module Power or Bank VCCIO power
- General purpose I/O pins mapped to the Cyclone 10 LP FPGA pins (**IO**)
- Fixed Function Input Pins **(I)**
- Fixed Function Output pins (**O**)

Table 3 contains a summary of the MitySOM-5CSx pin-mapping. For pins connected directly to an FPGA ball, the following FPGA information is also included in the table:

- FPGA Ball Number
- FPGA Bank Number
- FPGA IO Voltage Reference Group; this can vary with FPGA density option
- FPGA IO Optional Function; this can vary with FPGA density option
- Matched Length Group; each bank of FPGA pins includes a group of IO that have the trace lengths matched to +/- 5mil to better support high speed bus IO routing. Lengths between groups are not matched.
- LVDS / differential support; FPGA IO pairs routed to the edge connector are indicated. TRUE pairs represent pins on FPGA ROW I/O banks supporting true LVDS standards. EMULATED pairs represent pins on FPGA COLUMN I/O banks. See the Cyclone 10 LP Fabric User Guide for additional detail. FPGA IO pairs are routed differentially on the MitySOM-C10L.

The MitySOM-C10L does not include differential receiver termination required for LVDS signaling. A configuration option can be made available for installing 100 Ohm termination resistors on the pairs in Bank 2 as indicated by Table 3. Contact Critical Link for more detail. The other banks have relatively short routing distance from the FPGA balls to the edge connectors. If necessary, the LVDS pairs could be terminated at the DDR4 connector on the carrier card. Customers should carefully consider signal integrity of signals using such an arrangement.

Card-Edge Mating Connector

The MitySOM-C10L module mates with a single connector that contains all the power and I/O for the module. The mating socket is a 260-pin SODIMM DDR4 style connector. An example connector is a TE Connectivity AMP Connectors 2309411-1, which is available from distributors such as DigiKey and Mouser. There are several height options for these connectors, the height should be selected based on application requirements.

More information is available in the MitySOM-C10L Carrier Board Design guide from Critical Link.

Table 3: MitySOM-C10L Edge Connector Pin-Out

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
1	+5V	P	-												
2	GND	P	-	-											
3	+5V	P	-												
4	GND	P	-	-											
5	+5V	P	-												
6	GND	P	-	-											
7	+5V	P	-												
8	GND	P	-	-											
9	+5V	P	-												
10	GND	P	-	-											
11	+5V	P	-												
12	GND	P	-	-											
13	+5V	P	-												
14	GND	P	-	-											
15	RESERVED	-	-												No Connect
16	TDI	I	L5	1			1	3	1	2					
17	RESERVED	-	-												No Connect
18	TDO	O	L4	1			1	3	1	2					
19	+2.5V_JTAG	P	-												Output for JTAG connector
20	TCK	I	L1	1			1	3	1	2					
21	POWER_GOOD	O	-												Open Collector output tied to +5V via 10K. High indicates onboard 1.2 and 3.3V supplies are OK.
22	TMS	I	L2	1			1	3	1	2					
23	NCONFIG	I	K5	1			1	3	1	2					10K Pullup to 3.3V
24	CONF_DONE	O	M18	6			1	3	1	2					10K pullup to VCCIO_G3
25	VCCIO_G2	P	Multiple	4, 5											Bank 4 and 5 VCCIO
26	VCCIO_G1	P	Multiple	2, 3											Bank 2 and 3 VCCIO
27	VCCIO_G2	P	Multiple	4, 5											Bank 4 and 5 VCCIO
28	VCCIO_G1	P	Multiple	2, 3											Bank 2 and 3 VCCIO

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
29	GND	P	-												
30	GND	P	-	-											
31	GND	P	-												
32	GND	P	-	-											
33	B2_DIFFCLK1_P	I	T2	2	1	TRUE	0	0	0	0	DIFFCLK_1p	DIFFCLK_1p	DIFFCLK_1p	DIFFCLK_1p	100 Ohm Rx Term Option Available
34	B3_IO_PLL1_CLKOUT_P	IO	AA3	3	4	EMULATED	1	2	1	2	PLL1_CLKOUTp	PLL1_CLKOUTp	PLL1_CLKOUTp	PLL1_CLKOUTp	
35	B2_DIFFCLK1_N	I	T1	2	1	TRUE	0	0	0	0	DIFFCLK_1n	DIFFCLK_1n	DIFFCLK_1n	DIFFCLK_1n	100 Ohm Rx Term Option Available
36	B3_IO_PLL1_CLKOUT_N	IO	AB3	3	4	EMULATED	1	2	1	2	PLL1_CLKOUTn	PLL1_CLKOUTn	PLL1_CLKOUTn	PLL1_CLKOUTn	
37	B2_DIO25_P	IO	Y2	2	1	TRUE	1	2	1	1					100 Ohm Rx Term Option Available
38	B3_DIO8_P	IO	AA4	3	4	EMULATED*	1	2	1	2					Differential Support for 16 KLE Only
39	B2_DIO25_N	IO	Y1	2	1	TRUE	1	2	1	1					100 Ohm Rx Term Option Available
40	B3_DIO8_N	IO	AB4	3	4	EMULATED*	1	2	1	2		VREFB3N2	VREFB3N1	VREFB3N2	Differential Support for 16 KLE Only
41	B2_DIO24_P	IO	W2	2	1	TRUE	1	2	1	1					100 Ohm Rx Term Option Available
42	B3_DIO9_P	IO	AA5	3	4	EMULATED	1	2	1	2					
43	B2_DIO24_N	IO	W1	2	1	TRUE	1	2	1	1					100 Ohm Rx Term Option Available
44	B3_DIO9_N	IO	AB5	3	4	EMULATED	1	2	1	2					
45	B2_DIO21_P	IO	V2	2	1	TRUE	0	1	0	1					100 Ohm Rx Term Option Available
46	B3_DIO10_P	IO	W7	3	4	EMULATED	1	2	1	2					
47	B2_DIO21_N	IO	V1	2	1	TRUE	0	1	1	1					100 Ohm Rx Term Option Available
48	B3_DIO10_N	IO	Y7	3	4	EMULATED	0	2	1	2					
49	GND	-	-	-											
50	GND	P	-	-											
51	B2_DIO20_N	IO	U1	2	1	TRUE	0	1	0	1					100 Ohm Rx Term Option Available
52	B3_DIO12_P	IO	AA7	3	4	EMULATED	0	1	1	1					
53	B2_DIO20_P	IO	U2	2	1	TRUE	0	1	0	1					100 Ohm Rx Term Option Available

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
54	B3_DIO12_N	IO	AB7	3	4	EMULATED	0	1	1	1					
55	B2_DIO18_N	IO	R1	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
56	B3_DIO15_P	IO	AA8	3	4	EMULATED	0	1	0	0					
57	B2_DIO18_P	IO	R2	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
58	B3_DIO15_N	IO	AB8	3	4	EMULATED	0	1	0	0					
59	B2_DIO17_N	IO	P1	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
60	B3_DIO16_P	IO	AA9	3	4	EMULATED	0	1	0	0					
61	B2_DIO17_P	IO	P2	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
62	B3_DIO16_N	IO	AB9	3	4	EMULATED	0	1	0	0	DPCLK3	DPCLK3	DPCLK3	DPCLK3	
63	B2_DIO16_N	IO	N1	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
64	B3_DIO11_P	IO	U9	3	4	EMULATED	0	2	1	2					
65	B2_DIO16_P	IO	N2	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
66	B3_DIO11_N	IO	V8	3	4	EMULATED	0	2	1	2					
67	GND	-	-	-											
68	GND	P	-	-											
69	B2_DIO19_P	IO	P4	2	1	TRUE	0	1	0	1	DPCLK1	DPCLK1	DPCLK1	DPCLK1	100 Ohm Rx Term Option Available
70	B3_DIFFCLK6_P	I	AA11	3	4	EMULATED	0	0	0	0	DIFFCLK_6p	DIFFCLK_6p	DIFFCLK_6p	DIFFCLK_6p	
71	B2_DIO19_N	IO	P3	2	1	TRUE	0	1	0	1					100 Ohm Rx Term Option Available
72	B3_DIFFCLK6_N	I	AB11	3	4	EMULATED	0	0	0	0	DIFFCLK_6n	DIFFCLK_6n	DIFFCLK_6n	DIFFCLK_6n	
73	B2_DIO14_P	IO	M2	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
74	B3_DIO17_P	IO	V11	3	4	EMULATED*	0	0	0	0					Differential Support for 16 KLE Only
75	B2_DIO14_N	IO	M1	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
76	B3_DIO17_N	IO	W10	3	4	EMULATED*	0	0	0	0					Differential Support for 16 KLE Only
77	B2_DIO15_P	IO	M4	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
78	B3_IO29	IO	Y8	3		N/A	0	1	0	1					
79	B2_DIO15_N	IO	M3	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
80	B3_IO12	IO	Y3	3		N/A	1	3	1	2					
81	B2_DIO13_P	IO	L6	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
82	B3_IO16	IO	W6	3		N/A	1	2	1	2					
83	B2_DIO13_N	IO	M6	2	1	TRUE	0	0	0	0					100 Ohm Rx Term Option Available
84	B3_IO6	IO	V5	3		N/A	1	3	1	2					
85	GND	P	-	-											
86	GND	P	-	-											
87	B2_IO15	IO	N5	2		N/A	0	1	0	0					
88	B3_IO13	IO	Y6	3		N/A	1	3	1	2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	
89	B2_IO22_RUP1	IO	V4	2		N/A	1	3	1	2	RUP1	RUP1	RUP1	RUP1	
90	B3_DIO18_P	IO	Y10	3	4	EMULATED*	0	0	0	0					Differential Support for 16 KLE Only
91	B2_IO22_RDN1	IO	V3	2		N/A	1	3	1	2	RDN1	RDN1	RDN1	RDN1	
92	B3_DIO18_N	IO	AA10	3	4	EMULATED*	0	0	0	0					Differential Support for 16 KLE Only
93	B2_IO37	IO	R5	2		N/A	1	3	1	2		VREFB2N3		VREFB2N2	
94	B3_IO44	IO	AB10	3		N/A	0	0	0	0					
95	B2_IO38_CDPCLK1	IO	T4	2		N/A	1	3	1	2	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	
96	B3_IO26	IO	W8	3		N/A	0	2	1	2					
97	B2_IO39	IO	T5	2		N/A	1	3	1	2					
98	B3_IO31	IO	V10	3		N/A	0	1	0	1	DPCLK2	DPCLK2	DPCLK2	DPCLK2	
99	B2_IO22	IO	P5	2		N/A	0	1	1	1		VREFB2N1			
100	B3_IO33	IO	U10	3		N/A	0	1	0	0					
101	B2_IO23	IO	N6	2		N/A	0	1	1	1					
102	B3_IO39	IO	U11	3		N/A	0	0	0	0		VREFB3N0		VREFB3N0	
103	GND	P	-	-											
104	GND	P	-	-											
105	B5_DIO34_N	IO	W20	5	2	TRUE*	1	3	1	2	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	Differential Support for 16 KLE Only

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
106	B4_DIFFCLK7_P	I	AA12	4	5	EMULATED	1	3	1	2	DIFFCLK_7p	DIFFCLK_7p	DIFFCLK_7p	DIFFCLK_7p	
107	B5_DIO34_P	IO	W19	5	2	TRUE*	1	3	1	2		VREFB5N3	VREFB5N1	VREFB5N2	Differential Support for 16 KLE Only
108	B4_DIFFCLK7_N	I	AB12	4	5	EMULATED	1	3	1	2	DIFFCLK_7n	DIFFCLK_7n	DIFFCLK_7n	DIFFCLK_7n	
109	B5_DIO35_N	IO	AA22	5	2	TRUE	1	3	1	2					
110	B4_DIO19_P	IO	AA13	4	5	EMULATED	1	3	1	2					
111	B5_DIO35_P	IO	AA21	5	2	TRUE	1	3	1	2					
112	B4_DIO19_N	IO	AB13	4	5	EMULATED	1	3	1	2					
113	B5_DIO33_N	IO	Y22	5	2	TRUE	1	3	1	2					
114	B4_DIO20_P	IO	AA14	4	5	EMULATED	1	3	1	2					
115	B5_DIO33_P	IO	Y21	5	2	TRUE	1	2	1	2					
116	B4_DIO20_N	IO	AB14	4	5	EMULATED	1	3	1	2					
117	B5_DIO31_N	IO	W22	5	2	TRUE	1	2	1	2					
118	B4_DIO22_P	IO	AA15	4	5	EMULATED	1	3	1	2					
119	B5_DIO31_P	IO	W21	5	2	TRUE	1	2	1	2					
120	B4_DIO22_N	IO	AB15	4	5	EMULATED	1	3	1	2					
121	GND	P	-	-											
122	GND	P	-	-											
123	B5_DIO28_N	IO	V22	5	2	TRUE	1	2	1	1					
124	B4_DIO24_P	IO	AA16	4	5	EMULATED	1	2	1	1					
125	B5_DIO28_P	IO	V21	5	2	TRUE	1	2	1	1					
126	B4_DIO24_N	IO	AB16	4	5	EMULATED	1	2	1	1					
127	B5_DIO27_N	IO	U22	5	2	TRUE	0	2	0	1					
128	B4_DIO21_P	IO	W13	4	5	EMULATED	1	3	1	2					
129	B5_DIO27_P	IO	U21	5	2	TRUE	0	1	0	1					
130	B4_DIO21_N	IO	Y13	4	5	EMULATED	1	3	1	2	DPCLK4	DPCLK4	DPCLK4	DPCLK4	
131	B5_DIFFCLK3_P	I	T21	5	2	TRUE	0	0	0	0	DIFFCLK_3p	DIFFCLK_3p	DIFFCLK_3p	DIFFCLK_3p	
132	B4_DIO29_P	IO	W17	4	5	EMULATED	0	0	0	0					
133	B5_DIFFCLK3_N	I	T22	5	2	TRUE	0	0	0	0	DIFFCLK_3n	DIFFCLK_3n	DIFFCLK_3n	DIFFCLK_3n	
134	B4_DIO29_N	IO	Y17	4	5	EMULATED	0	0	0	0	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	
135	B5_DIO25_N	IO	R22	5	2	TRUE	0	1	0	1					

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
136	B4_DIO30_P	IO	AA20	4	5	EMULATED	0	0	0	0					
137	B5_DIO25_P	IO	R21	5	2	TRUE	0	1	0	1					
138	B4_DIO30_N	IO	AB20	4	5	EMULATED	0	0	0	0					
139	GND	P	-	-											
140	GND	P	-	-											
141	B5_DIO26_N	IO	R18	5	2	TRUE	0	1	0	1					
142	B4_DIO27_P	IO	V15	4	5	EMULATED	0	2	0	1					
143	B5_DIO26_P	IO	R19	5	2	TRUE	0	1	0	1					
144	B4_DIO27_N	IO	W15	4	5	EMULATED	0	1	0	1					
145	GND	P	-	-											
146	GND	P	-	-											
147	B5_DIO32_N	IO	U20	5	2	TRUE	1	2	1	2					
148	B4_DIO31_P	IO	U15	4	5	EMULATED	0	2	0	1					
149	B5_DIO32_P	IO	U19	5	2	TRUE	1	2	1	2					
150	B4_DIO31_N	IO	U14	4	5	EMULATED	0	2	0	1					
151	B5_DIO24_N	IO	P22	5	2	TRUE	0	1	0	0					
152	B4_IO5	IO	V12	4		N/A	1	3	1	2		VREFB4N3	VREFB4N1	VREFB4N2	
153	B5_DIO24_P	IO	P21	5	2	TRUE	0	1	0	0					
154	B4_IO10	IO	U12	4		N/A	1	3	1	2					
155	B5_DIO21_N	IO	N22	5	2	TRUE	0	0	0	0					
156	B4_IO15	IO	V13	4		N/A	1	2	1	1	DPCLK5	DPCLK5	DPCLK5	DPCLK5	
157	B5_DIO21_P	IO	N21	5	2	TRUE	0	0	0	0					
158	B4_IO18	IO	V14	4		N/A	0	2	1	1					
159	GND	P	-	-											
160	GND	P	-	-											
161	B5_DIO20_N	IO	M22	5	2	TRUE	0	0	0	0					
162	B4_IO_PLL4_CLKOUT_P	IO	T16	4	5	EMULATED	0	0	0	0	PLL4_CLKOUTp	PLL4_CLKOUTp	PLL4_CLKOUTp	PLL4_CLKOUTp	
163	B5_DIO20_P	IO	M21	5	2	TRUE	0	0	0	0					
164	B4_IO_PLL4_CLKOUT_N	IO	R16	4	5	EMULATED	0	0	0	0	PLL4_CLKOUTn	PLL4_CLKOUTn	PLL4_CLKOUTn	PLL4_CLKOUTn	
165	B5_DIO23_N	IO	N20	5	2	TRUE	0	1	0	0					

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
166	B4_IO36	IO	R14	4		N/A	0	0	0	0					
167	B5_DIO23_P	IO	N19	5	2	TRUE	0	1	0	0				VREFB5N0	
168	B4_IO22	IO	T15	4		N/A	0	1	0	1					
169	B5_DIO19_N	IO	M20	5	2	TRUE	0	0	0	0					
170	B4_IO23	IO	AB18	4		N/A	0	1	0	1					
171	B5_DIO19_P	IO	M19	5	2	TRUE	0	0	0	0					
172	B4_IO24	IO	AA18	4		N/A	0	1	0	1		VREFB4N1	VREFB4N0	VREFB4N1	
173	B5_IO37	IO	N18	5		N/A	0	0	0	0	DPCLK6	DPCLK6	DPCLK6	DPCLK6	
174	B5_IO5_RDN3	IO	T18	5		N/A	1	3	1	2	RDN3	RDN3	RDN3	RDN3	50 Ohm in series to FPGA ball. Connect to GND to support Ext. OCT.
175	B5_IO23	IO	R20	5		N/A	1	2	1	1					
176	B5_IO44	IO	M16	5		N/A	0	0	0	0		VREFB5N0			
177	GND	P	-	-											
178	GND	P	-	-											
179	B6_IO6_VREFB6N1	IO	K19	6		N/A	1	3	1	2	VREFB6N1	VREFB6N3	VREFB6N1	VREFB6N2	
180	B8_IO_PLL3_CLKOUT_P	IO	E5	8	6	EMULATED	1	3	1	2	PLL3_CLKOUTp	PLL3_CLKOUTp	PLL3_CLKOUTp	PLL3_CLKOUTp	
181	B6_IO25_VREFB6N0	IO	H18	6		N/A	0	1	0	1	VREFB6N0	VREFB6N1	VREFB6N0	VREFB6N1	
182	B8_IO_PLL3_CLKOUT_N	IO	E6	8	6	EMULATED	1	3	1	2	PLL3_CLKOUTn	PLL3_CLKOUTn	PLL3_CLKOUTn	PLL3_CLKOUTn	
183	B6_IO8	IO	J18	6		N/A	1	2	1	2		VREFB6N2			
184	B8_IO30	IO	F8	8		N/A	1	3	1	1					
185	B6_IO40	IO	F17	6		N/A	0	0	0	0					
186	B8_IO27	IO	C6	8		N/A	1	2	1	1					
187	B6_DIO17_P	IO	L21	6	3	TRUE	1	3	1	2					
188	B8_IO24	IO	B5	8		N/A	1	2	1	1		VREFB8N2	VREFB8N1	VREFB8N1	
189	B6_DIO17_N	IO	L22	6	3	TRUE	1	3	1	2					
190	B8_IO23	IO	A5	8		N/A	0	2	1	1					
191	B6_DIO16_P	IO	K21	6	3	TRUE	1	3	1	2					
192	B8_DIO8	IO	C10	8		N/A	0	0	0	0		VREFB8N0	VREFB8N0	VREFB8N0	
193	B6_DIO16_N	IO	K22	6	3	TRUE	1	3	1	2					
194	B8_IO2	IO	D10	8		N/A	0	0	0	0					

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
195	GND	P	-	-											
196	GND	P	-	-											
197	B6_DIFFCLK2_N	I	G22	6	3	TRUE	1	3	1	2	DIFFCLK_2n	DIFFCLK_2n	DIFFCLK_2n	DIFFCLK_2n	
198	B8_DIFFCLK4_P	I	B11	8	6	EMULATED	0	0	0	0	DIFFCLK_4p	DIFFCLK_4p	DIFFCLK_4p	DIFFCLK_4p	
199	B6_DIFFCLK2_P	I	G21	6	3	TRUE	1	3	1	2	DIFFCLK_2p	DIFFCLK_2p	DIFFCLK_2p	DIFFCLK_2p	
200	B8_DIFFCLK4_N	I	A11	8	6	EMULATED	0	0	0	0	DIFFCLK_4n	DIFFCLK_4n	DIFFCLK_4n	DIFFCLK_4n	
201	B6_DIO15_P	IO	J21	6	3	TRUE	1	3	1	2					
202	B8_DIO6_P	IO	F10	8	6	EMULATED*	1	2	1	1					Differential Support for 16 KLE Only
203	B6_DIO15_N	IO	J22	6	3	TRUE	1	3	1	2	DPCLK7	DPCLK7	DPCLK7	DPCLK7	
204	B8_DIO6_N	IO	F9	8	6	EMULATED*	1	3	1	2					Differential Support for 16 KLE Only
205	B6_DIO13_P	IO	H21	6	3	TRUE	1	2	1	2					
206	B8_DIO14_P	IO	B10	8	6	EMULATED	0	0	0	0					
207	B6_DIO13_N	IO	H22	6	3	TRUE	1	3	1	2					
208	B8_DIO14_N	IO	A10	8	6	EMULATED	0	0	0	0					
209	B6_DIO11_P	IO	F21	6	3	TRUE	0	2	1	1					
210	B8_DIO13_P	IO	B9	8	6	EMULATED	0	0	0	0	DPCLK10	DPCLK10	DPCLK10	DPCLK10	
211	B6_DIO11_N	IO	F22	6	3	TRUE	1	2	1	1					
212	B8_DIO13_N	IO	A9	8	6	EMULATED	0	0	0	0					
213	GND	P	-	-											
214	GND	P	-	-											
215	B6_DIO9_P	IO	E21	6	3	TRUE	0	1	0	1					
216	B8_DIO12_P	IO	B8	8	6	EMULATED	0	1	0	0					
217	B6_DIO9_N	IO	E22	6	3	TRUE	0	1	0	1					
218	B8_DIO12_N	IO	A8	8	6	EMULATED	0	0	0	0					
219	B6_DIO7_P	IO	D21	6	3	TRUE	0	1	0	1					
220	B8_DIO9_P	IO	C7	8	6	EMULATED	0	1	0	1					
221	B6_DIO7_N	IO	D22	6	3	TRUE	0	1	0	1					
222	B8_DIO9_N	IO	C8	8	6	EMULATED	0	1	0	1	DPCLK11	DPCLK11	DPCLK11	DPCLK11	
223	B6_DIO4_P	IO	C21	6	3	TRUE	0	0	0	0					

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
224	B8_DIO11_P	IO	B7	8	6	EMULATED	0	1	0	0					
225	B6_DIO4_N	IO	C22	6	3	TRUE	0	1	0	0					
226	B8_DIO11_N	IO	A7	8	6	EMULATED	0	1	0	0					
227	B6_DIO3_P	IO	B21	6	3	TRUE	0	0	0	0					
228	B8_DIO10_P	IO	B6	8	6	EMULATED	0	1	0	0					
229	B6_DIO3_N	IO	B22	6	3	TRUE	0	0	0	0					
230	B8_DIO10_N	IO	A6	8	6	EMULATED	0	1	0	0					
231	GND	P	-	-											
232	GND	P	-	-											
233	B6_DIO2_P	IO	D20	6	3	TRUE	0	0	0	0		VREFB6N0		VREFB6N0	
234	B8_DIO1_P	IO	G7	8	6	EMULATED	1	3	1	2					
235	B6_DIO2_N	IO	C20	6	3	TRUE	0	0	0	0	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	
236	B8_DIO1_N	IO	F7	8	6	EMULATED	1	3	1	2					
237	B6_DIO6_P	IO	F19	6	3	TRUE	0	1	0	1					
238	B8_DIO5_P	IO	B4	8	6	EMULATED	1	3	1	1					
239	B6_DIO6_N	IO	F20	6	3	TRUE	0	1	0	1					
240	B8_DIO5_N	IO	A4	8	6	EMULATED	1	2	1	1					
241	B6_DIO10_P	IO	H19	6	3	TRUE	0	1	0	1					
242	B8_DIO3_P	IO	B3	8	6	EMULATED	1	3	1	2					
243	B6_DIO10_N	IO	H20	6	3	TRUE	0	1	0	1					
244	B8_DIO3_N	IO	A3	8	6	EMULATED	1	3	1	1					
245	B6_DIO5_P	IO	H17	6	3	TRUE	0	1	0	1					
246	B8_DIO2_P	IO	C4	8	6	EMULATED	1	3	1	2	CDPCLK7	CDPCLK7	CDPCLK7	CDPCLK7	
247	B6_DIO5_N	IO	G18	6	3	TRUE	0	1	0	1					
248	B8_DIO2_N	IO	C3	8	6	EMULATED	1	3	1	2					
249	GND	P	-	-											
250	GND	P	-	-											
251	GND	P	-	-											
252	GND	P	-	-											
253	RESERVED	-	-	-											No Connect

Pin	Net Name	Type	FPGA Ball	FPGA Bank	ML Group	LVDS?	Bank VREF Group				Optional Function				Notes
							16 KLE	40 KLE	55 KLE	80 KLE	16 KLE	40 KLE	55 KLE	80 KLE	
254	VCCIO_G3	P	Multiple	6, 8											
255	RESERVED	-	-	-											No Connect
256	VCCIO_G3	P	Multiple	6, 8											
257	RESERVED	-	-	-											No Connect
258	RESERVED	-	-	-											
259	RESERVED	-	-	-											No Connect
260	RESERVED	-	-	-											

The on-board FPGA connections to the tri-color USER LED, the SPI NOR FLASH, the HyperBus RAM, and the I2C EEPROM are listed in Table 4.

Table 4 MitySOM-C10L Internal FPGA functional connections

FPGA Ball	Bank	Connection	IO Voltage
B2	1	Tri-Color LED Red Cathode	3.3 V
B1	1	Tri-Color LED Green Cathode	3.3 V
D2	1	Tri-Color LED Blue Cathode	3.3 V
D1	1	SPI NOR Serial Out Data	3.3 V
E2	1	SPI NOR Chip Select (active low)	3.3 V
E1	1	SPI NOR Write Protect (active low)	3.3 V
K1	1	SPI NOR Serial In Data	3.3 V
K2	1	SPI NOR Clock	3.3 V
E16	7	HyperBus Chip Select (active low)	1.8 V
A20	7	HyperBus Clock N	1.8 V
B20	7	HyperBus Clock P	1.8 V
E15	7	HyperBus Reset (active low)	1.8 V
A18	7	HyperBus DQ0	1.8 V
A16	7	HyperBus DQ1	1.8 V
B18	7	HyperBus DQ2	1.8 V
B17	7	HyperBus DQ3	1.8 V
A17	7	HyperBus DQ4	1.8 V
B16	7	HyperBus DQ5	1.8 V
A15	7	HyperBus DQ6	1.8 V
B15	7	HyperBus DQ7	1.8 V
E14	7	HyperBus RWDS	1.8 V
F15	7	Factory I2C EEPROM Write Protect	1.8 V
C19	7	I2C EEPROM SDL (2.2 K pullup)	1.8 V
D19	7	I2C EEPROM SCA (2.2 K pullup)	1.8 V

In order to provide as much flexibility on FPGA IO Standard utilization as possible, the Voltage Reference and On-Chip Termination (OCT) calibration pins not brought to the DDR4 edge connector have been connected on the MitySOM-C10L according to Table 5. If these pins are not required for a given design, they must be configured as Tri-State (High Impedance) input pins in the configuration bitstream.

Table 5 MitySOM-C10L FPGA Internal Connections for various VREF and OCT Calibration pins

FPGA Ball	Bank	Connection	16 KLE	40 KLE	55 KLE	80 KLE
M5	2	VCCIO_G1 * 0.5 Volts	VREFB2N0	VREFB2N0	VREFB2N0	VREFB2N0
T3	2	VCCIO_G1 * 0.5 Volts	VREFB2N1	VREFB2N2	VREFB2N1	VREFB2N1
Y4	3	VCCIO_G1 * 0.5 Volts	VREFB3N1	VREFB3N3		
V9	3	VCCIO_G1 * 0.5 Volts	VREFB3N0	VREFB3N1	VREFB3N0	VREFB3N1
W14	4	VCCIO_G2 * 0.5 Volts	VREFB4N1	VREFB4N2		
V16	4	VCCIO_G2 * 0.5 Volts	VREFB4N0	VREFB4N0		VREFB4N0

FPGA Ball	Bank	Connection	16 KLE	40 KLE	55 KLE	80 KLE
R17	5	VCCIO_G2 * 0.5 Volts	VREFB5N1	VREFB5N2		
P20	5	VCCIO_G2 * 0.5 Volts	VREFB5N0	VREFB5N1	VREFB5N0	VREFB5N1
D17	7	0.9V	VREFB7N0	VREFB7N0	VREFB7N0	VREFB7N0
C15	7	0.9V	VREFB7N1	VREFB7N2	VREFB7N1	VREFB7N1
E9	8	VCCIO_G3 * 0.5 Volts	VREFB8N0	VREFB8N1		
D6	8	VCCIO_G3 * 0.5 Volts	VREFB8N1	VREFB8N3		VREFB8N2
AA19	4	50 Ohm Pullup to VCCIO_G2	RUP2	RUP2	RUP2	RUP2
AB19	4	50 Ohm Pulldown to GND	RDN2	RDN2	RDN2	RDN2
T17	5	50 Ohm Pullup to VCCIO_G2	RUP3	RUP3	RUP3	RUP3
B19	7	50 Ohm Pullup to 1.8V	RUP4	RUP4	RUP4	RUP4
A19	7	50 Ohm Pulldown to GND	RDN4	RDN4	RDN4	RDN4

In order to support various FPGA density options, several FPGA IO pins have been connected to the FPGA VCCINT (1.2V) domain or to ground. These pins are identified in Table 6. These pins must be configured as Tri-Stated Inputs (high impedance) in bitstreams targeting FPGA density options that support using the pins as IO.

Table 6 Reserved IO Pins that should be configured as Tri-State Inputs

FPGA Ball	Bank	Connection	16 KLE Option	40 KLE Option	55 KLE Option	80 KLE Option
L8	1	GND	IO	IO	GND	GND
K8	1	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
J7	1	1.2V / VCCINT	IO	IO	IO	VCCINT
K7	1	GND	IO	IO	IO	GND
L7	2	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
M7	2	GND	IO	IO	GND	GND
M8	2	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
N8	2	GND	IO	IO	GND	GND
N7	2	1.2V / VCCINT	IO	IO	IO	VCCINT
P7	2	1.2V / VCCINT	IO	IO	IO	VCCINT
P6	2	GND	IO	IO	IO	GND
R6	2	1.2V / VCCINT	IO	IO	IO	VCCINT
R7	2	GND	IO	IO	GND	GND
T7	2	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
P8	2	GND	IO	GND	GND	GND
R8	2	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
R9	3	GND	IO	GND	GND	GND
T8	3	GND	IO	IO	GND	GND
R10	3	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
T9	3	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
V6	3	GND	IO	IO	IO	GND
U7	3	GND	IO	IO	IO	GND
U8	3	1.2V / VCCINT	IO	IO	IO	VCCINT
R11	3	GND	IO	GND	GND	GND

FPGA Ball	Bank	Connection	16 KLE Option	40 KLE Option	55 KLE Option	80 KLE Option
R12	3	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
V7	3	1.2V / VCCINT	IO	IO	IO	VCCINT
T10	3	GND	IO	IO	IO	GND
T11	3	1.2V / VCCINT	IO	IO	IO	VCCINT
T12	4	GND	IO	IO	GND	GND
R13	4	GND	IO	GND	GND	GND
U13	4	GND	IO	IO	IO	GND
T14	4	GND	IO	IO	IO	GND
R15	4	1.2V / VCCINT	IO	IO	IO	VCCINT
P14	5	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
N14	5	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
P15	5	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
P16	5	GND	IO	IO	GND	GND
M15	5	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
N15	5	GND	IO	GND	GND	GND
P17	5	1.2V / VCCINT	IO	IO	IO	VCCINT
N16	5	1.2V / VCCINT	IO	IO	IO	VCCINT
N17	5	GND	IO	IO	IO	GND
L16	6	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
L15	6	GND	IO	GND	GND	GND
K15	6	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
J15	6	GND	IO	GND	GND	GND
J16	6	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
K16	6	GND	IO	GND	GND	GND
K17	6	1.2V / VCCINT	IO	IO	IO	VCCINT
J17	6	1.2V / VCCINT	IO	IO	IO	VCCINT
H16	6	GND	IO	IO	IO	GND
G17	6	GND	IO	IO	IO	GND
F16	7	GND	IO	IO	IO	GND
G16	7	1.2V / VCCINT	IO	IO	IO	VCCINT
G15	7	GND	IO	IO	IO	GND
H15	7	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
H14	7	GND	IO	IO	GND	GND
G13	7	GND	IO	IO	IO	GND
F12	7	GND	IO	GND	GND	GND
H13	7	GND	IO	GND	GND	GND
H12	7	GND	IO	GND	GND	GND
G12	7	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT
H11	8	1.2V / VCCINT	IO	IO	VCCINT	VCCINT
E10	8	GND	IO	IO	IO	GND
G11	8	GND	IO	IO	IO	GND
G10	8	1.2V / VCCINT	IO	IO	IO	VCCINT
G9	8	GND	IO	IO	IO	GND
H10	8	GND	IO	IO	GND	GND
H9	8	1.2V / VCCINT	IO	VCCINT	VCCINT	VCCINT

FPGA Ball	Bank	Connection	16 KLE Option	40 KLE Option	55 KLE Option	80 KLE Option
G8	8	1.2V / VCCINT	IO	IO	IO	VCCINT

ELECTRICAL CHARACTERISTICS

Table 7 lists the Power Supply Input voltage levels and current consumption. The current consumption of the FPGA portion of the SOM is highly dependent on the application. Users are strongly encouraged to examine the Power Estimate provide by the Intel FPGA design suite (Quartus Prime).

Table 7: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Voltage supply, volt input.		4.8	5.0	5.15	Volts
$I_{5.0}$	Quiescent Current draw	5.0 volt input		TBS		mA
$I_{5.0\text{-}max}$	Max current draw	5.0 volt input		TBS	3000	mA
VCCIO_XX	Fpga VCCIO Supply, Group 1, 2, or 3		1.2	1.8/2.5/3.3	3.4	Volts
I_{VCCIO}	Quiescent Current draw			TBS		mA
$I_{VCCIO\text{-}max}$	Max current draw			TBS	750	mA
	1. Power utilization of the MitySOM-C10L is heavily dependent on end-user application.					

ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these configurations please contact your Critical Link representative or visit one of our authorized distributors.

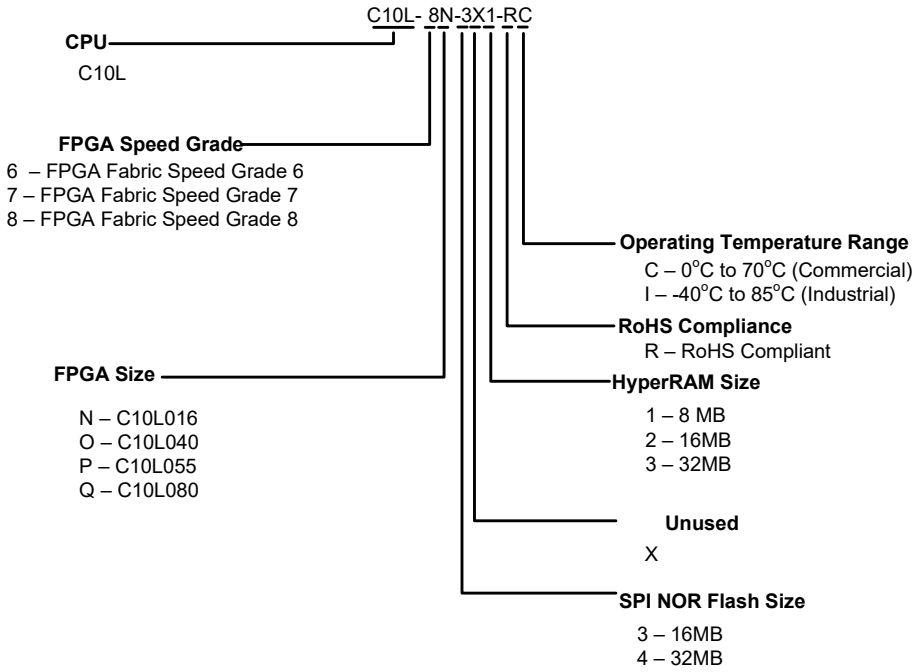
Table 8: Standard Model Numbers

Model	Speed Grade	Hyper RAM	FPGA KLE	NOR	Temperature Ratings
C10L-7N-3XX-RI	7	N/A	16	16MB	-40ºC to 85º C
C10L-7Q-3X3-RI	7	32 MB	80	16MB	-40ºC to 85º C

MitySOM-C10L Module Family Model Number Guide

If you a module suitable for your specific application is not found in Table 8 please reference the following MitySOM-C10L model number decoder for configuring a custom module. Please contact your Critical Link representative to determine pricing, lead-time and availability of a custom module.

Figure 3 MitySOM-C10L Model Number Decoder



MECHANICAL INTERFACE

A mechanical outline of the MitySOM-C10L is illustrated in Figure 4, below.

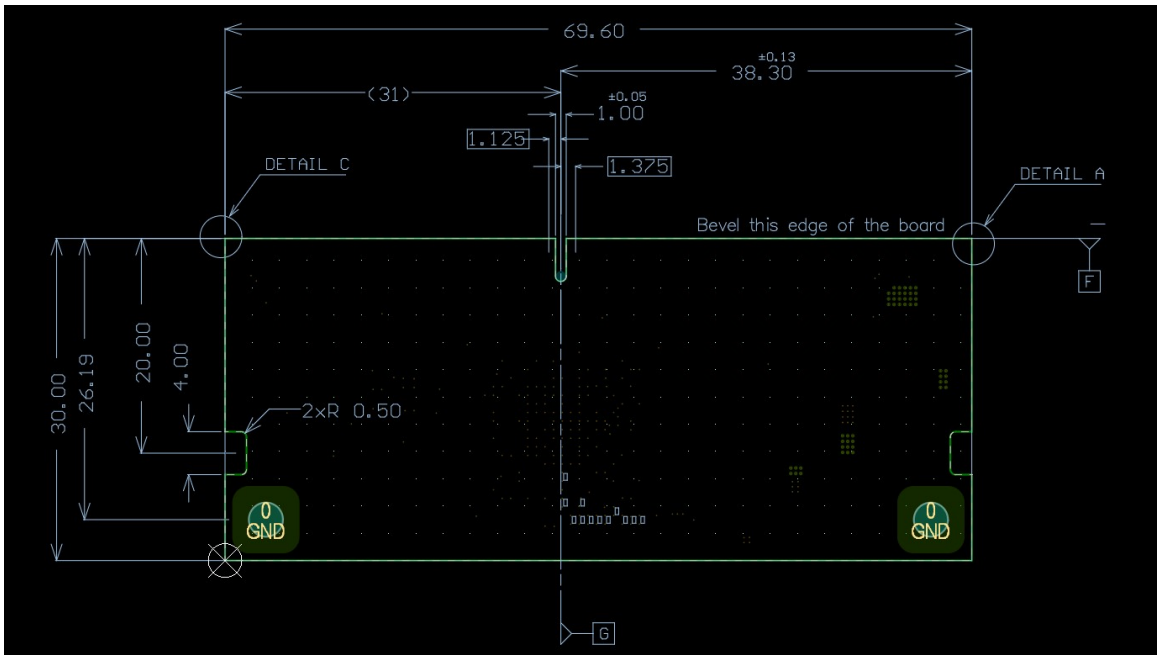


Figure 4 MitySOM-C10L Mechanical Outline

REVISION HISTORY

Date	Revision	Change Description
08-FEB-2022	A	Initial Revision
06-JAN-2023	B	Updated Table 8, Standard Model Numbers