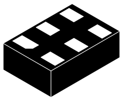
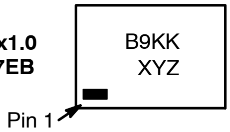
TinyLogic UHS 2-Input Non-Inverting Multiplexer

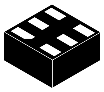
NC7SZ157

MARKING DIAGRAMS

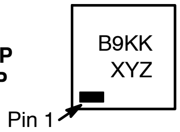


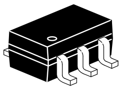
SIP6 1.45x1.0
CASE 127EB



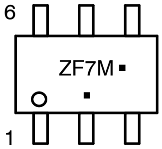


UDFN6
1.0X1.0, 0.35P
CASE 517DP





SC−88
CASE 419B−02



B9, ZF7 = Specific Device Code
KK = 2−Digit Lot Run Traceability Code
XY = 2−Digit Date Code Format
Z = Assembly Plant Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

Description

The NC7SZ157 is a single, high performance, 2−to−1 CMOS non−inverting multiplexer from **onsemi**'s Ultra−High Speed series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} operating range. The inputs and outputs are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating range.

Features

- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Ultra High−Speed
- Power Down High−Impedance Inputs / Outputs
- Over−Voltage Tolerance Inputs Facilitate 5 V to 3 V Translation
- Proprietary Noise / EMI Reduction Circuitry
- Ultra−Small MicroPak™ Packages
- Space−Saving SC−88 Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

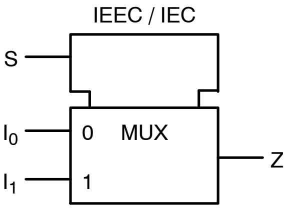


Figure 1. Logic Symbol

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

August, 2024 − Rev. 7

Pin Configurations

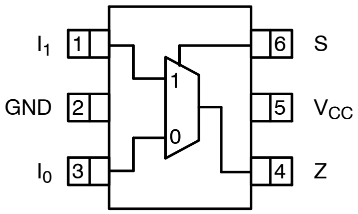


Figure 2. SC−88 (Top View)

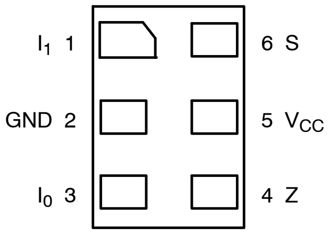
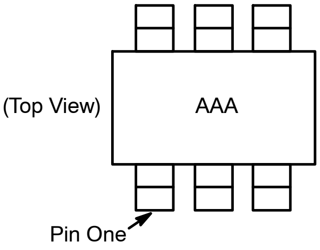


Figure 3. MicroPak (Top Through View)



NOTES:

1. AAA represents product code top mark (*see Ordering Information*).
2. Orientation of top mark determines pin one location.
3. Reading the top mark left to right, pin one is the lower left pin.

Figure 4. Pin 1 Orientation

PIN DEFINITIONS

Pin # SC−88	Pin # MicroPak	Name	Description
1	1	I_1	Data Input
2	2	GND	Ground
3	3	I_0	Data Input
4	4	Z	Output
5	5	V_{CC}	Supply Voltage
6	6	S	Control Input

FUNCTION TABLE

Inputs			Output
S	**I_1**	**I_0**	**$Z = (I_0) \cdot (\overline{S}) + (I_1) \cdot (S)$**
L	X	L	L
L	X	H	H
H	L	X	L
H	H	X	H

H = HIGH Logic Level
L = LOW Logic Level
X = Don’t Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	$V_{IN} < 0$ V	–	−50	mA
I_{OK}	DC Output Diode Current	$V_{OUT} < 0$ V	–	−50	mA
I_{OUT}	DC Output Current		–	±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		–	±50	mA
T_{STG}	Storage Temperature Range		−65	+150	°C
T_J	Junction Temperature Under Bias		–	+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		–	+260	°C
P_D	Power Dissipation in Still Air	SC−88	–	332	mW
		MicroPak−6	–	812	
		MicroPak2™−6	–	812	
ESD	Human Body Model, JEDEC: JESD22−A114		–	4000	V
	Charge Device Model, JEDEC: JESD22−C101		–	2000	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.50	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Times	V_{CC} at 1.8 V ±0.15 V, 2.5 V ±0.2 V	0	20	ns/V
		V_{CC} at 3.3 V ±0.3 V	0	10	
		V_{CC} at 5.0 V ±0.5 V	0	5	
θ_{JA}	Thermal Resistance	SC−88	–	377	°C/W
		MicroPak−6	–	154	
		MicroPak2−6	–	154	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

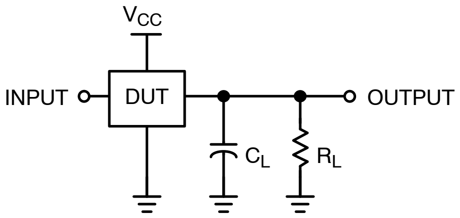
DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = −40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95			0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
		2.30 to 5.50			0.70 V_{CC}	–	–	0.70 V_{CC}	–	
V_{IL}	LOW Level Input Voltage	1.65 to 1.95			–	–	0.35 V_{CC}	–	0.35 V_{CC}	V
		2.30 to 5.50			–	–	0.30 V_{CC}	–	0.30 V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	$V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = −100 μA	1.55	1.65	–	1.55	–	V
		2.30			2.20	2.30	–	2.20	–	
		3.00			2.90	3.00	–	2.90	–	
		4.50			4.40	4.50	–	4.40	–	
		1.65		I_{OH} = −4 mA	1.29	1.52	–	1.29	–	
		2.30		I_{OH} = −8 mA	1.90	2.15	–	1.90	–	
		3.00		I_{OH} = −16 mA	2.40	2.80	–	2.40	–	
		3.00		I_{OH} = −24 mA	2.30	3.68	–	2.30	–	
		4.50		I_{OH} = −32 mA	3.90	4.20	–	3.80	–	
V_{OL}	LOW Level Output Voltage	1.65	$V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 100 μA	–	0	0.10	–	0.10	V
		2.30			–	0	0.10	–	0.10	
		3.00			–	0	0.10	–	0.10	
		4.50			–	0	0.10	–	0.10	
		1.65		I_{OL} = 4 mA	–	0.08	0.24	–	0.24	
		2.30		I_{OL} = 8 mA	–	0.10	0.30	–	0.30	
		3.00		I_{OL} = 16 mA	–	0.15	0.40	–	0.40	
		3.00		I_{OL} = 24 mA	–	0.22	0.55	–	0.55	
		4.50		I_{OL} = 32 mA	–	0.22	0.55	–	0.55	
I_{IN}	Input Leakage Current	1.65 to 5.5		V_{IN} = 5.5 V, GND	–	–	±0.1	–	±1	μA
I_{OFF}	Power Off Leakage Current	0		V_{IN} or V_{OUT} = 5.5 V	–	–	1.0	–	10	μA
I_{CC}	Quiescent Supply Current	1.65 to 5.50		V_{IN} = 5.5 V, GND	–	–	1.0	–	10	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay S to Z (Figure 5, 6)	1.80 ±0.15	C_L = 15 pF, R_L = 1 MΩ,	–	6.0	11.5	–	12.0	ns
		2.50 ±0.20		–	3.5	6.1	–	6.5	
		3.30 ±0.30		–	2.6	4.1	–	4.5	
		5.00 ±0.50		–	1.9	3.2	–	3.5	
	Propagation Delay I_n to Z (Figure 5, 6)	1.80 ±0.15	C_L = 15 pF, R_L = 1MΩ,	–	5.9	10.0	–	10.5	
		5.00 ±0.50		–	3.5	5.8	–	6.1	
		3.30 ±0.30		–	2.6	3.9	–	4.2	
		5.00 ±0.50		–	1.9	3.1	–	3.3	
	Propagation Delay S to Z (Figure 5, 6)	3.30 ±0.30	C_L = 50 pF, R_L = 500 Ω,	–	3.2	4.8	–	5.2	
		5.00 ±0.50		–	2.4	3.8	–	4.1	
	Propagation Delay I_n to Z (Figure 5, 6)	3.30 ±0.30	C_L = 50 pF, R_L = 500 Ω,	–	3.2	4.6	–	5.0	
		5.00 ±0.50		–	2.4	3.7	–	4.0	
C_{IN}	Input Capacitance	0.00		–	2	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Note 4) (Figure 7)	3.30		–	14	–	–	–	pF
		5.00		–	17	–	–	–	

4. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}\text{static})$.



NOTE:
5. C_L includes load and stray capacitance; inputs PRR = 1.0 MHz, t_W = 500 ns.

Figure 5. AC Test Circuit

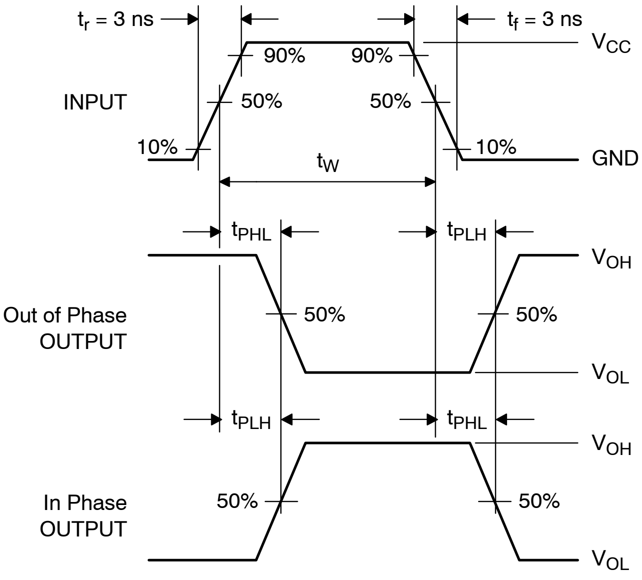
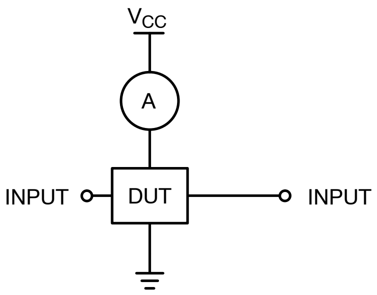


Figure 6. AC Waveforms



NOTE:
6. Input = AC Waveform; PRR = Variable; Duty Cycle = 50%.

Figure 7. I_{CCD} Test Circuit

DEVICE ORDERING INFORMATION

Device	Top Mark	Packages	Shipping†
NC7SZ157P6X	ZF7	6−Lead SC70, EIAJ SC−88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ157L6X	B9	6−Lead MicroPak, 1.00 mm Wide	5000 / Tape & Reel
NC7SZ157FHX	B9	6−Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch	5000 / Tape & Reel

DISCONTINUED (Note 7)

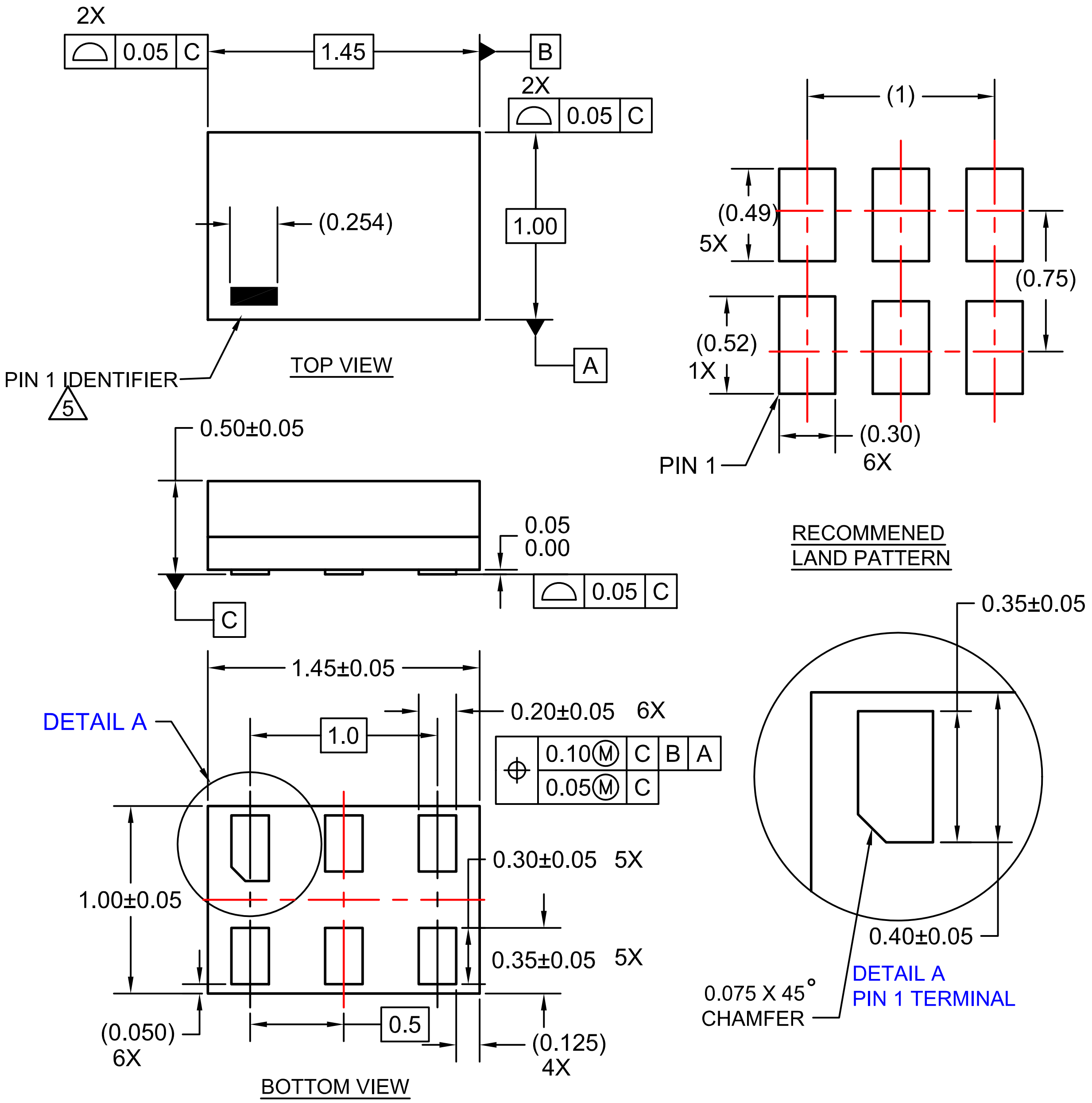
NC7SZ157P6X−L22347	ZF7	6−Lead SC70, EIAJ SC−88, 1.25 mm Wide	3000 / Tape & Reel
NC7SZ157L6X−L22175	B9	6−Lead MicroPak, 1.00 mm Wide	5000 / Tape & Reel
NC7SZ157FHX−L22175	B9	6−Lead, MicroPak2, 1x1 mm Body, .35 mm Pitch	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

SIP6 1.45X1.0
CASE 127EB
ISSUE O

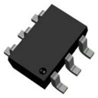
DATE 31 AUG 2016



NOTES:

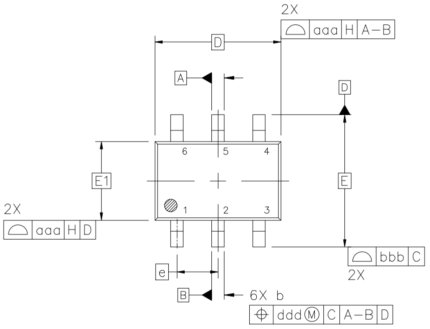
1. CONFORMS TO JEDEC STANDARD MO-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-2009
4. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

DOCUMENT NUMBER:	**98AON13590G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SIP6 1.45X1.0**	**PAGE 1 OF 1**



SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

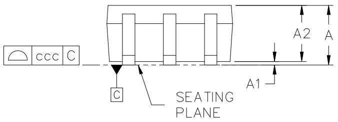
DATE 18 APR 2024



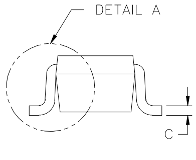
TOP VIEW

NOTES:

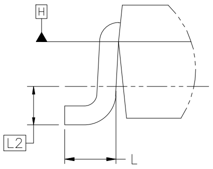
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.



SIDE VIEW

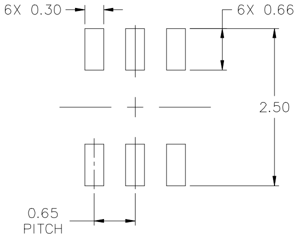


END VIEW



DETAIL A
SCALE 2:1

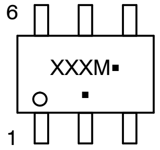
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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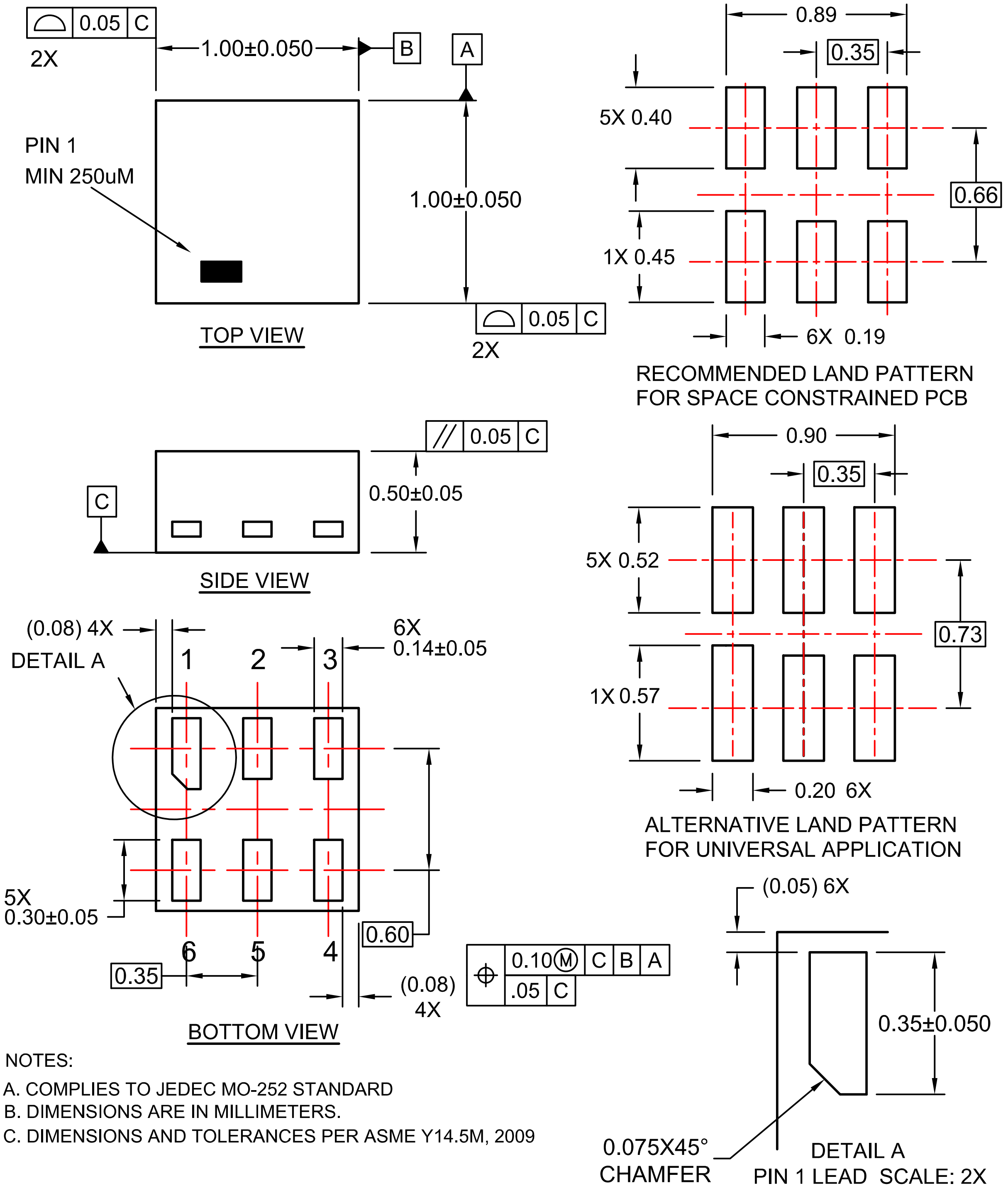
CASE 517DP
ISSUE O

DATE 31 AUG 2016



NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009

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