NCP81044

Product Preview

Low Voltage Synchronous Buck Controller

The NCP81044 is a PWM controller designed to operate from a 5 V or 12 V supply. These devices are capable of producing an output voltage as low as 0.8 V. These 8−pin devices provide an optimal level of integration to reduce size and cost of the power supply. The NCP81044 provides a 1 A gate driver design and an internally set 275 kHz oscillator. In addition to the 1 A gate drive capability, other efficiency enhancing features of the gate driver include adaptive non−overlap circuitry. The devices also incorporate an externally compensated error amplifier and a capacitor programmable soft−start function. Protection features include programmable short circuit protection and under voltage lockout (UVLO). The NCP81044 comes in an 8−pin SOIC package.

Features

- Input Voltage Range from 4.5 to 13.2 V
- 275 kHz Internal Oscillator
- Boost Pin Operates to 30 V
- Voltage Mode PWM Control
- 0.8 V ±1.0 % Internal Reference Voltage
- Adjustable Output Voltage
- Capacitor Programmable Soft−Start
- Internal 1 A Gate Drivers
- 80% Max Duty Cycle
- Input Under Voltage Lockout
- Programmable Current Limit
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Graphics Cards
- Desktop Computers
- Servers / Networking
- DSP & FPGA Power Supply
- DC−DC Regulator Modules

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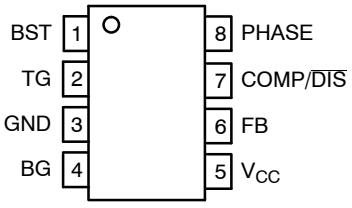
MARKING DIAGRAM

SOIC−8
D SUFFIX
CASE 751

81044 = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Device

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP81044DR2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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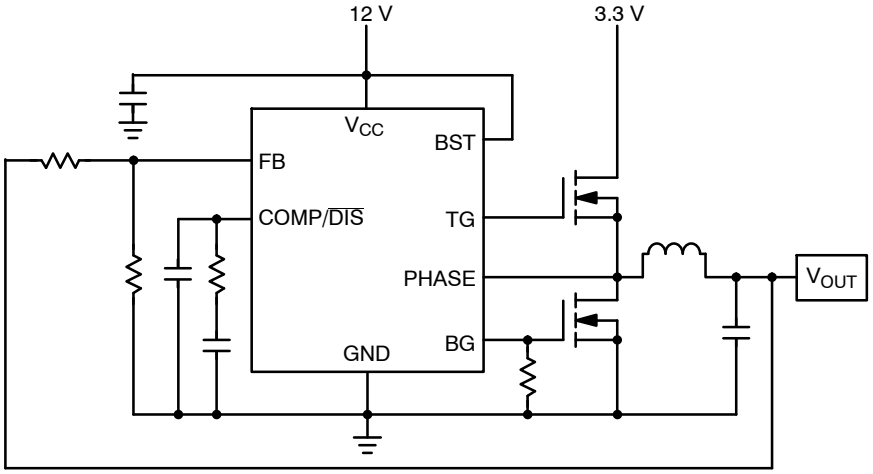


Figure 1. Typical Application Diagram

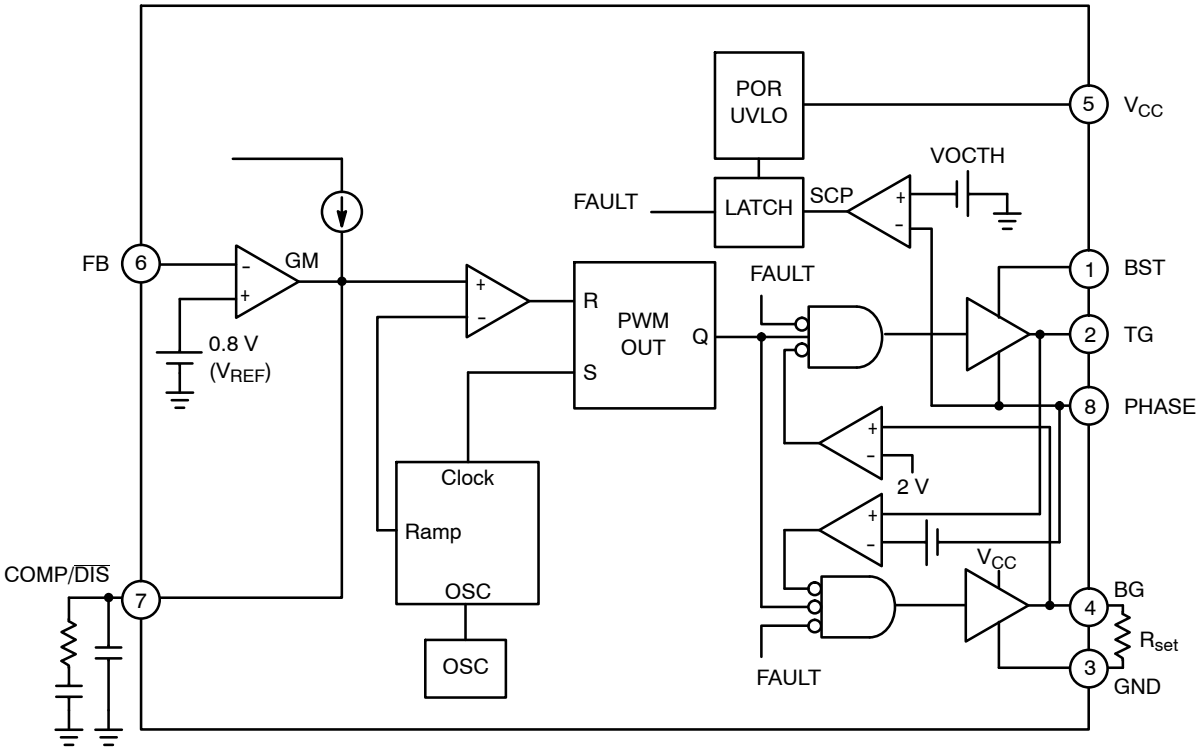


Figure 2. Detailed Block Diagram

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BST	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BST pin). Connect a capacitor (C_{BST}) between this pin and the PHASE pin. Typical values for C_{BST} range from 0.1 μF to 1 μF. Ensure that C_{BST} is placed near the IC.
2	TG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N−Channel MOSFET.
3	GND	IC ground reference. All control circuits are referenced to this pin.
4	BG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N−Channel MOSFET.
5	V_{CC}	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 μF capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
6	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage−control feedback loop. Connect this pin to the output resistor divider (if used) or directly to V_{out}.
7	COMP/$\overline{DIS}$	Compensation Pin. This is the output of the error amplifier (EA) and the non−inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage−control feedback loop. The compensation capacitor also acts as a soft−start capacitor. Pull this pin low for disable.
8	PHASE	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	V_{MAX}	V_{MIN}
Main Supply Voltage Input	V_{CC}	15 V	−0.3 V
Bootstrap Supply Voltage Input	BST	35 V wrt/PGND 40 V < 50 ns wrt/PGND 15 V wrt/SW	−0.3 V −0.3 V −0.3 V
Switching Node (Bootstrap Supply Return)	PHASE	35 V 40 V < 50 ns	−5.0 V −10 V for < 200 ns
High−Side Driver Output (Top Gate)	TG	30 V wrt/GND 15 V wrt/PHASE	−0.3 V wrt/PHASE −2 V < 200 ns wrt/PHASE
Low−Side Driver Output (Bottom Gate)	BG	15 V	−0.3 V −5.0 V for < 200 ns
Feedback	FB	5.5 V	−0.3 V
COMP/$\overline{DISABLE}$	COMP/$\overline{DIS}$	5.5 V	−0.3 V

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	165	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	45	°C/W
Operating Junction Temperature Range	T_J	0 to 125	°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS ($0°C < T_A < 70°C$; $4.5\ V < V_{CC} < 13.2\ V$, $4.5\ V < [BST–PHASE] < 13.2\ V$, $4.5\ V < BST < 30\ V$, $0\ V < PHASE < 21\ V$, $C_{TG} = C_{BG} = 1.0\ nF$, for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range	–	4.5	–	13.2	V
Boost Voltage Range	–	4.5	–	26.5	V
Supply Current					
Quiescent Supply Current	V_{FB} = 1.0 V, No Switching, V_{CC} = 13.2 V	1.0	–	8.0	mA
Boost Quiescent Current	V_{FB} = 1.0 V, No Switching, V_{CC} = 13.2 V	0.1	–	1.0	mA
Under Voltage Lockout					
UVLO Threshold	V_{CC} Rising Edge	3.8	–	4.2	V
UVLO Hysteresis	–	–	350	–	mV
Switching Regulator					
VFB Feedback Voltage, Control Loop in Regulation	T_A = 0 to 70°C	792	800	808	mV
Oscillator Frequency	T_A = 0 to 70°C	250	275	300	kHz
Ramp–Amplitude Voltage		0.8	1.1	1.4	V
Minimum Duty Cycle		0	–	–	%
Maximum Duty Cycle		80	88	93	%
Error Amplifier (GM)					
Transconductance		3.0	–	4.4	mmho
Open Loop DC Gain		55	70	–	DB
Output Source Current Output Sink Current	V_{FB} < 0.8 V V_{FB} > 0.8 V	80 80	120 120	– –	μA
Input Bias Current		–	0.1	1.0	μA
Soft–Start					
SS Source Current	V_{FB} < 0.8 V	8.49	11	13.3	μA
Switch Over Threshold	V_{FB} = 0.8 V	–	100	–	% of Vref
Gate Drivers					
Upper Gate Source	V_{CC} = 12 V, VTG = VBG = 2.0 V	–	1.0	–	A
Upper Gate Sink		–	1.0	–	A
Lower Gate Source		–	1.0	–	A
Lower Gate Sink		–	2.0	–	A
TG Falling to BG Rising Delay	V_{CC} = 12 V, TG < 2.0 V, BG > 2.0 V	–	40	90	ns
BG Falling to TG Rising Delay	V_{CC} = 12 V, BG < 2.0 V, TG > 2.0 V	–	35	90	ns
Enable Threshold		0.3	0.4	0.5	V
Over–Current Protection					
OCSET Current Source	Sourced from BG pin, before SS	8.9	10	11.1	μA
OC Switch–Over Threshold		–	700	–	mV
Fixed OC Threshold		–	–375	–	mV

TYPICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

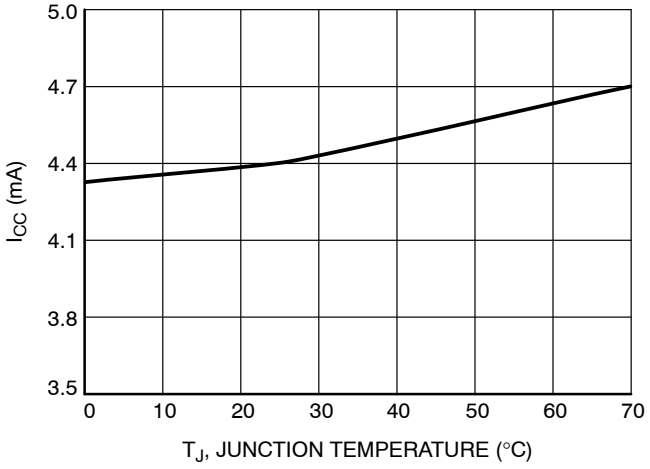


Figure 3. I_{CC} vs. Temperature

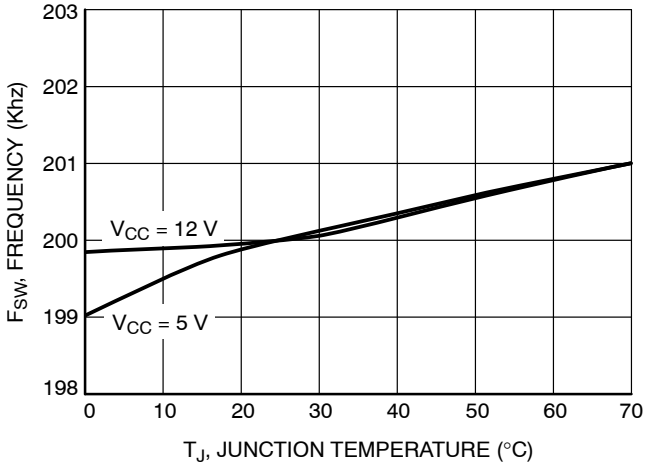


Figure 4. Oscillator Frequency (F_{SW}) vs. Temperature

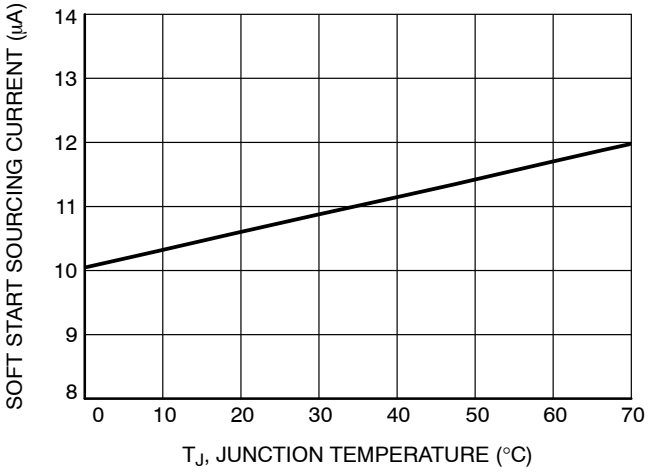


Figure 5. Soft Start Sourcing Current vs. Temperature

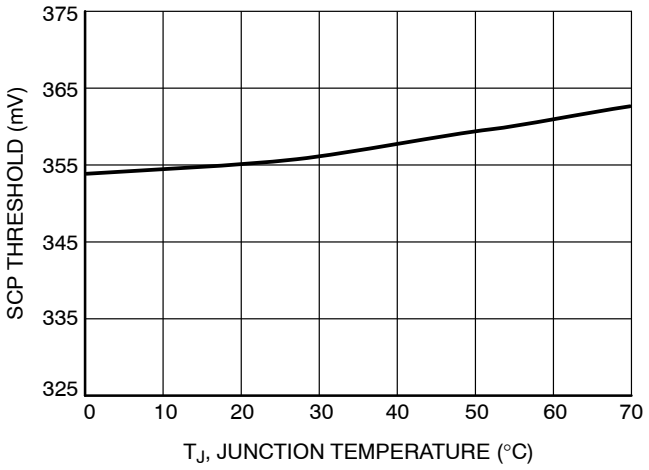


Figure 6. SCP Threshold vs. Temperature

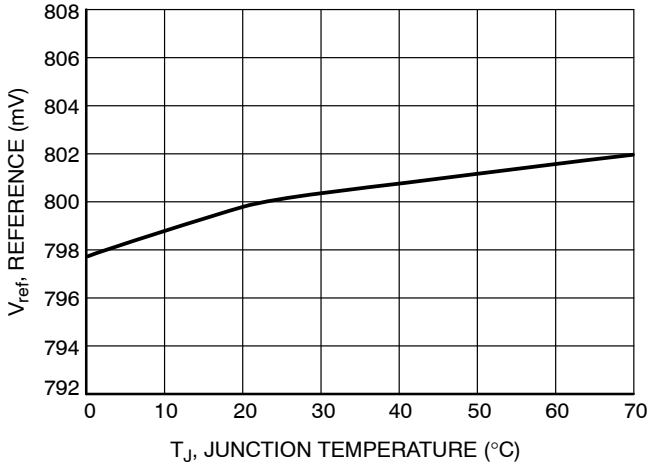


Figure 7. Reference Voltage (V_{ref}) vs. Temperature

DETAILED OPERATING DESCRIPTION

General

The NCP81044 is a PWM controller intended for DC−DC conversion from 5.0 V & 12 V buses. The devices have a 1 A internal gate driver circuit designed to drive N−channel MOSFETs in a synchronous−rectifier buck topology. The output voltage of the converter can be precisely regulated down to 800 mV ±1.0% when the V_{FB} pin is tied to V_{OUT}. The switching frequency, is internally set to 275 kHz. A high gain operational transconductance error amplifier (OTA) is used.

Duty Cycle and Maximum Pulse Width Limits

In steady state DC operation, the duty cycle will stabilize at an operating point defined by the ratio of the input to the output voltage. The devices can achieve an 80% duty cycle. There is a built in off−time which ensures that the bootstrap supply is charged every cycle. This part can allow a 12 V to 0.8 V conversion at 275 kHz.

Input Voltage Range (V_{CC} and BST)

The input voltage range for both V_{CC} and BST is 4.5 V to 13.2 V with respect to GND and PHASE, respectively. Although BST is rated at 13.2 V with respect to PHASE, it can also tolerate 26.4 V with respect to GND.

External Enable/Disable

When the Comp pin voltage falls or is pulled externally below the 400 mV threshold, it disables the PWM Logic and the gate drive outputs. In this disabled mode, the operational transconductance amplifier (EOTA) output source current is reduced and limited to the Soft−Start mode of 10 μA.

Normal Shutdown Behavior

Normal shutdown occurs when the IC stops switching because the input supply reaches UVLO threshold. In this case, switching stops, the internal SS is discharged, and all GATE pins go low. The switch node enters a high impedance state and the output capacitors discharge through the load with no ringing on the output voltage.

External Soft−Start

The NCP81044 features an external soft−start function, which reduces inrush current and overshoot of the output voltage. Soft−start is achieved by using the internal current source of 10 μA (typ), which charges the external integrator capacitor of the transconductance amplifier. Figure 8 is a typical soft−start sequence. This sequence begins once V_{CC} surpasses its UVLO threshold and OCP programming is complete. During soft−start, as the Comp Pin rises through 400 mV, the PWM Logic and gate drives are enabled. When the feedback voltage crosses 800 mV, the EOTA will be given control to switch to its higher regulation mode output current of 120 μA.

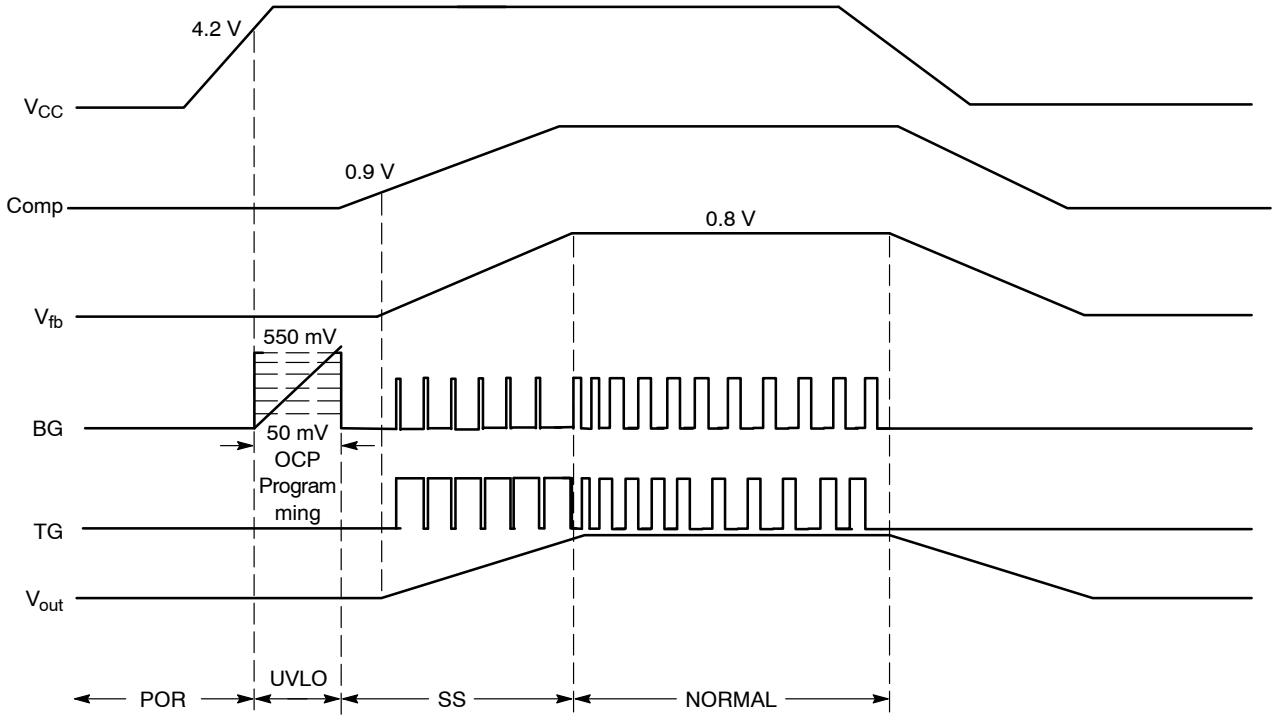


Figure 8. Soft−Start Implementation

UVLO

Undervoltage Lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{CC} is too low to support the internal rails and power the converter. For the NCP81044, the UVLO is set to permit operation when converting from a 5.0 input voltage.

Overcurrent Threshold Setting

NCP81044 can easily program an Overcurrent Threshold ranging from 50 mV to 550 mV, simply by adding a resistor (RSET) between BG and GND. During a short period of time following V_{CC} rising over UVLO threshold, an internal 10 μA current (I_{OCSET}) is sourced from BG pin, determining a voltage drop across R_{OCSET}. This voltage drop will be sampled and internally held by the device as Overcurrent Threshold. The OC setting procedure overall time length is about 6 ms. Connecting a R_{OCSET} resistor between BG and GND, the programmed threshold will be:

$$I_{OCth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}} \quad \text{(eq. 1)}$$

RSET values range from 5 kΩ to 55 kΩ. In case R_{OCSET} is not connected, the device switches the OCP threshold to a fixed 375 mV value: an internal safety clamp on BG is triggered as soon as BG voltage reaches 700 mV, enabling the 375 mV fixed threshold and ending OC setting phase. The current trip threshold tolerance is ±25 mV. The accuracy of the set point is best at the highest set point (550 mV). The accuracy will decrease as the set point decreases.

Current Limit Protection

In case of a short circuit or overload, the low−side (LS) FET will conduct large currents. The controller will shut down the regulator in this situation for protection against overcurrent. The low−side $R_{DS(on)}$ sense is implemented at the end of each of the LS−FET turn−on duration to sense the over current trip point. While the LS driver is on, the Phase voltage is compared to the internally generated OCP trip voltage. If the phase voltage is lower than OCP trip voltage, an overcurrent condition occurs and a counter is initiated. When the counter completes, the PWM logic and both HS−FET and LS−FET are turned off. The controller has to go through a Power On Reset (POR) cycle to reset the OCP fault.

Drivers

The NCP81044 includes gate drivers to switch external N−channel MOSFETs. This allows the devices to address high−power as well as low−power conversion requirements. The gate drivers also include adaptive non−overlap circuitry. The non−overlap circuitry increase efficiency, which minimizes power dissipation, by minimizing the body diode conduction time.

A detailed block diagram of the non−overlap and gate drive circuitry used in the chip is shown in Figure 9.

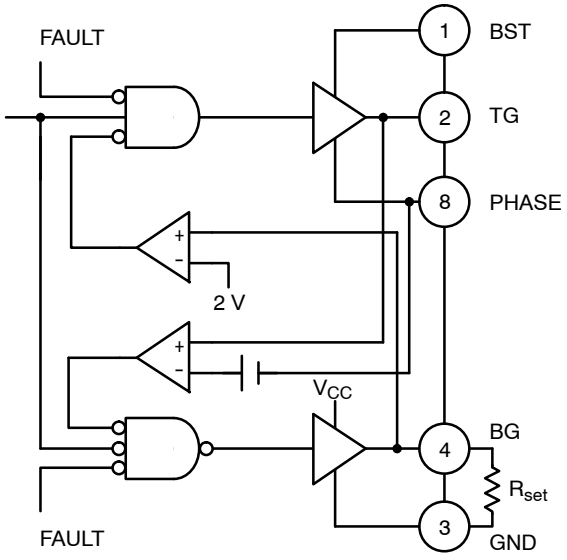


Figure 9. Block Diagram

Careful selection and layout of external components is required, to realize the full benefit of the onboard drivers. The capacitors between V_{CC} and GND and between BST and SWN must be placed as close as possible to the IC. The current paths for the TG and BG connections must be optimized. A ground plane should be placed on the closest layer for return currents to GND in order to reduce loop area and inductance in the gate drive circuit.

APPLICATION SECTION

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$Iin_{RMS} = I_{OUT}\sqrt{D \times (1 - D)} \ ,$$

where D is the duty cycle, Iin_{RMS} is the input RMS current, & I_{OUT} is the load current. The equation reaches its maximum value with D = 0.5. Loss in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \times Iin_{RMS}{}^2 \ ,$$

where P_{CIN} is the power loss in the input capacitors & ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must by surge protected. Otherwise, capacitor failure could occur.

Calculating Input Start-up Current

To calculate the input start up current, the following equation can be used.

$$I_{inrush} = \frac{C_{OUT} \times V_{OUT}}{t_{SS}} \ ,$$

where I_{inrush} is the input current during start-up, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the soft start interval.

If the inrush current is higher than the steady state input current during max load, then the input fuse should be rated accordingly, if one is used.

Calculating Soft Start Time

To calculate the soft start time, the following equation can be used.

$$t_{ss} = \frac{(C_p + C_c) * \Delta V}{I_{ss}}$$

Where C_c is the compensation as well as the soft start capacitor,

C_p is the additional capacitor that forms the second pole.

I_{ss} is the soft start current

ΔV is the comp voltage from 0.9 V to until it reaches regulation: ((d * ramp) + 0.9)

Output Capacitor Selection

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The controller immediately recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

During a load step transient the output voltage initial drops due to the current variation inside the capacitor and the ESR. ((neglecting the effect of the effective series inductance (ESL)):

$$\Delta V_{OUT-ESR} = \Delta I_{OUT} \times ESR_{COUT}$$

where $V_{OUT-ESR}$ is the voltage deviation of V_{OUT} due to the effects of ESR and the ESR_{COUT} is the total effective series resistance of the output capacitors.

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is given by the following equation:

$$\Delta V_{OUT-DISCHARGE} = \frac{\Delta I_{OUT}{}^2 \times L_{OUT}}{2 \times C_{OUT} \times (V_{IN} \times D - V_{OUT})} \ ,$$

where $V_{OUT-DISCHARGE}$ is the voltage deviation of V_{OUT} due to the effects of discharge, L_{OUT} is the output inductor value & V_{IN} is the input voltage.

It should be noted that $\Delta V_{OUT-DISCHARGE}$ and $\Delta V_{OUT-ESR}$ are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL).

Inductor Selection

Both mechanical and electrical considerations influence the selection of an output inductor. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space-constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by:

$$SlewRate_{LOUT} = \frac{V_{IN} - V_{OUT}}{L_{OUT}}$$

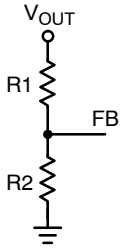
This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. This results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak-to-peak ripple current for NCP81044 is given by the following equation:

$$Ipk - pk_{LOUT} = \frac{V_{OUT}(1 - D)}{L_{OUT} \times 275\ kHz} \ ,$$

where $Ipk\text{-}pk_{LOUT}$ is the peak to peak current of the output. From this equation it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade-off between dynamic response and ripple current.

Feedback and Compensation

The NCP81044 allows the output of the DC-DC converter to be adjusted from 0.8 V to 5.0 V via an external resistor divider network. The controller will try to maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the controller will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin.



The relationship between the resistor divider network above and the output voltage is shown in the following equation:

$$R_2 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}} \right)$$

Resistor R1 is selected based on a design tradeoff between efficiency and output voltage accuracy. For high values of R1 there is less current consumption in the feedback network, However the trade off is output voltage accuracy due to the bias current in the error amplifier. The output voltage error of this bias current can be estimated using the following equation (neglecting resistor tolerance):

$$\text{Error\%} = \frac{0.1\ \mu A \times R_1}{V_{REF}} \times 100\%$$

Once R1 has been determined, R2 can be calculated.

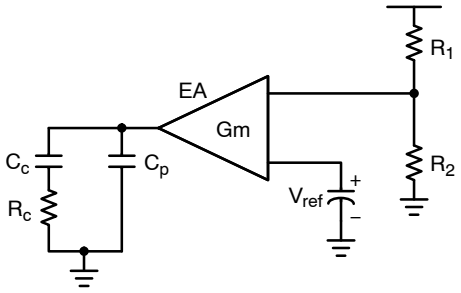


Figure 10. Type II Transconductance Error Amplifier

Figure 10 shows a typical Type II transconductance error amplifier (EOTA). The compensation network consists of the internal error amplifier and the impedance networks ZIN (R_1, R_2) and external Z_{FB} (R_c, C_c and C_p). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response (but always lower than $F_{SW}/8$) and the highest gain in DC conditions to minimize the load regulation. A stable control loop has a gain crossing with -20 dB/decade slope and a phase margin greater than 45°. Include worst-case component variations when determining phase margin. Loop stability is defined by the compensation network around the EOTA, the output capacitor, output inductor and the output divider. Figure 11 shows the open loop and closed loop gain plots.

Compensation Network Frequency:

The inductor and capacitor form a double pole at the frequency

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_o \times C_o}}$$

The ESR of the output capacitor creates a “zero” at the frequency,

$$F_{ESR} = \frac{1}{2\pi \times ESR \times C_o}$$

The zero of the compensation network is formed as,

$$F_Z = \frac{1}{2\pi \times R_c C_c}$$

The pole of the compensation network is calculated as,

$$F_p = \frac{1}{2\pi \times R_c \times C_p}$$

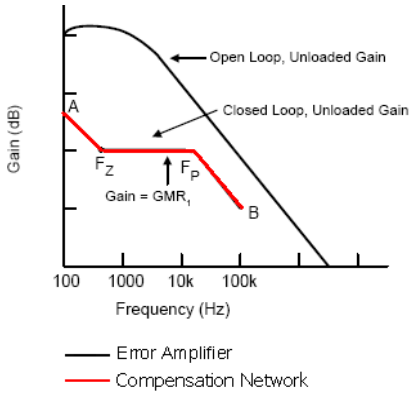


Figure 11. Gain Plot of the Error Amplifier

Thermal Considerations

The power dissipation of the NCP81044 varies with the MOSFETs used, V_{CC}, and the boost voltage (V_{BST}). The average MOSFET gate current typically dominates the control IC power dissipation. The IC power dissipation is determined by the formula:

$$P_{IC} = (I_{CC} \times V_{CC}) + P_{TG} + P_{BG}$$

Where:

P_{IC} = control IC power dissipation,
I_{CC} = IC measured supply current,
V_{CC} = IC supply voltage,
P_{TG} = top gate driver losses,
P_{BG} = bottom gate driver losses.

The upper (switching) MOSFET gate driver losses are:

$$P_{TG} = Q_{TG} \times f_{SW} \times V_{BST}$$

Where:

Q_{TG} = total upper MOSFET gate charge at VBST,
f_{SW} = the switching frequency,
V_{BST} = the BST pin voltage.

The lower (synchronous) MOSFET gate driver losses are:

$$P_{BG} = Q_{BG} \times f_{SW} \times V_{CC}$$

Where:

Q_{BG} = total lower MOSFET gate charge at V_{CC}.

The junction temperature of the control IC can then be calculated as:

$$T_J = T_A + P_{IC} \times \theta_{JA}$$

Where:

T_J = the junction temperature of the IC,

T_A = the ambient temperature,

θ_{JA} = the junction−to−ambient thermal resistance of the IC package.

The package thermal resistance can be obtained from the specifications section of this data sheet and a calculation can be made to determine the IC junction temperature. However, it should be noted that the physical layout of the board, the proximity of other heat sources such as MOSFETs and inductors, and the amount of metal connected to the IC, impact the temperature of the device. Use these calculations as a guide, but measurements should be taken in the actual application.

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding. The figure below shows the critical power components of the converter. To minimize the voltage overshoot the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in the figure below should be located as close together as possible. Please note that the capacitors C_{IN} and C_{OUT} each represent numerous physical capacitors. It is desirable to locate the NCP81044 within 1 inch of the MOSFETs, Q1 and Q2. The circuit traces for the MOSFETs' gate and source connections from the NCP81044 must be sized to handle up to 2 A peak current.

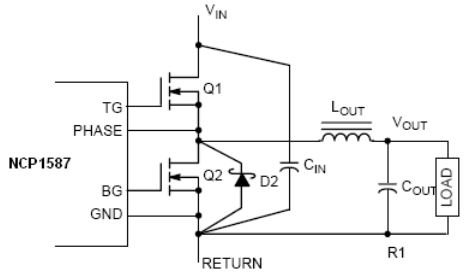


Figure 12. Components to be Considered for Layout Specifications

DESIGN EXAMPLE I: Type II Compensation (Electrolytic Cap. with large ESR)

Switching Frequency	F_{SW} = 275 KHz
Output Capacitance	R_{ESR} = 45 mΩ/Each
Output Capacitance	C_{out} = 2×1800 μF
Output Inductance	L_{out} = 1 μH
Input Voltage	V_{in} = 12 V
Output Voltage	V_{out} = 1.6 V

Choose the loop gain crossover frequency;

$$F_{co} = \frac{1}{5} \times F_{sw} = 55\ \text{KHz}$$

The corner frequency of the output filter is calculated below;

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{1\ \mu\text{H} \times 3600\ \mu\text{F}}} = 2.65\ \text{KHz}$$

Check that the ESR zero frequency is not too high;

$$F_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_O} < \frac{F_{co}}{10}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times \frac{45\ \text{m}\Omega}{2} \times (1800\ \mu\text{F} \times 2)} = 2\ \text{KHz}$$

If ESR zero is larger than F_{co}/10, Type III compensation is necessary.

Choose C_C for the crossover frequency and the soft start

$$C_C = 100\ \text{nF}$$

The compensation capacitor (C_C) is related to the loop gain magnitude, zero position and the soft start. By adjusting the value of this compensation capacitor, the crossover frequency and the soft start time can be adjusted.

Zero of the compensation network is calculated as follows;

$$F_Z = F_{LC} = 2.65\ \text{KHz}$$

$$R_C = \frac{1}{2 \times \pi \times F_z \times C_C} = \frac{1}{2 \times \pi \times 2.65\ \text{kHz} \times 100\ \text{nF}} = 600.6\ \Omega$$

Pole of the compensation network is calculated as follows;

$$F_p = F_{sw} = 275\ \text{KHz}$$

$$C_p = \frac{1}{2 \times \pi \times F_p \times R_C} = \frac{1}{2 \times \pi \times 275\ \text{kHz} \times 600.6} = 963.6\ \text{pF}$$

The recommended compensation values are; R_C = 604, C_C = 100 nF, C_P = 1000 pF

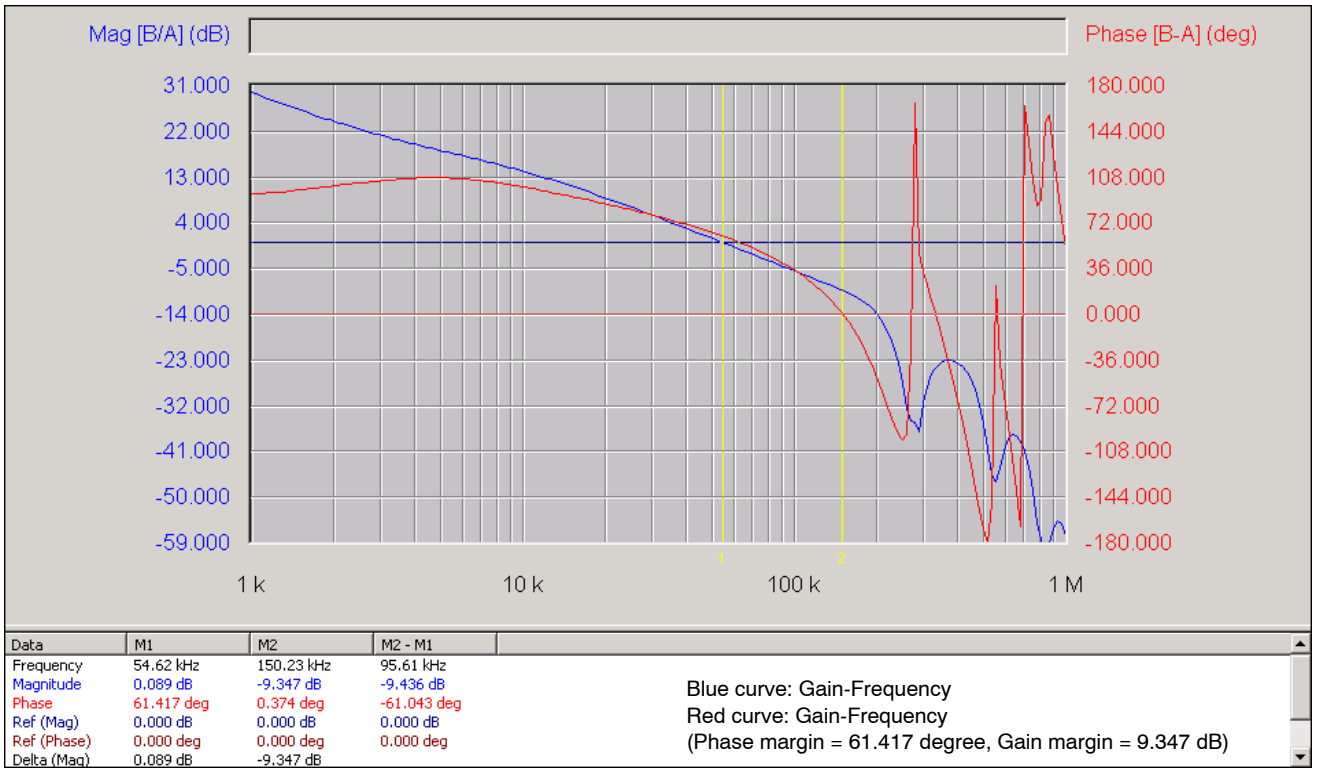


Figure 13. Closed-loop Voltage Loop-gain of the NCP81044

DESIGN EXAMPLE II: Type III Compensation (Oscon Cap. with small ESR; Do not place R_C, C_C, C_P)

Switching Frequency	F_{sw} = 275 KHz
Output Capacitance	R_{ESR} = 7 mΩ/Each
Output Capacitance	C_{out} = 2×560 μF
Output Inductance	L_{out} = 1 μH
Input Voltage	V_{in} = 12 V
Output Voltage	V_{out} = 1.6 V

Choose the loop gain crossover frequency;

$$F_{co} = \frac{1}{5} \times F_{sw} = 55\ KHz$$

The corner frequency of the output filter is calculated below;

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{1\ \mu H \times 1120\ \mu F}} = 4.7\ KHz$$

Check the ESR zero frequency;

$$F_{ESR} = \frac{1}{2 \times \pi \times R_{ESR} \times C_O}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times 7\ m\Omega \times 560\ \mu F} = 40.6\ KHz$$

Choose C_{C1} for the soft start

$$C_{C1} = 33\ nF$$

The compensation capacitor (C_{C1}) is related to the loop gain magnitude, one zero position and the soft start. By adjusting the value of this compensation capacitor, the crossover frequency and the soft start time can be adjusted.

Zeros of the compensation network are calculated as follows;

1st zero;

$$F_{Z1} = \frac{F_{LC}}{10} = 470\ Hz$$

$$R_{C1} = \frac{1}{2 \times \pi \times F_{z1} \times C_{C1}}$$

$$= \frac{1}{2 \times \pi \times 470\ Hz \times 30\ nF} = 11.3\ k\Omega$$

R_{C1} should be much larger than 2/gm in order to get the stable system with transconductance amplifier. ➞ choose R_{C1} = 12.1 kΩ

2nd zero;

Choose R3 for the crossover frequency. R3 should be much larger than 2/gm for the stable system.

$$R3 = 10\ k\Omega$$

$$F_{z2} = F_{LC} = 4.7\ KHz$$

$$C20 = \frac{1}{2 \times \pi \times F_{z2} \times R3}$$

$$= \frac{1}{2 \times \pi \times 4.7\ KHz \times 10\ k\Omega} = 3.4\ nF$$

Choose C20 = 3.3 nF

Poles of the compensation network are calculated as follows;

1st pole;

Choose R4 to cancel the output capacitor ESR zero.

$$F_{P1} = F_{ESR} = 40.6\ KHz$$

$$R4 = \frac{1}{2 \times \pi \times F_{P1} \times C20}$$

$$= \frac{1}{2 \times \pi \times 40.6\ kHz \times 3.3\ n} = 1.2\ k\Omega$$

After choose R4 value, adjust R4 to get enough phase margin → R4 = 665 Ω

2nd pole;

Choose C_{P1} to eliminate the noise;

$$F_{P2} = F_{sw} = 275\ KHz$$

$$C_{P1} = \frac{1}{2 \times \pi \times F_{P2} \times R_{C1}} = \frac{1}{2 \times \pi \times 275\ kHz \times 12\ k\Omega} = 48.23\ pF$$

Choose C_{P1} = 47 pF

The recommended compensation values are;

R2 = 10 kΩ, R3 = 10 kΩ, R4 = 665 Ω,

R_{C1} = 12.1 kΩ, C_{C1} = 33 nF, C_{P1}= 47 pF,

C20 = 3.3 nF

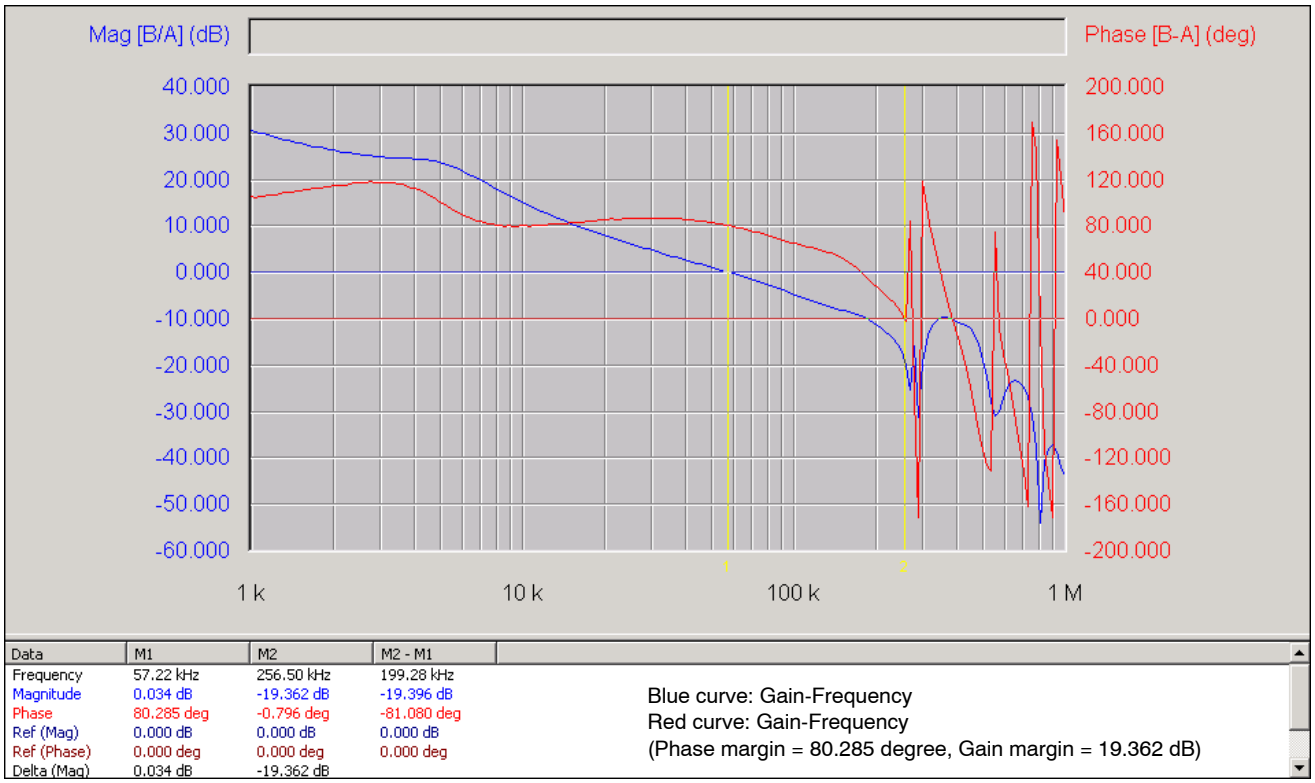


Figure 14. Closed-loop Voltage Loop-gain of the NCP81044

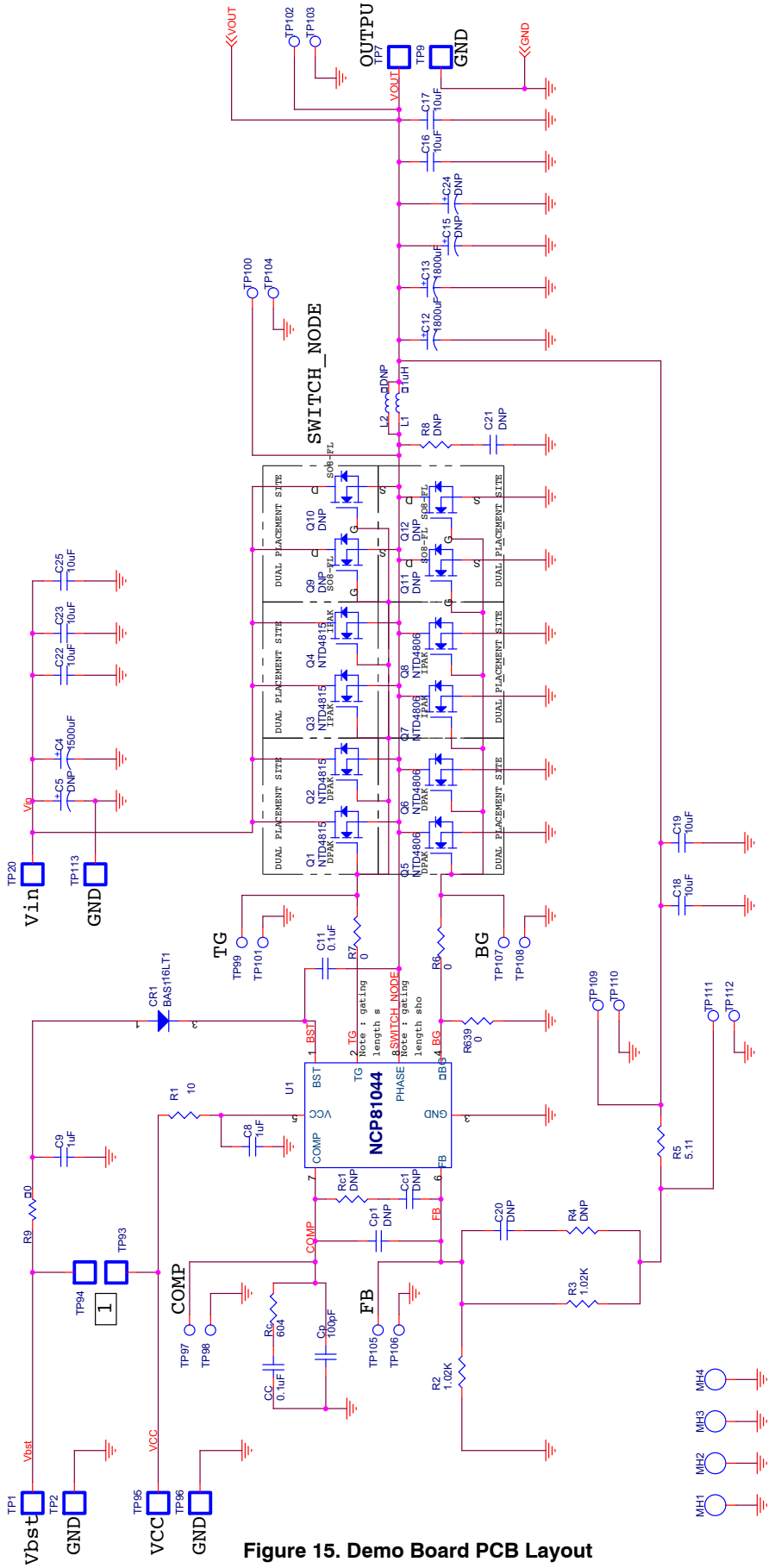


Figure 15. Demo Board PCB Layout

Bill of Materials

Item Number	Part Reference	Value	Quantity	MFG
1	C4	1500 μF	1	PANASONIC
2	C5	DNP	1	-
3	C8,C9	1 μF	2	TAIYO YUDEN
4	C11	0.1 μF	1	AVX
5	C12,C13	1800 μF	2	PANASONIC
6	C15,C24	DNP	2	-
7	C16,C17,C18,C19,C22,C23,C25	10 μF	7	PANASONIC
8	C20,CC1,CP1	DNP	3	-
9	C21	DNP	1	-
10	CC	0.1 μF	1	TDK
11	CR1	BAS116LT1	1	ON SEMICONDUCTOR
12	CP	100 pF	1	PANASONIC
13	J9	20PIN 2ROW	1	MOLEX
14	J23	5PIN	1	PASTERNACK ENTERPRISES
15	L1	1 μH	1	PANASONIC
16	L2	DNP	1	-
17	Q1,~~Q2~~	NTD4815	2	ON SEMICONDUCTOR
18	~~Q3,Q4~~	NTD4815	2	ON SEMICONDUCTOR
19	Q5,~~Q6~~	NTD4806	2	ON SEMICONDUCTOR
20	~~Q7,Q8~~	NTD4806	2	ON SEMICONDUCTOR
21	Q9,Q10,Q11,Q12	DNP	4	-
22	Q17,Q18,Q19,Q20,Q21,Q22,Q23,Q24,Q25,Q26, Q27,Q28,Q29,Q30,Q31,Q32,Q33,Q34,Q35,Q36, Q37,Q38,Q39,Q40	NTHS5404T1	24	ON SEMICONDUCTOR
23	R1	10	1	PANASONIC
24	R2,R3	1.02 K	2	DALE
25	R4,RC1	DNP	2	-
26	R5	5.11	1	DALE
27	R6,R7,R639	0	3	PANASONIC
28	R8	DNP	1	-
29	R9	0	1	DALE
30	R551,R552,R553,R569,R570,R571,R584,R585, R586,R599,R600,R601,R608,R609,R610,R617, R618,R619,R626,R627,R628,R635,R636,R637	100 K	24	DALE
31	R602,R603,R604,R605,R606,R607,R611,R612, R613,R614,R615,R616,R620,R621,R622,R623, R624,R625,R629,R630,R631,R632,R633,R634	0.56	24	PANASONIC
32	R638	49.9	1	DALE
33	RC	604	1	DALE
34	TP97,TP98,TP99,TP100,TP101,TP102,TP103, TP104,TP105,TP106,TP107,TP108,TP109, TP110,TP111,TP112	TP	16	KEYSTONE
35	U1	NCP81044	1	ON SEMICONDUCTOR

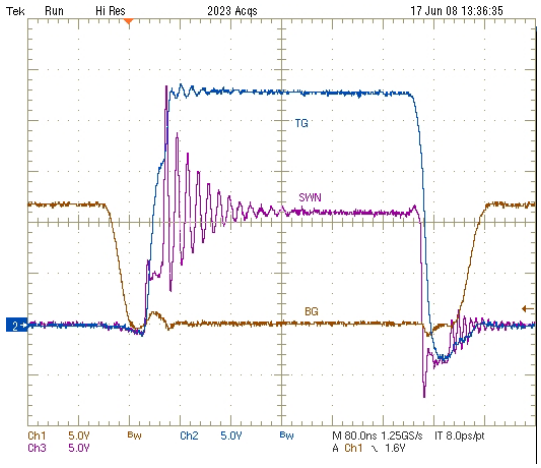


Figure 16. Gate Waveforms 20 A Load Sustaining

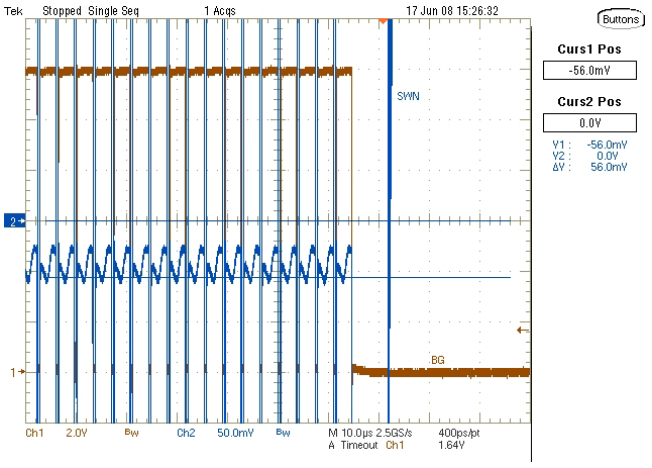


Figure 17. Over Current Protection (12.4 A DC Trip)

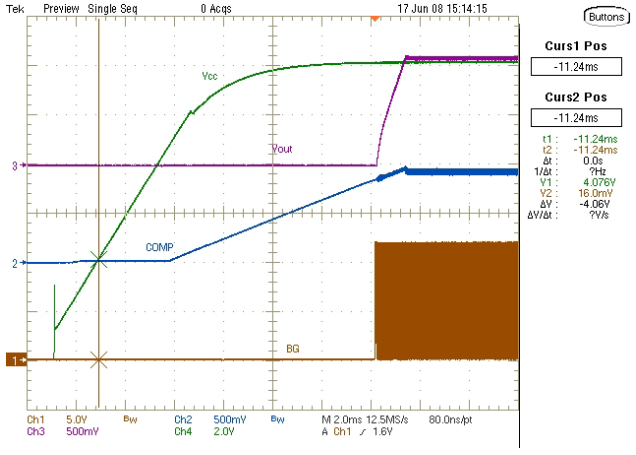


Figure 18. Start-up Sequence

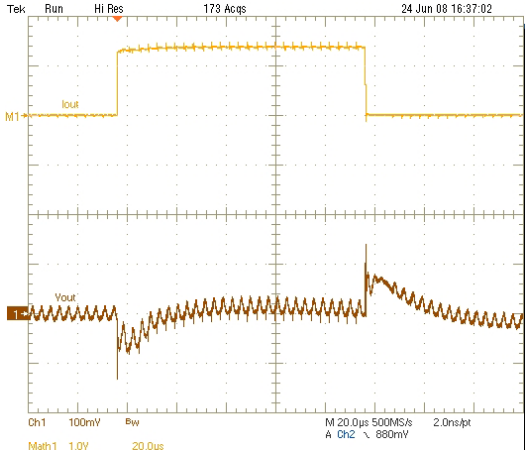


Figure 19. Transient Response 0-10 A Load Step

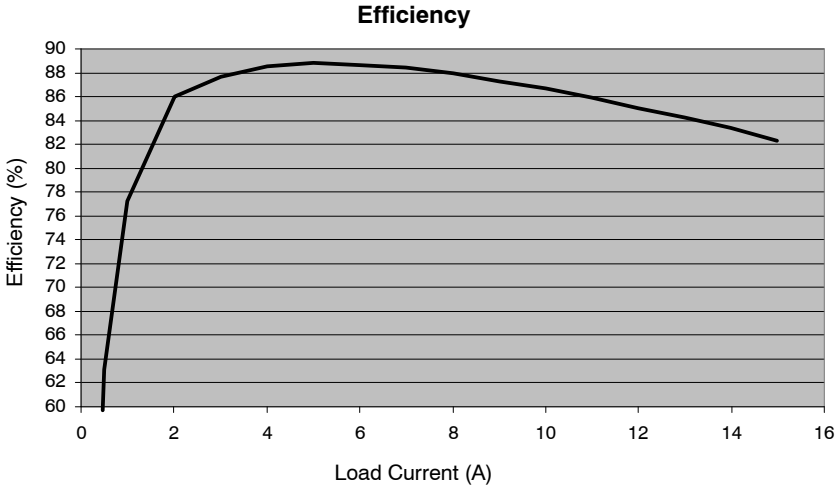


Figure 20. Efficiency vs. Load Current

SCALE 1:1

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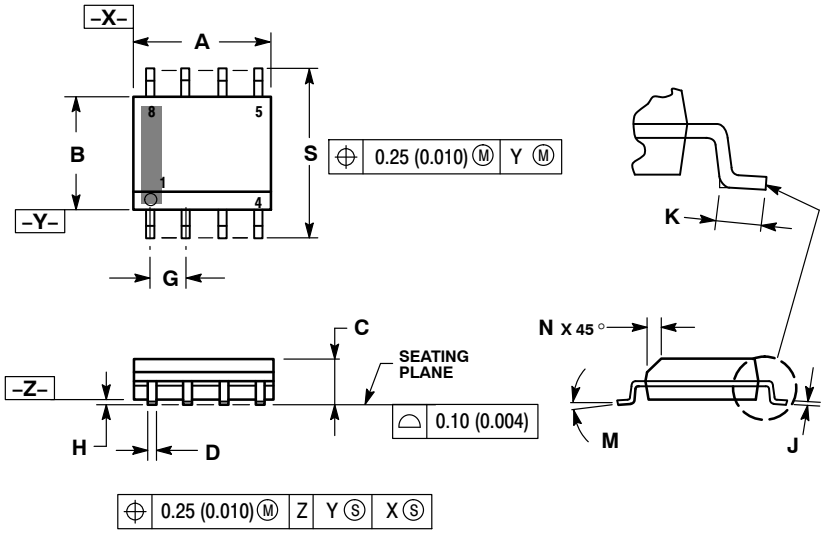
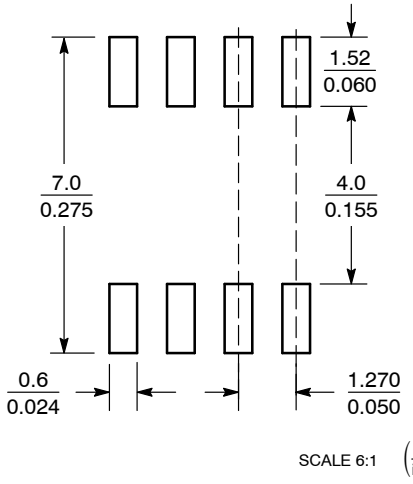


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

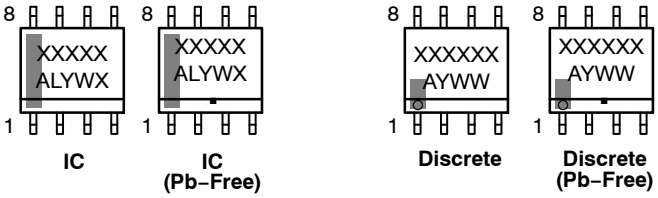
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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CASE 751−07
ISSUE AK

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STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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