PCI11010

PCIe Switch with Integrated Ethernet MAC & Programmable I/O

Highlights

- PCIe Gen 4 (8GT/s) switch fabric
- 1-lane PCIe Gen 4 (8GT/s) expansion port
- 2.5Gbps Ethernet MAC (RGMII/SGMII/SGMII+)
- I/O Multiplexer (SMBus/SPI/UART/GPIO)

Target Applications

- Industrial PCs (Network interface, PCIe fanout)

Features

- Integrated PCI switching fabric
  - 512byte maximum payload size
- Integrated PCIe physical interfaces
  - 2-lane (2x8GT/s) upstream port
  - 1-lane (1x8GT/s) downstream port
- 2.5Gbps Ethernet MAC
  - IEEE 802.3 compliant
  - RGMII support for 10/100/1000Mbps
  - SGMII support for 1Gbps
  - SGMII+ support for 2.5Gbps
  - Jumbo frame support
- Precision Time Protocol
  - IEEE 1588-2008 E2E and P2P one and two step support
  - IEEE 1588-2008 Programmable Time Compare output (e.g., 1PPS)
- Comprehensive power management features
  - PCIe 3.1 LPSS (Low Power Sub States): L2 (with aux. power supply)
- Power and I/O
  - Integrated power-on reset circuit with configurable under/over voltage protection
  - Latch-up performance exceeds 150mA per EIA/JESD78, Class II
  - JEDEC Class 3A ESD performance
- UARTs
  - RS232/RS485
  - Auto-direction control
  - Standard and advanced speed support
  - Basic or comprehensive signal support
- Additional features
  - Multifunction GPIOs
  - Programmable pin multiplexer
  - Ability to use low-cost 25MHz crystal or clock for reduced BOM
  - SPI peripheral interface
  - SMBus target interface
  - SMBus controller interface
  - PVT Sensor
  - JTAG TAP
- Packaging
  - Pb-free RoHS compliant 100-pin VQFN package
- Environmental
  - Available in commercial and industrial grades

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1.0 INTRODUCTION

1.1 General Description

The Microchip PCI11010 is a single-chip PCIe switch with an integrated Ethernet MAC and programmable I/O. The integrated PCIe physical interfaces provide a 2-lane (2x8GT/s) upstream port and a 1-lane (1x8GT/s) downstream port. The device is targeted to address customer requests for higher bandwidth PCIe sub-systems within embedded applications. The maximum line rate is 8GT/s and it is certified against the GEN4 compliance program as defined in the PCIe Revision 4.x specifications. PCIe upstream can be delivered across a single or multiple lanes to accommodate best system architecture. The PCI11010 includes a compliant PCIe implementation from external facing physical interfaces through to switch fabric and endpoint controllers.

The PCI11010 also includes an IEEE 802.3 compliant 2.5Gbps Ethernet MAC. The integrated RGMII and SGMII interfaces support 10/100/1000Mbps and 1/2.5Gbps operation, respectively.

A programmable pin multiplexer is used to map I/O functions to package pins. This enables designers to work with either a default configuration or modify signals to best fit their application. Example signals include those associated with USB operation, through to GPIO or SMBus, which are accessed via a dedicated PCIe Endpoint Controller.

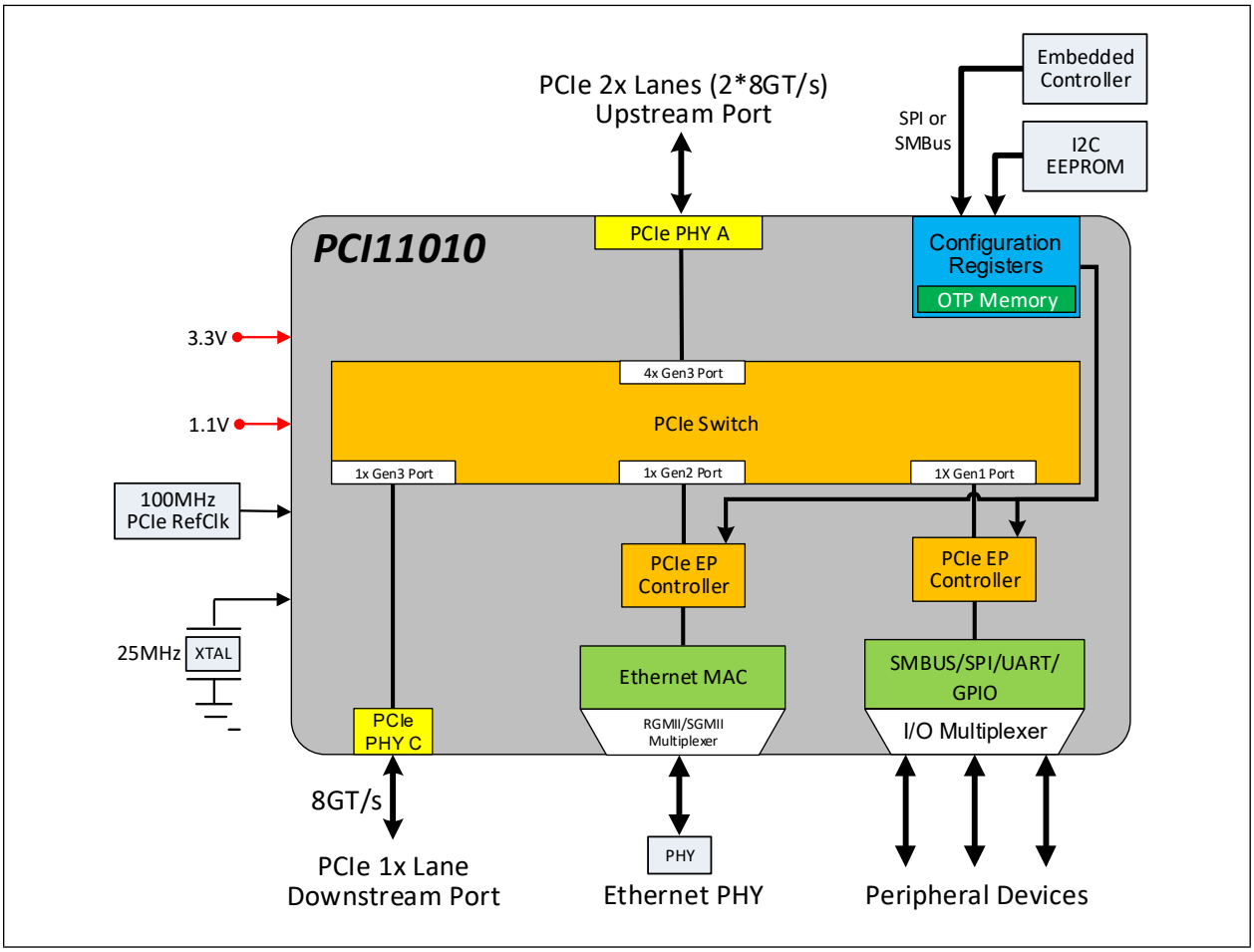
Though many clocks are required for PCI11010 operation, these are generated within an integrated clock farm. Only a single-ended 25MHz clock or crystal is required externally together with a PCIe reference clock.

PCI11010 software presentation is enabled using standard abstractions to major operating systems.

The PCI11010 is available in a 100-pin VQFN package in commercial (0°C to +70°C) or industrial (-40°C to +85°C) temperature ranges.

An internal block diagram of the PCI11010 is shown in Figure 1-1.

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



2.0 PACKAGE INFORMATION

FIGURE 2-1: 100-VQFN PACKAGE (DRAWING)

100-Lead Very Thin Quad Flat, No Lead Package (ZVX) - 12x12x0.9 mm Body [VQFN] With 8.0 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

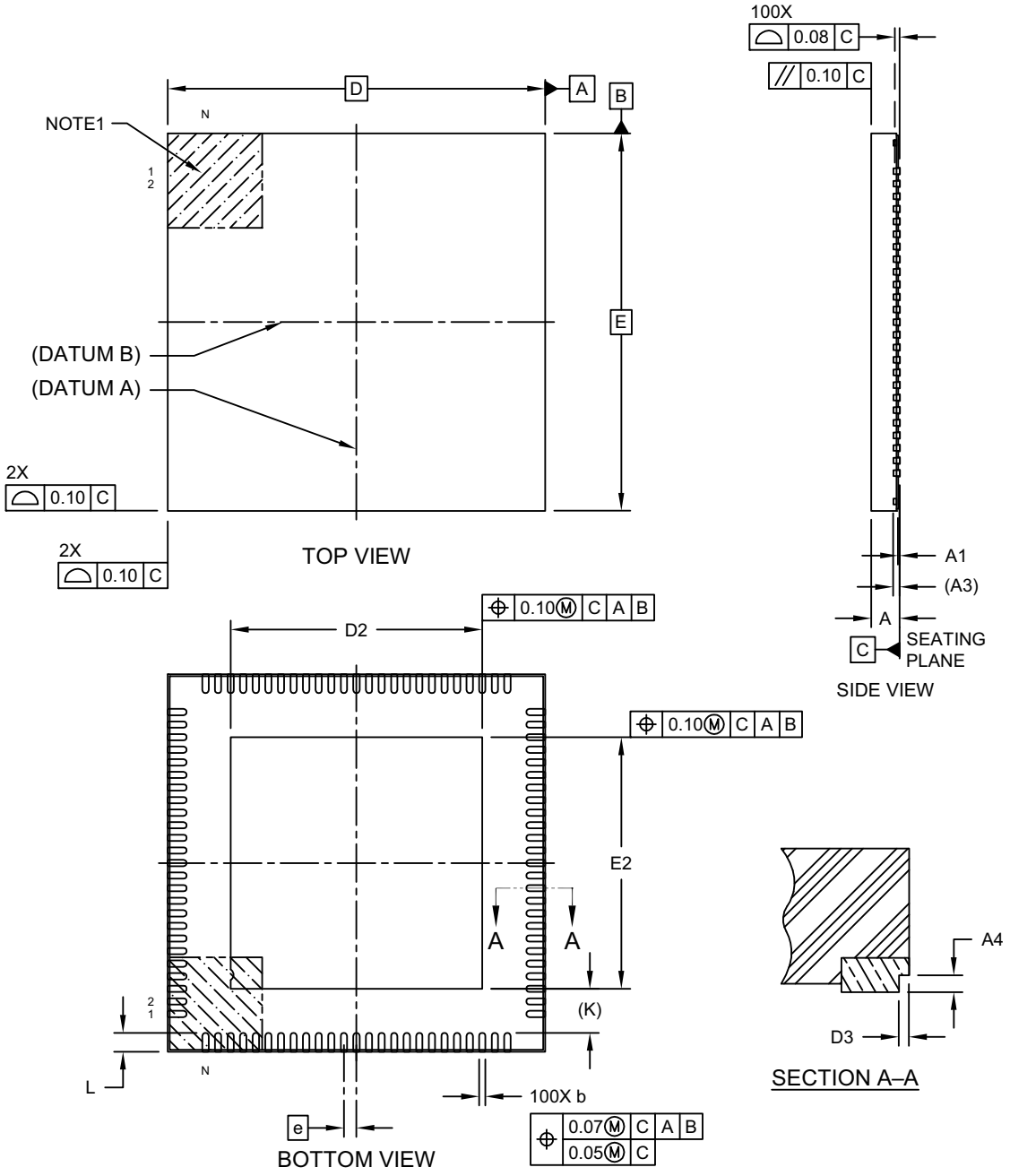
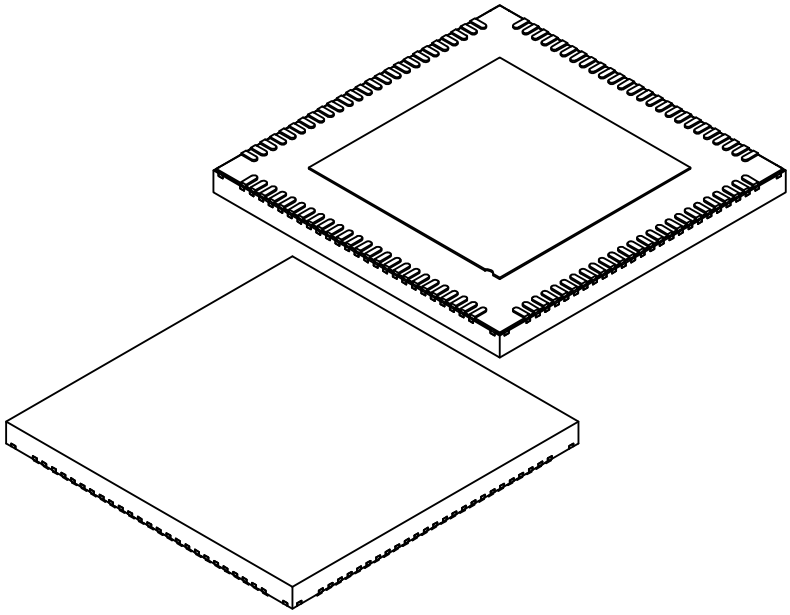


FIGURE 2-2: 100-VQFN PACKAGE (DIMENSIONS)

100-Lead Very Thin Quad Flat, No Lead Package (ZVX) - 12x12x0.9 mm Body [VQFN] With 8.0 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		100	
Pitch	e		0.40 BSC	
Overall Height	A	–	–	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		12.00 BSC	
Exposed Pad Length	D2	7.90	8.00	8.10
Overall Width	E		12.00 BSC	
Exposed Pad Width	E2	7.90	8.00	8.10
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K		1.40 REF	
Wettable Flank Step Cut Length	D3	-	-	0.085
Wettable Flank Step Cut Height	A4	0.10	-	0.19

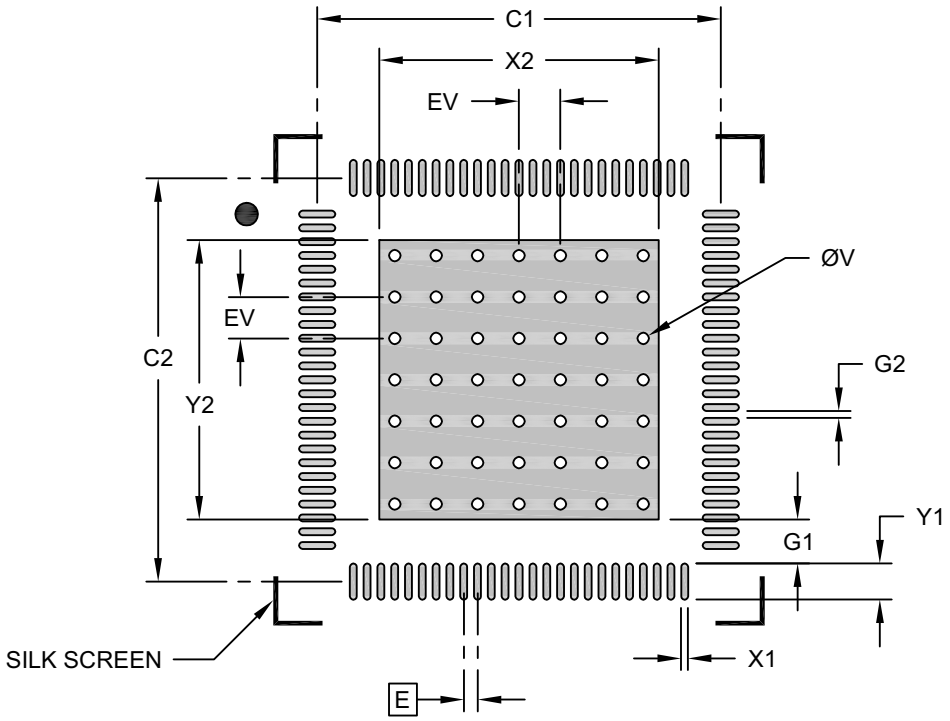
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

FIGURE 2-3: 100-VQFN PACKAGE (LAND PATTERN)

100-Lead Very Thin Quad Flat, No Lead Package (ZVX) - 12x12x0.9 mm Body [VQFN] With 8.0 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Center Pad Width	X2			8.10
Center Pad Length	Y2			8.10
Contact Pad Spacing	C1		11.70	
Contact Pad Spacing	C2		11.70	
Contact Pad Width (Xnn)	X1			0.20
Contact Pad Length (Xnn)	Y1			1.05
Contact Pad to Center Pad (Xnn)	G1	1.28		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003793B (05-17-23)	Highlights	Updated cover bullets for clarity.
	Features	Removed the following items from Comprehensive Power Management features section: L1.off and L1.snooze.
	Section 1.1, General Description	Added the following sentence to the first paragraph: “The maximum line rate is 8GT/s and it is certified against the GEN4 compliance program as defined in the PCIe Revision 4.x specifications.”
	Figure 1-1	Updated port names for clarity.
DS00003793A (01-08-21)	All	Initial Release.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/	XXX
Device	Tape and Reel Option		Temperature Range		Package

Device:	PCI11010= PCIe Switch with Ethernet MAC, Prog. I/O	
Tape and Reel Option:	Blank T	= Standard packaging (tray) = Tape and Reel (Note 1)
Temperature Range:	Blank I	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial)
Package:	ZVX =	100-pin VQFN

Examples:

a) PCI11010/ZVX
Tray, 0°C to +70°C, 100-pin VQFN

b) PCI11010T/ZVX
Tape & reel, 0°C to +70°C, 100-pin VQFN

c) PCI11010-I/ZVX
Tray, -40°C to +85°C, 100-pin VQFN

d) PCI11010T-I/ZVX
Tape & reel, -40°C to +85°C, 100-pin VQFN

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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