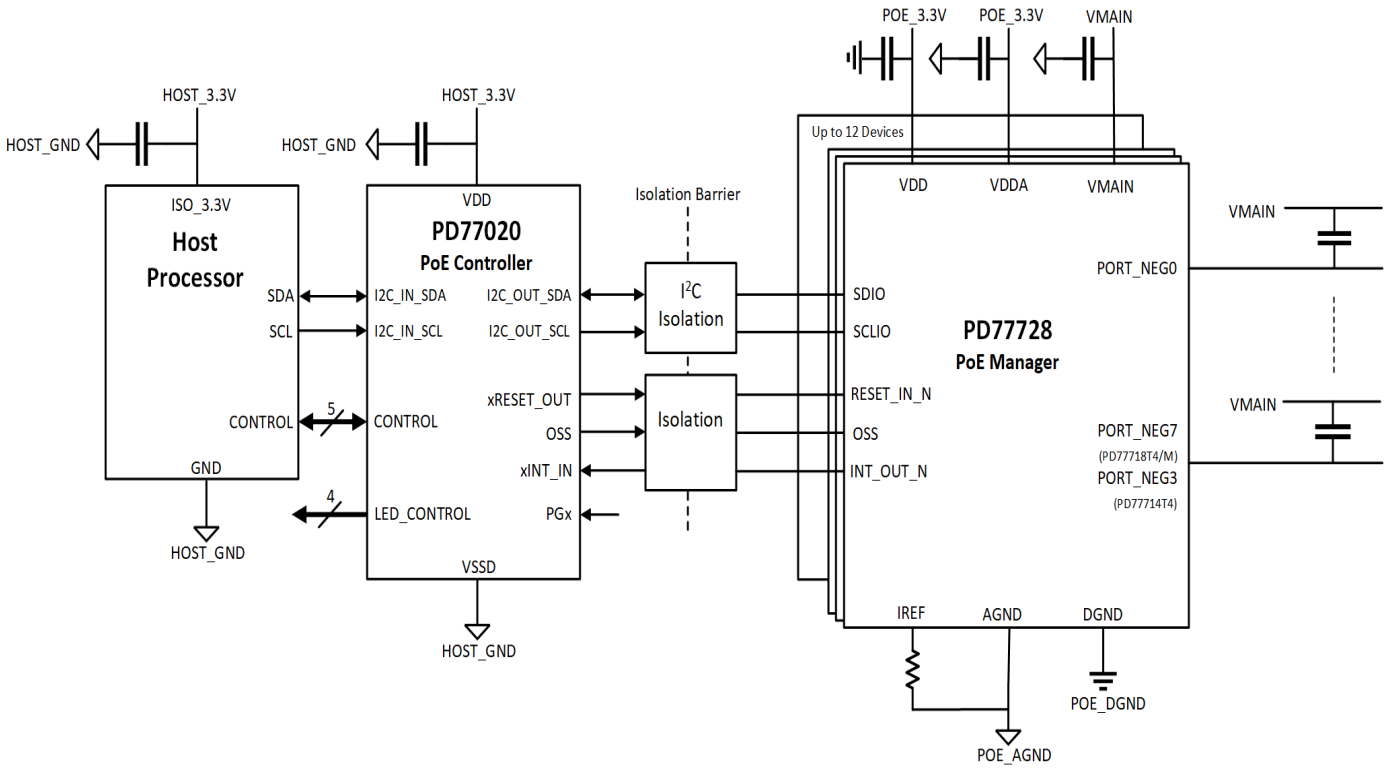
Introduction

The PD77020 PoE Power Management Controller provides multi-port PoE functions, such as, port mapping (Port Matrix), port priority, port status, and system power management. The PD77020 device can be used in conjunction with the PD77728 seventh generation PoE Manager from Microchip. The PD77020 device is based on a Microchip SAMD21 controller and is packaged in a 5 mm × 5 mm 32-pin QFN package.

The following figure shows a typical PoE application with PD77020.

Figure 1. Typical PoE Application with PD77020



Features

A PSE System operating in the Controller mode with PD777020 Controller and the PD77728 Manager has the following system and port level features:

- Detection
- Classification
- Inrush
- Port Power Up
- Real-Time Protection (RTP)
- Support for up to 16 Power Banks
- Power Management
  - Configure active ports (disabling unused ports)
  - Power up ports (based on detection/classification results)
  - Ports power down (based on power budget)
  - Autoclass
  - Power budgeting
  - Power Good pins to OSS translation
  - Power measurement
- Communication with Host (15-byte protocol)
  - System, Device, and Port Status
  - Temperature alarm
  - Reading chips temperature
- LLDP

Applications

- Switches and routers for enterprise, small and medium business, SOHO, and commercial markets.
- Switches and router for enterprise market.
- Switches for medium and small business, SOHO commercial markets.
- PoE injectors

Table of Contents

1. Application Information

This section provides practical operation information for a PSE based on the PD77728 and the PD77020 devices.

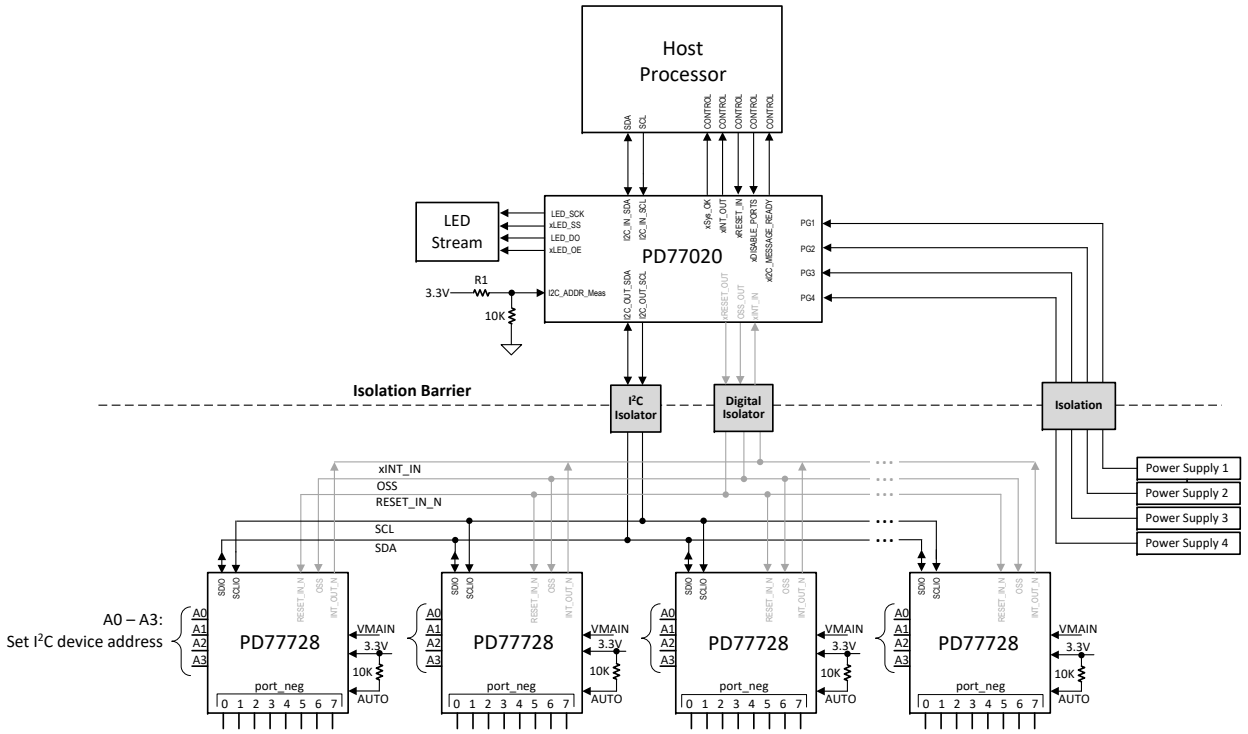
1.1 Controller Mode

This section provides a high-level description of the Controller Mode operation in a PSE based on the PD77728 and the PD77020 devices.

The PD77020 device is used in conjunction with the PD77728 devices to create an inclusive system, where the PD77020 PoE Power Management Controller provides high-level, sophisticated, and multi-port PoE functions, such as port mapping (Port Matrix), port priority, port status, and system power management.

The following figure shows the Controller mode operation.

Figure 1-1. Controller Mode Operation



2. Electrical Specifications

For the complete list of latest electrical specifications of the PD77020 device, see the *SAMD21 Family Data Sheet*.

2.1 Absolute Maximum Ratings

Stresses beyond those listed in this section might cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods might affect device reliability. The following table lists the absolute maximum ratings.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Power supply voltage	0	3.8	V
V_{PIN}	Pin voltage with respect to GND and V_{DD}	GND − 0.6V	V_{DD} + 0.6V	V
Lead soldering temperature (40s, reflow)	—	—	260	°C
Storage temperature	—	−60	150	°C

2.2 Immunity

The following table lists the immunity details of the PD77020 device.

Table 2-2. Immunity

Symbol	Parameter	Conditions	Min.	Max.	Units
ESD	ESD rating	HBM[1]	−2000	2000	V
		CDM[2]	−500	500	V

Notes:

1. ESD HBM complies with JESD22 Class 2 standard.
2. ESD CDM complies with JESD22 Class 1 standard.

2.3 Electrical Characteristics

The following table lists the general operating conditions for the PD77020 device.

Table 2-3. General Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{DD}	Power supply voltage	3.0	3.3	3.6	V
V_{DDA}	Power supply voltage	3.0	3.3	3.6	V
T_A	Temperature range	−40	25	85	°C
T_J	Junction temperature	—	—	100	°C

The following table lists the I/O characteristics of the PD77020 device.

Table 2-4. I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{PULL}	Internal Pull-up/Pull-down resistance	—	20	40	60	kΩ
V_{IL}	Input low-level voltage	V_{DD} = 3.0V–3.6V	—	—	0.3 × V_{DD}	V
V_{IH}	Input high-level voltage	V_{DD} = 3.0V–3.6V	0.55 × V_{DD}	—	—	
V_{OL}	Output low-level voltage	V_{DD} > 3.0V, I_{OL} maxI	—	0.1 × V_{DD}	0.2 × V_{DD}	
V_{OH}	Output high-level voltage	V_{DD} > 3.0V, I_{OH} maxII	0.8 × V_{DD}	0.9 × V_{DD}	—	
I_{OL}	Output low-level current	V_{DD} = 3V–3.63V	—	—	10	mA
I_{OH}	Output high-level current	V_{DD} = 3V–3.63V	—	—	7	mA
t_{RISE}	Rise time[1]	load = 20 pF, V_{DD} = 3.3V	—	—	15	ns
t_{FALL}	Fall time[1]	load = 20 pF, V_{DD} = 3.3V	—	—	15	ns
I_{LEAK}	Input leakage current	Pull-up resistors disabled	−1	±0.015	1	µA

Note:

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

The following table lists the I^2C pins characteristics of the PD77020 device.

Table 2-5. I^2C Pins Characteristics in I^2C Configuration

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input low-level voltage	V_{DD} = 3.0V–3.6V	—	—	0.3 × V_{DD}	V
V_{IH}	Input high-level voltage	V_{DD} = 3.0V–3.6V	0.55 × V_{DD}	—	—	
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.08 × V_{DD}	—	—	
V_{OL}	Output low-level voltage	V_{DD} > 3.0V, I_{OL} = 3 mA	—	—	0.4	
I_{OL}	Output low-level current	V_{OL} = 0.4V Fast Mode +	20	—	—	mA
f_{SCL}	SCL clock frequency		—	—	400	KHz

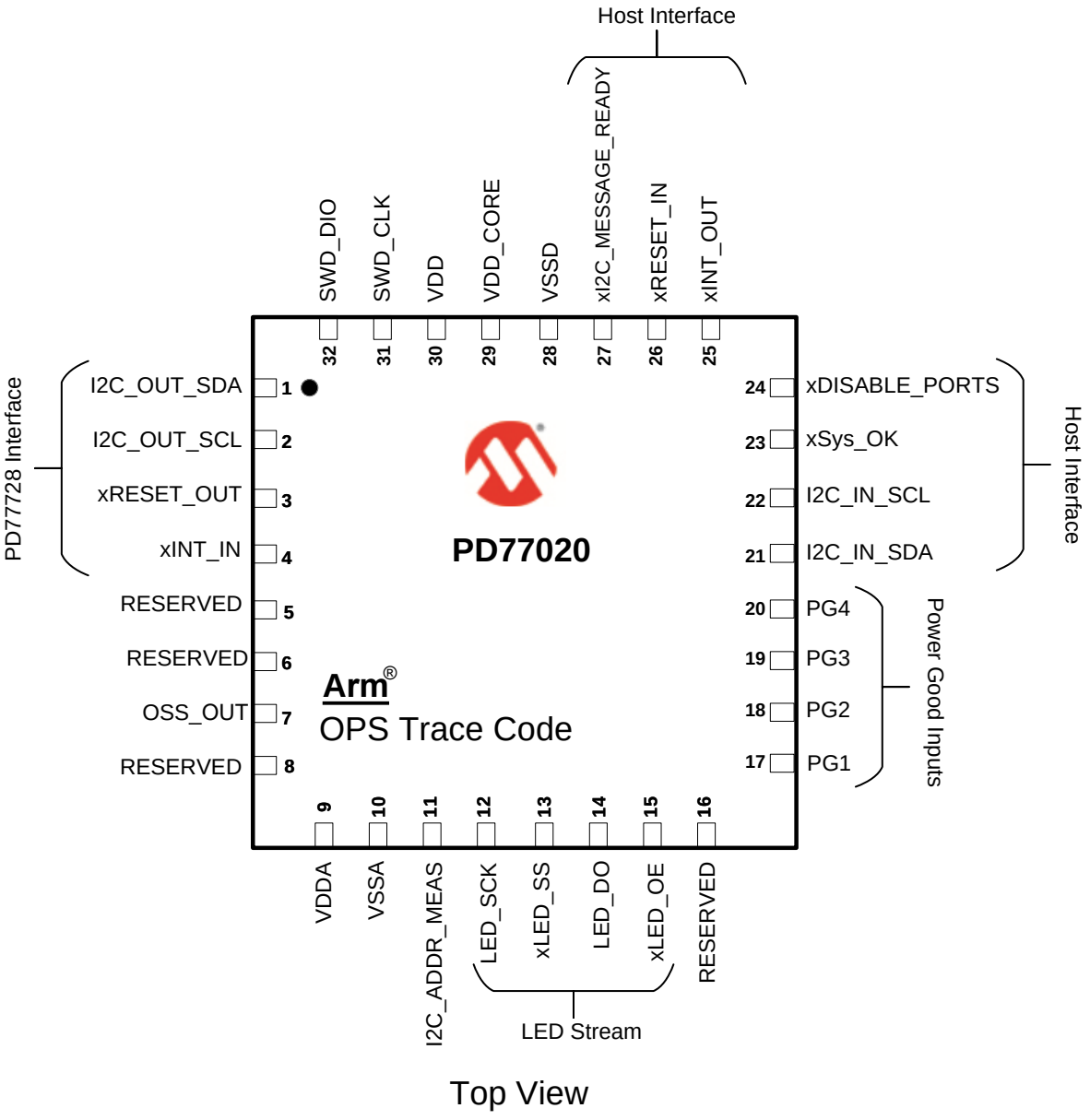
3. Pins

This section provides pin descriptions of the PD77020 device.

3.1 Pin Diagram

The following figure shows the pin diagram (top view) of the PD77020 device.

Figure 3-1. Pin Diagram



3.2 Pin Descriptions

The following table lists the functional pin descriptions of the PD77020 device.

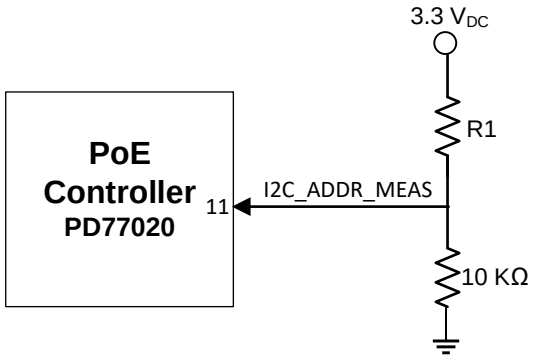
Table 3-1. PD77020 Pin Descriptions

PD77020	Designation	Type	Description
1	I2C_OUT_SDA	IN/OUT	I^2C bidirectional data to PD77728 devices It is required to add a 2 KΩ pull-up resistor.
2	I2C_OUT_SCL	OUT	I^2C SCL signal to PD77728 devices It is required to add a 2 KΩ pull-up resistor.
3	xRESET_OUT	OUT	Reset output (active low) to PD77728 devices
4	xINT_N	IN	An open-drain interrupt input from the common INT_OUT_N output from all the PD77728 devices This pin is active low. Connect a pull-up resistor to V_{DD}.
5	RESERVED	—	Unused, leave floating
6	RESERVED	—	Unused, leave floating
7	OSS_OUT	OUT	DATA output for OSS signaling to the PD77728 devices
8	RESERVED	—	Unused, leave floating
9	VDDA	Supply	Main supply 3.3V
10	VSSA	GND	Ground
11	I2C_ADDR_MEAS	Analog_IN	Analog input to determine the I^2C address See Figure 3-2 and Table 3-2 for details.
12	LED_SCK	OUT	LED stream Clock out
13	xLED_SS	OUT	LED stream Client-Select (active low)
14	LED_DO	OUT	LED stream Data out
15	xLED_OE	OUT	LED stream Output Enable (active low)
16	RESERVED	—	Unused, leave floating
17	PG1	IN	Power Good input 1
18	PG2	IN	Power Good input 2
19	PG3	IN	Power Good input 3
20	PG4	IN	Power Good input 4
21	I2C_IN_SDA	IN/OUT	I^2C bidirectional data 15-byte protocol messages are transmitted on this line. Pull-up required, see *AN4896* for details.
22	I2C_IN_SCL	IN	I^2C clock from the host master Speed is limited to 400 KHz. Pull-up required.
23	xSys_OK	OUT	System validity indication The behavior of this output is controlled by individual software mask (active low). This pin is a push-pull output.
24	xDISABLE_PORTS	IN	Disable all PoE ports. When this input is asserted low, the controller shuts down all PoE ports in the system. See *AN4896* for pin connection requirements (active low).
25	xINT_OUT	OUT	Interrupt output indication This line is asserted low when a pre-configured event is in progress (active low). This pin is an open-drain output with internal pull up.
26	xRESET_IN	IN	Host Reset input (active low)
27	xI2C_MESSAGE_READY	OUT	I^2C message ready indication to the host This signal is LOW when a message is ready to be read. I^2C read cycle must be invoked only if this signal is low. After reading the message, the pin is set high again, until next message is ready.

.....continued			
PD77020	**Designation**	**Type**	**Description**
28	VSSD	GND	Ground
29	VDD_CORE	Power	Internal 1.2V core voltage Connect 1 µF capacitor to VSSD.
30	VDD	Supply	Main 3.3V supply
31	SWD_CLK	SWD	Connect 1 kΩ pull-up to 3.3V.
32	SWD_DIO	SWD	Leave open
ePAD	ePAD	GND	Connect to VSSA. It must have sufficient copper mass to ensure adequate thermal performance.

The following figure shows the I²C address selection of the PD77020 PoE Controller.

Figure 3-2. I²C Address Selection



The following table lists the specific value of R to choose I²C and set the address.

Table 3-2. I²C Address Selection

I²C Address (Hexadecimal)	R1–KΩ (1%)
0x4	147
0x8	86.6
0xC	57.6
0x10	43.2
0x14	34
0x18	26.7
0x1C	22.1
0x20	18.2
0x24	15.4
0x28	13
0x2C	11
0x30	9.31
0x34	7.87
0x38	6.49
0x3C	5.49

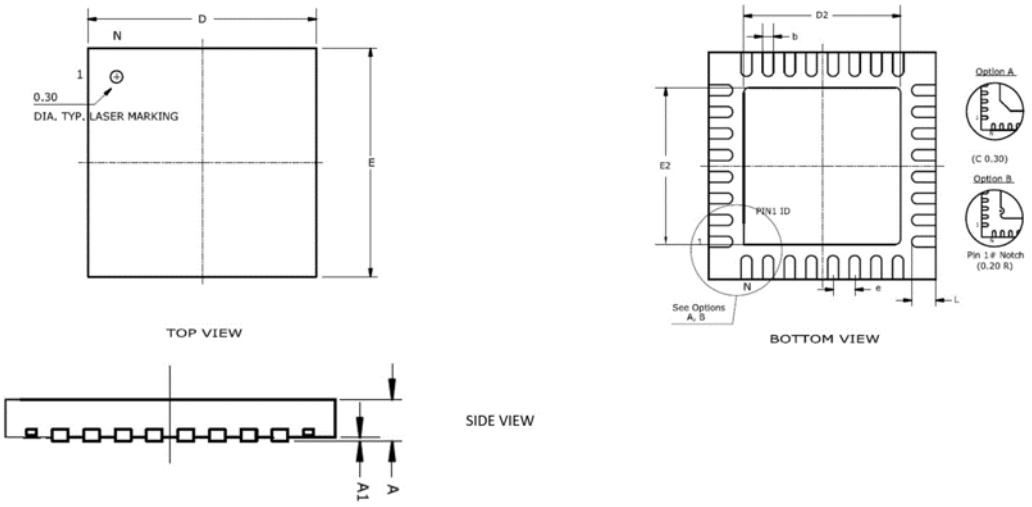
4. Package Information

This section provides the package information for the PD77020 device.

4.1 PD77020 Package Outline Drawing

The following figure shows the package drawing of the PD77020 device.

Figure 4-1. PD77020 Package Outline Drawing (32 Pin QFN 5 mm × 5 mm)



The following table lists the dimensions and measurements of the PD77020 package.

Table 4-1. PD77020 Package Outline Dimensions and Measurements

Dimension	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
e	0.50 BSC	—	0.02 BSC	—
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	3.50	3.70	0.138	0.147
E2	3.50	3.70	0.138	0.147
D	5.00 BSC	—	0.197 BSC	—
E	5.00 BSC	—	0.197 BSC	—

Note: Dimensions do not include protrusions; they must not exceed 0.155 mm (0.006 inch) on any side. Lead dimension must not include solder coverage. Dimensions are in millimeters and inches for reference.

4.2 Thermal Specifications

The following table lists the thermal specifications of the PD77020 device.

Table 4-2. Thermal Specifications

Thermal Resistance	Device	Typ.	Units	Description
θ_{JA}	PD77020	40.9	°C/W	Junction-to-ambient thermal resistance.
θ_{JC}	PD77020	15.2	°C/W	Junction-to-case thermal resistance.

4.3 Recommended PCB Layout

The following figures show the recommended PCB layout pattern for the PD77020 32-pin QFN 5 mm × 5 mm. Units are in mm.

Figure 4-2. PD77020 Solder Mask

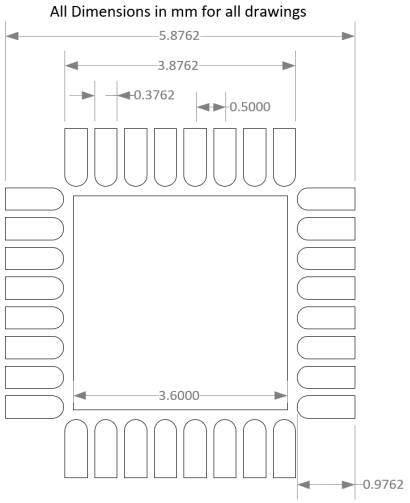


Figure 4-3. PD77020 Top-Layer Copper

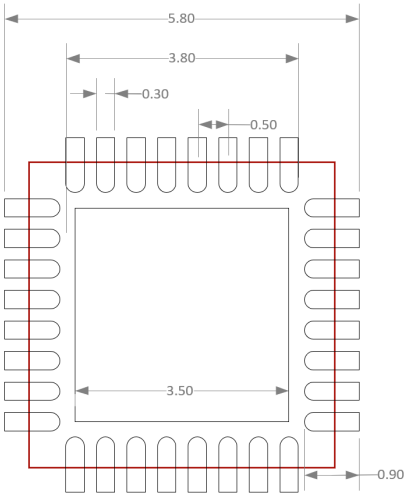
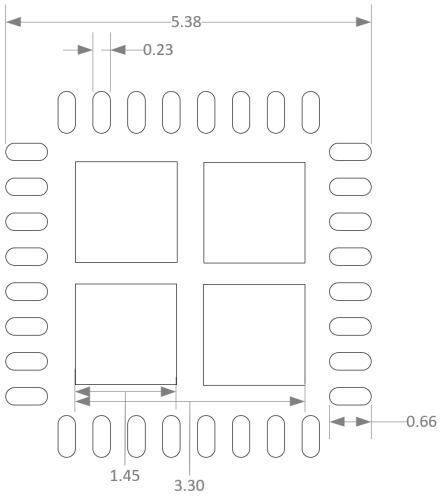


Figure 4-4. PD77020 Paste Mask



Note: The contract manufacturer has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil covers 65% to 80% of the thermal pad and must not allow solder to be applied to the thermal vias under the QFN package using any method they deem appropriate. Any design must be subject to system validation and qualification prior to commitment to mass production of field deployment. Use a 5 mil stencil.

4.4 Recommended Solder Reflow Information

The recommended solder reflow information is as follows:

- RoHS 6/6
- Pb-free 100% Matte Tin Finish
- Package Peak Temperature for Solder Reflow (40s maximum exposure)—260 °C (0 °C, −5 °C)

The following figures and tables show the classification reflow profiles and temperatures.

Table 4-3. Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TS_{max} to Tp)	3 °C/s maximum	3 °C/s maximum
Preheat		
Temperature min (TS_{min})	100 °C	150 °C
Temperature max (TS_{max})	150 °C	200 °C
Time (ts_{min} to ts_{max})	60s to 120s	60s to 180s
Time Maintained		
Temperature (T_L)	183 °C	217 °C
Time (t_L)	60s to 150s	60s to 150s
Peak classification temperature (TP)	210 °C to 235 °C	240 °C to 255 °C
Time within 5 °C of actual peak temperature (tp)	10s to 30s	20s to 40s
Ramp-down rate	6 °C/s maximum	6 °C/s maximum
Time 25 °C to peak temperature	6 minutes maximum	8 minutes maximum

Figure 4-5. Classification Reflow Profiles

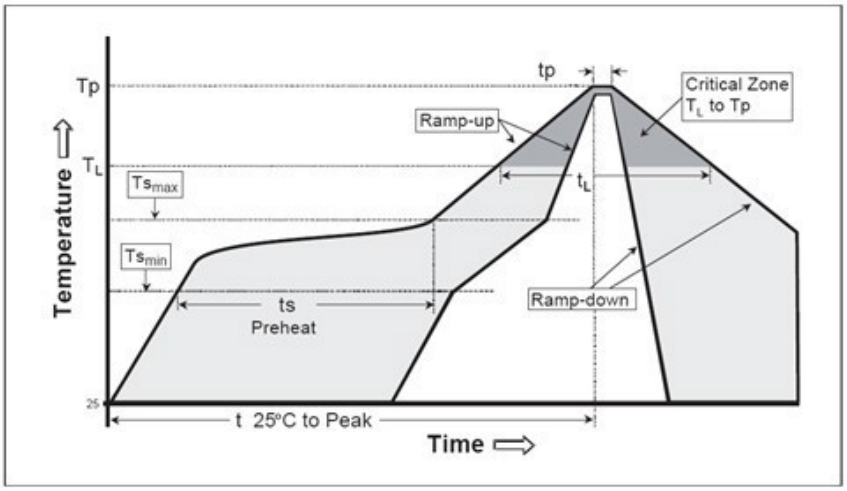


Table 4-4. Pb-Free Process—Package Classification Reflow Temperatures

Package Thickness	Volume < 350 mm^3	Volume 350–2000 mm^3	Volume > 2000 mm^3
Less than 1.6 mm[1]	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6 mm to 2.5 mm[1]	260 + 0 °C	250 + 0 °C	245 + 0 °C
Greater than or equal to 2.5 mm[1]	250 + 0 °C	245 + 0 °C	245 + 0 °C

Note:

1. Tolerance: The device manufacturer or supplier must assure process compatibility up to and including the stated classification temperature, that is, the Peak reflow temperature is 0 °C. For example, 260 °C to 0 °C, at the rated MSL value.

Exceeding the ratings that are mentioned in the preceding table might cause damage to the device.

5. Ordering Information

The following table lists the part ordering information of the PD77020 device.

Table 5-1. Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking
PD77020-VVVV[2]SS[3]-TR	Plastic QFN 5 mm × 5 mm (32 lead)	Tape and Reel	−40 °C to 85 °C	Microchip Logo PD77020 e3 Arm® YYWWNNN[1]
PD77020-VVVV[2]SS[3]	Plastic QFN 5 mm × 5 mm (32 lead)	Tray	−40 °C to 85 °C	Microchip Logo PD77020 e3 Arm YYWWNNN[1]

Notes:

1. YY= Year; WW= Week; and NNN= Trace code
2. VVVV = Firmware revision
3. SS = Firmware parameters options

6. Reference Documents

This data sheet has the following reference documents:

- *PD77728 8-Port PoE PSE Controller/Manager Data Sheet*
- *AN4896 Designing an IEEE® 802.3bt/at/af PoE System Based on PD77728*
- *AN4813 Surge Protection for Systems Based on PD77728 8-Port PSE PoE Controller/Manager*
- *PD77728 Auto Mode Register Map*
- *AN4952 PD77728 PSE Firmware Download and Replace Flow*
- *PD77728 Auto Mode Evaluation Board User Guide*

7. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 7-1. Revision History

Revision	Date	Description
B	01/2025	The following changes were made in Revision B of this document: • Updated the following figures: – Figure 1. Typical PoE Application with PD77020 – Figure 1-1. Controller Mode Operation
A	08/2023	Initial revision

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