A Product Line of Diodes Incorporated

PI3EQX10312

# 10Gbps, 2-Port, USB 3.1 Mux/Demux ReDriver™ with Integrated USB-C Detector

## Description

PI3EQX10312 is a low-power, high-performance 10Gbps 2-Port USB 3.1 Gen-2/Gen-1 Mux/DeMux ReDriver with Plug-in Detector for Type-C connector.

The device includes two main function blocks:

1) The 2 Port Mux/DeMux ReDriver
2) The Plug-in Detector for USB-C Connector

### The 2 Port Mux/Demux ReDriver

The ReDriver provides programmable equalization, swing, and flat gain to optimize performance over a variety of physical mediums by reducing intersymbol interference. The ReDriver supports two 100Ω differential CML data I/Os between the protocol ASIC to a switch fabric, over cable, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver. A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. The channels' input signal level determines whether the output is active.

The ReDriver also includes an adaptive power management feature to maximize battery life for power-sensitive consumer devices.

### The Plug-in Detector for USB-C Connector

The plug-in detector detects the plug-in orientation of the cable at a USB-C connector. It supports the port to configure as SOURCE mode, SINK mode, and DRP modes and automatically connects based on the voltage levels detected on CC pin. It is a fully-integrated solution with ultra-low power dissipation.

The plug-in detector supports both pin and I2C control based on ADDR1 pin setting. It allows the system to choose between pin control and I2C control mode.

In pin control mode, the PORT0 and PORT1 input pins determine the port setting in which the SOURCE, SINK, or DRP port can be selected. In SOURCE and DRP modes, the SRC_CUR input pin selects USB Type-C current advertisement at default USB, 1.5A, and 3A level. The system running in source mode can monitor ID pin to know the connector attached or not. Systems running in SINK mode can monitor system's VBUS for connector status as well as OUT1, and OUT2 for host's charging profile capability. DEBUG and OUT3 pins also indicate if a debug or audio accessory is attached.

The plug-in detector provides VCONN function to power active cables and other accessories through VCONN pin. Low-resistance power switches are integrated in the chip-to-connect CC1/CC2 pins to VCONN pin.

Enabling I2C control **mode allows** high flexibility for port control and communications through registers read/write. An interrupt signal for indicating changes with the I2C registers is sent to the master to notify the system any change in the **USB**-C connector while in parallel the system can still monitor ID pin.

## Features

**ReDriver**

- 10Gbps Serial Link with Linear Equalizer
- Full Compliancy to USB 3.1 Gen-2 and Gen-1 Super-Speed Standard
- 1-to-2 DeMux from Host Tx to Device Rx
- 2-to-1 Mux from Device Tx to Host Rx
- Adjustable Output Linear Swing, Flat Gain and Equalization via I2C or Pin Control
- 100Ω Differential CML I/Os
- Automatic Receiver Detect
- Auto "Slumber" Mode for Adaptive Power Management
- Supply Voltage 3.3V

**Plug-in Detector**

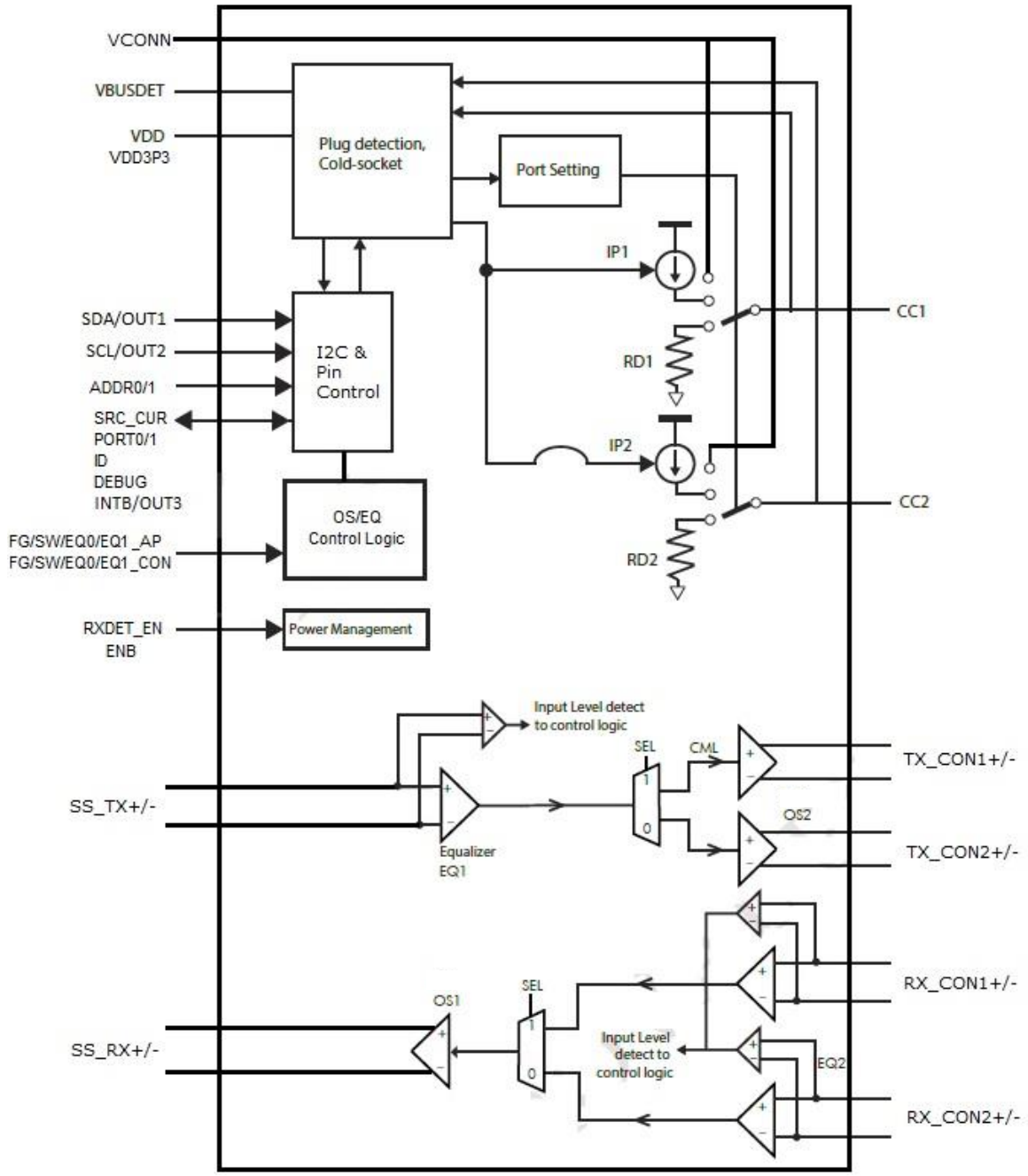
- USB Type-C Specification 1.3
- Supports SOURCE/SINK/DRP Modes
- Support DRP Modes with Try.SNK/Try.SRC
- Auto-Configure Ports Orientation through CC Detection
- Supports VCONN to Power Active Cables and Other Accessories
- Supports Overcurrent Protection and Overvoltage Protection for VCONN
- Allow Both Pin Control and I2C Interface
- Integrated Power Switches, High-Precision Resistors and Current Sources for CC Pins
- Provides Support for Default USB Power, 1.5A, and 3A SOURCE Modes with I2C Control and Pin Control
- Output Indicator for Plug-in Detection
- Power-Saving Mode
- 24V Tolerance on CC1, CC2 and VBUSDET
- Power Supply Range: 3.0V to 5.0V
- Temperature Range: -40°C to 70°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Packaging (Pb-free & Green):
  – 42-contact, ZH42 (3.5mm × 9mm)

## Application(s)

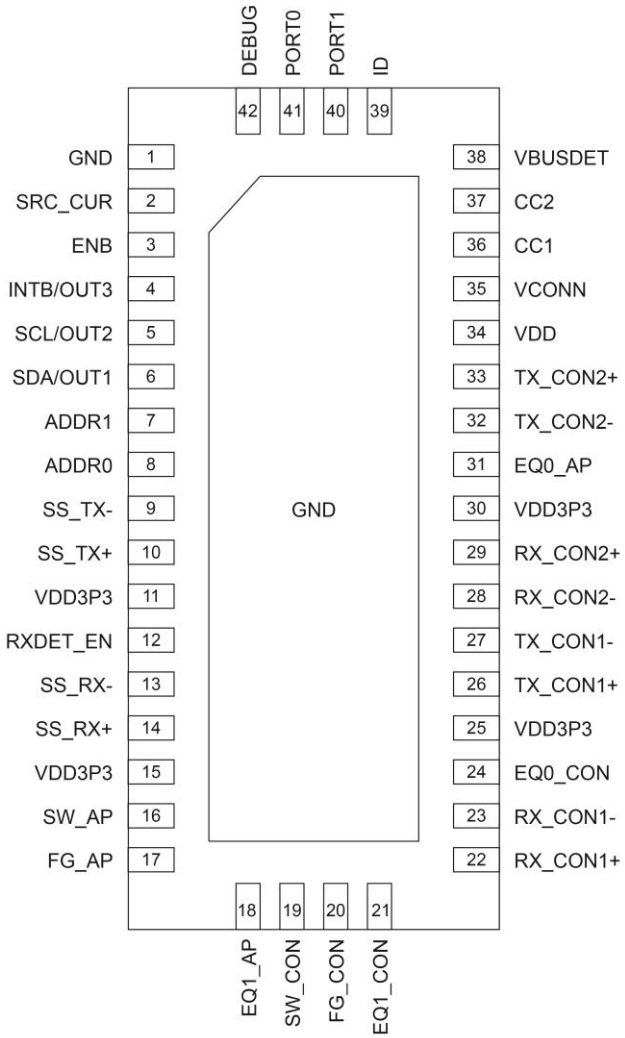
- Notebooks
- Mobile Phones
- Tablets
- Docking Station

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Block Diagram



## Pin Configuration

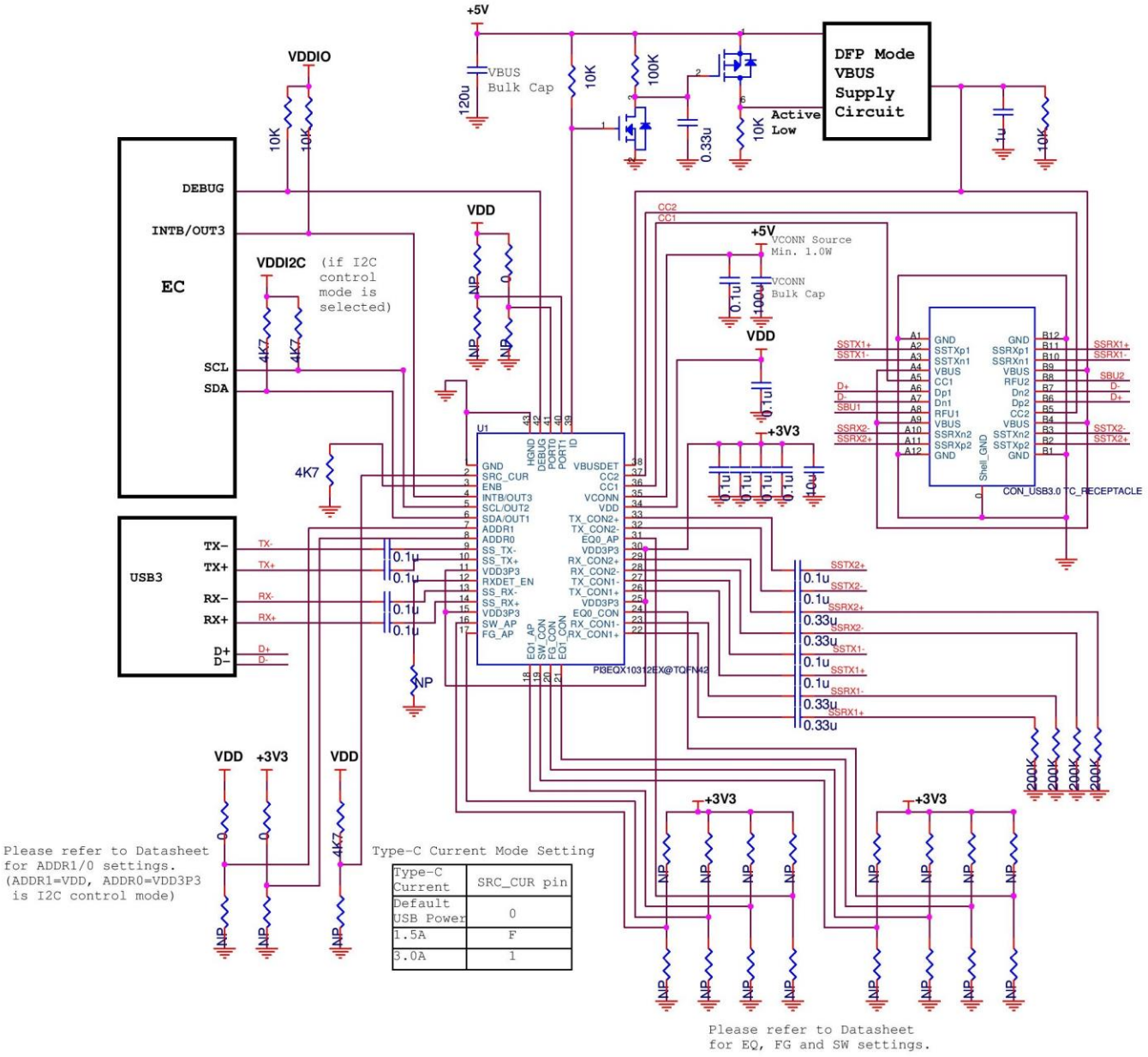



## Pin Descriptions

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 1, Thermal PAD | GND | Ground | Ground pin. Thermal Pad. |
| 2 | SRC_CUR | I | Tri-level input pin to indicate SOURCE current mode (for pin control only):<br>PORT=floating – SOURCE 1.5A current mode;<br>PORT=VDD – SOURCE 3A current mode;<br>PORT=GND – SOURCE Default current mode |
| 3 | ENB | I | Active-low enable input pin (with internal weak pull high):<br>ENB=VDD – Disabled/Low Power State<br>ENB=GND – Enabled/Active State |
| 4 | INTB/OUT3 | O | Open-drain output. In I2C control mode, this is an active LOW interrupt signal for indicating changes in I2C registers. |

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| | | | Dual function as analog audio-adapter detection in pin control mode:<br>OUT3=Hi-Z – Not detected;<br>OUT3=Low – Analog audio adapter detected |
| 5 | SCL/OUT2 | I/O | I2C communication clk signal.<br>Dual function as open-drain Type-C Current Mode Detected in pin control mode when port is a SINK;<br>OUT2 OUT1 Current Mode<br>Hi-Z Hi-Z Default<br>Hi-Z Low Medium<br>Low Low High |
| 6 | SDA/OUT1 | I/O | $I^2C$ communication data signal.<br>Dual function as open-drain Type-C Current Mode Detected in pin control mode when port is a SINK;<br>OUT2 OUT1 Current Mode<br>Hi-Z Hi-Z Default<br>Hi-Z Low Medium<br>Low Low High |
| 7, 8 | ADDR1, ADDR0 | I | Multi-level input pins to indicate $I^2C$ address or pin control mode of USB-C Detector and ReDriver:<br>Please refer to Table of $I^2C$ Slave Address. |
| 10, 9<br>22, 23<br>29, 28 | SS_TX+, SS_TX-,<br>RX_CON1+, RX_CON1-,<br>RX_CON2+, RX_CON2- | I | Input terminals. With selectable input termination between 50Ω to VDD, 75kΩ to VbiasRX, or 75kΩ to GND. |
| 11, 15, 25, 30 | VDD3p3 | Power | Dedicated 3.3V Power Supply. |
| 12 | RXDET_EN | I | ReDriver Loading Detection Enable Pin:<br>1 = ReDriver Loading Detection Enabled (Default Setting in Application)<br>0 = ReDriver Loading Detection Disabled |
| 14, 13<br>26, 27<br>33, 32 | SS_RX+,SS_RX-,<br>TX_CON1+,TX_CON1-,<br>TX_CON2+, TX_CON2- | O | Output terminals. With selectable output termination between 50Ω to VbiasTx, 6kΩ to VbiasTx, 75kΩ to VbiasTx, and 75kΩ to GND. |
| 16, 17, 18, 31 | SW_AP<br>FG_AP<br>EQ1_AP, EQ0_AP | I | SW/FG/EQ setup for USB channels with receiver terminal is connected to AP Side. |
| 19, 20, 21, 24 | SW_CON<br>FG_CON<br>EQ1_CON, EQ0_CON | I | SW/FG/EQ setup for USB channels with receiver terminal is connected to Connector Side. |
| 34 | VDD | Power | Positive supply voltage from VBAT. |
| 35 | VCONN | Power | Supply voltage for VCONN. |
| 36 | CC1 | I/O | Type-C configuration channel 1 signal. |
| 37 | CC2 | I/O | Type-C configuration channel 2 signal. |
| 38 | VBUSDET | I | VBUS detection. |
| 39 | ID | O | Open-drain output. Asserted low when CC pin detected device attachment when port is a Host (or dual-role acting as Host), otherwise ID is hi-z. |
| 40, 41 | PORT1,PORT0 | I | Tri-level input pins to indicate port mode (for pin control only). |
| 42 | DEBUG | O | Open drain output for Debug Accessory Detection.<br>Open drain output. Asserted low when CC pin detected Debug Accessory attachment; otherwise, DEBUG pin is Hi-Z. |

## Application Schematic



## Maximum Ratings

| | | |
|---|---|---|
| Storage Temperature | -65 to 150 | ℃ |
| Battery Supply Voltage | -0.5 to 6 | V |
| 3.3V Supply Voltage | -0.5 to 3.8 | V |
| System VBUS Voltage Detection | -0.5 to 24 | V |
| VCONN Supply Voltage Range | -0.5 to 6 | V |
| CC1, CC2 Input Voltage | -0.5 to 24 | V |
| Voltage of IO Pins (ENB, ADDR1, PORT1,PORT0 SRC_CUR, INTB/OUT3, ID, DEBUG) | -0.5 to 6 | V |
| Voltage of 3.3V IO Pins (SCL/OUT2, SDA/OUT1, RXDET_EN, ADDR0, SW_AP,FG_AP, EQ1_AP, EQ0_AP,SW_CON,FG_CON, EQ1_CON,EQ0_CON) | -0.5 to VDD3P3+0.5 | V |
| Voltage of SS_TX+/-,SS_RX+/-,TX_CON1/2 +/-, RX_CON1/2 +/- | -0.5 to VDD3P3+0.5 | V |
| Output Current from CC1, CC2 | Internally Limited | — |
| Sink Current from CC1, CC2 | 30 | mA |
| Sink Current from ID, DEBUG, INTB/OUT3, SCL/OUT2, SDA/OUT1 | 10 | mA |
| Continuous Input Current to SS_TX+/-, RX_CON1/2 +/- | ±30 | mA |
| ESD (HBM) | 2KV | — |

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operation Conditions

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{DD}$ | Battery Supply Voltage | 3.0 | 5.5 | V |
| $V_{DD3P3}$ | 3.3V Supply Voltage | 3.0 | 3.6 | V |
| $V_{BUSDET}$ | System VBUS Voltage Detection | 0 | 22 | V |
| $V_{BAT\_TH}$ | Battery Supply Undervoltage Lockout | 2.2 | 2.65 | V |
| $V_{CONN}$ | VCONN Supply Voltage Range | 2.7 | 5.5 | V |
| $V_{IN\_CC12}$ | CC1, CC2 Input Voltage | 0 | 5.5 | V |
| $V_{IO}$ | Voltage of IO pins (ENB, ADDR1, PORT1,PORT0 SRC_CUR, INTB /OUT3, ID, DEBUG) | 0 | 5.5 | V |
| $V_{IO3P3}$ | Voltage of 3.3V IO pins (SCL/OUT2, SDA/OUT1, RXDET_EN, ADDR0, SW_AP,FG_AP, EQ1_AP, EQ0_AP, SW_CON, FG_CON, EQ1_CON, EQ0_CON) | 0 | 3.6 | V |
| $V_{TXRX}$ | Voltage of SS_TX+/-,SS_RX+/-,TX_CON1/2 +/-, RX_CON1/2 +/- | 0 | 3.6 | V |
| $V_{NOISE}$ | Supply Noise up to 50MHz | — | 100 | mVpp |
| $T_A$ | Operating Temperature | -40 | 70 | °C |

## USB-C Detector DC Electrical Characteristics

Min and Max apply for $T_A$ between -40°C to 85°C (unless otherwise noted). Typical values are referenced to $V_{DD}$=3.6V, $T_A$=+25°C

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **CC1/CC2 Configuration (Device Mode, SNK)** | | | | | | |
| $R_D$ | Device Mode Pulldown Resistor | — | 4.6 | 5.1 | 5.6 | kΩ |
| $V_{TH3\_SNK}$ | High Current Mode Entry Threshold | — | 1.16 | 1.23 | 1.31 | V |
| $V_{TH2\_SNK}$ | Medium Current Mode Entry Threshold | — | 0.61 | 0.66 | 0.70 | V |
| $V_{TH1\_SNK}$ | Default Current Mode Entry Threshold | — | 0.15 | 0.2 | 0.25 | V |
| **CC1/CC2 Configuration (Host Mode, SRC)** | | | | | | |
| $I_P$ | Host Mode Pullup Current Source | Default current mode | 64 | 80 | 96 | µA |
| | | Medium current mode (1.5A) | 166 | 180 | 194 | |
| | | High current mode (3A) | 304 | 330 | 356 | |
| $V_{OPEN}$ | CC Open Voltage | $V_{DD}$ = 2.7V to 5.5V Default/Medium/High current mode | 2.6 | — | — | V |
| **CC1/CC2 Configuration (DRP)** | | | | | | |
| $t_{DRP}$ | The Period a DRP Shall Complete a Source to Sink and Back Advertisement | $V_{DD}$ = 3.6V | 50 | 75 | 100 | ms |
| **VBUS Detection** | | | | | | |
| $V_{VBUS}$ | VBUS Detection Threshold (Rising) | — | 1.7 | 2.2 | 2.7 | V |
| | VBUS Detection Hysteresis | — | — | 0.1 | — | V |
| **VCONN** | | | | | | |
| $R_{VCONN}$ | VCONN Switch On-Resistance | $I_{LOAD}$ = -100mA, $V_{CONN}$ = 5V | — | 1 | — | Ω |
| $I_{VCONN}$ @80% $V_{CONN}$ | VCONN Output Current at 80% VCONN | $V_{CONN}$ = 5V, Vcc1 or Vcc2 = 4V | 500 | 570 | 650 | mA |
| $V_{OVP}$ | CC1 & CC2 Overvoltage Protection | — | 5.5 | 6.0 | 6.5 | V |
| $I_{OVP}$ | Sink Current into CC1 or CC2 During OVP | $V_{CC1}$ or $V_{CC2}$ = 14V, $V_{DD}$ = 3.6V, ENB = 3.6V | — | — | 13 | mA |
| | | $V_{CC1}$ or $V_{CC2}$ = 24V, $V_{DD}$ = 3.6V, ENB = 3.6V | — | — | 30 | |
| **Host Interface Pins (SDA/OUT1, SCL/OUT2, INTB/OUT3, DEBUG, ID)** | | | | | | |
| $V_{OL}$ | Output Low Voltage at 3mA Sink Current (Open-Drain) | — | 0 | — | 0.4 | V |
| $I_{OFF}$ | Off-State Leakage Current | — | — | — | 1 | µA |
| **Input Control Pins (ENB, SDA/OUT1, SCL/OUT2)** | | | | | | |
| $V_{IH}$ | High-Level Input Voltage | — | 1.05 | — | — | V |
| $V_{IL}$ | Low-Level Input Voltage | — | — | — | 0.4 | V |
| $I_{IH\_LOGIC}$ | High-Level Input Current | Pin = $V_{DD}$ | -1 | — | 1 | µA |
| $I_{IL\_LOGIC}$ | Low-Level Input Current | Pin = 0V | -1 | — | 1 | µA |
| **Tri-State Input Control Pins (PORT1, PORT0, SRC_CUR)** | | | | | | |
| $V3_{IH}$ | High-Level Input Voltage | — | VDD-0.4 | — | — | V |
| $V3_{IL}$ | Low-Level Input Voltage | — | — | — | 0.4 | V |
| $I_{IH\_3STATE}$ | High-Level Input Current | Pin = $V_{DD}$ | -5 | — | 5 | µA |
| $I_{IL\_3STATE}$ | Low-Level Input Current | Pin = 0V | -5 | — | 5 | µA |
| **ADDR1 Pin** | | | | | | |
| | Resistor to GND (Pin Control Mode) | — | — | — | 100 | Ω |
| | Resistor to GND (I2C Address 1010101X) | — | 7.79K | 8.2K | 8.61K | Ω |
| | Resistor to GND (I2C Address 1110101X) | — | 15.2K | 16K | 16.8K | Ω |
| | Resistor to GND (I2C Address 1000101X) | — | 22.8K | 24K | 25.2K | Ω |
| | Resistor to VDD (I2C Address 1100101X) | — | — | — | 100 | Ω |

| | | | | | | |
|---|---|---|---|---|---|---|
| **VDD Current Consumption** | | | | | | |
| $I_{DD}$ | Operating Current, Device Mode | $V_{DD}$ = 3.6V,SNK connects to SRC | — | 40 | 65 | µA |
| | Operating Current, Host Mode | $V_{DD}$ = 3.6V,SRC Connects to SNK Default Current Mode | — | 150 | 200 | µA |
| $I_{DEV\_STBY}$ | Device Mode Standby Current | $V_{DD}$ = 3.6V, Floating CC1 and CC2 | — | 40 | 65 | µA |
| $I_{DUAL\_STBY}$ | Dual-Role Mode Standby Current | $V_{DD}$ = 3.6V, Floating CC1 and CC2 | — | 55 | 80 | µA |
| $I_{HOST\_STBY}$ | Host Mode Standby Current | $V_{DD}$ = 3.6V, Floating CC1 and CC2 | — | 70 | 95 | µA |
| $I_{DISABLE}$ | Chip is Disabled | ENB=VDD | — | — | 5 | µA |
| $I_{PWRSAVING}$ | Chip is in Power Saving Mode | Bit [7] of Control Register (01H)=1 | — | — | 40 | µA |
| **Thermal Shutdown** | | | | | | |
| $T_{OTP}$ | Thermal Shutdown Threshold | — | — | 155 | — | °C |
| $T_{hys}$ | Thermal Shutdown Hysteresis | — | — | 20 | — | °C |

## ReDriver AC/DC Electrical Characteristics

### Power Consumption (VDD3P3)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{PD}$ | Typical Pin Power Down Current | USB-C is Unattached | — | 26 | 100 | µA |
| $I_{DDQ\_PD}$ | I2C Power Down Current | USB-C is Attached<br>I2C Byte4<7:4>=1111 | — | — | 340 | µA |
| **USB 3.1 Gen 2 Mode** | | | | | | |
| $I_{U0}$ | Current in USB U0 Mode | USB U0 Mode | — | 80 | 112 | mA |
| $I_{U1}$ | Current in USB U1 Mode | USB U1 Mode | — | 16 | 20 | mA |
| $I_{U2/U3}$ | Current in USB U2/U3 Mode | USB U2/U3 Mode | — | 0.5 | 0.6 | mA |
| $I_{RXDET}$ | Current RXDET Mode | RXDET Mode | — | 0.5 | 0.6 | mA |
| **4-level control pins (FG_AP, FG_CON, EQ1_AP, EQ0_AP, EQ1_CON,EQ0_CON)** | | | | | | |
| $V_{IH}$ | DC INPUT LOGIC HIGH | — | 0.92×VDD3P3 | VDD3P3 | — | V |
| $V_{IF}$ | DC Input Logic “Float” | — | 0.59×VDD3P3 | 0.67×VDD3P3 | 0.75×VDD3P3 | V |
| $V_{IR}$ | DC Input Logic with Rext to GND | — | 0.25×VDD3P3 | 0.33×VDD3P3 | 0.41×VDD3P3 | V |
| $V_{IL}$ | DC Input Logic Low | — | — | GND | 0.08×VDD3P3 | V |
| $I_{IH}$ | Input High Current | — | — | — | 50 | µA |
| $I_{IL}$ | Input Low Current | — | -75 | — | — | µA |
| Rext | External Resistance Connects to GND (±5%) | — | 64.6 | 68 | 71.4 | kΩ |
| **2-level control pins (ADDR0, RXDET_EN, SW_AP, SW_CON)** | | | | | | |
| $V_{IH}$ | DC Input Logic High | — | 2.0 | — | — | V |
| $V_{IL}$ | DC Input Logic Low | — | — | — | 0.8 | V |
| $I_{IH}$ | Input High Current | — | — | — | 25 | µA |
| $I_{IL}$ | Input Low Current | — | -25 | — | — | µA |

### USB Differential Channel

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **USB Differential Input** | | | | | | |
| $C_{RXPARASITIC}$ | The Parasitic Capacitor for RX | — | — | — | 1.0 | pF |
| $R_{RX-DIFF-DC}$ | DC Differential Input Impedance | — | 72 | | 120 | Ω |
| $R_{RX-SINGLE-DC}$ | DC Single-ended Input Impedance | DC impedance limits are required to guarantee RxDet.<br>Measured with respect to GND over a voltage of 500mV max. | 18 | — | 30 | Ω |
| $Z_{RX-HIZ-DC-PD}$ | DC Input CM Input Impedance for V>0 During Reset or Power Down | (Vcm = 0 to 500mV) | 25 | — | — | kΩ |
| $C_{AC\_COUPLING}$ | AC Coupling Capacitance | — | 75 | — | 265 | nF |
| $V_{RX-CM-AC-P}$ | Common Mode Peak Voltage | AV up to 5GHz | — | — | 150 | mVpeak |
| $V_{RX-CM-DC-Active-Idle-Delta-P}$ | Common Mode Peak Voltage | Between U0 and U1,<br>Active up to 5GHz | — | — | 200 | mVpeak |
| **USB Differential Output** | | | | | | |
| $V_{TX-DIFF-PP}$ | Output Differential p-p Voltage Swing | Differential Swing $\|V_{TX-D+}-V_{TX-D-}\|$ | — | — | 1.2 | Vppd |
| $R_{TX-DIFF-DC}$ | DC Differential TX Impedance | — | 72 | — | 120 | Ω |
| $V_{TX-RCV-DET}$ | The Amount of Voltage Change Allowed During RxDet | — | — | — | 600 | mV |
| $C_{ac\_coupling}$ | AC Coupling Capacitance | — | 75 | — | 265 | nF |
| $T_{TX-EYE(10Gbps)}$ | Transmitter eye, Include all Jitter | At the silicon pad; 10Gbps | 0.646 | — | — | UI |
| $T_{TX-EYE(5Gbps)}$ | Transmitter eye, Include all Jitter | At the silicon pad; 5Gbps | 0.625 | — | — | UI |
| $T_{TX-DJ-DD(10Gbps)}$ | Transmitter Deterministic Jitter | At the silicon pad; 10Gbps | — | — | 0.17 | UI |
| $T_{TX-DJ-DD(5Gbps)}$ | Transmitter Deterministic Jitter | At the silicon pad; 5Gbps | — | — | 0.205 | UI |
| $C_{TXPARASITIC}$ | The Parasitic Capacitor for TX | — | — | — | 1.1 | pF |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $R_{TX-DC-CM}$ | Common Mode DC Output Impedance | — | 18 | — | 30 | Ω |
| $V_{TX-DC-CM}$ | The Instantaneous Allowed DC Common Mode Voltage at the Connector Side of the AC Coupling Capacitors | $\|V_{TX-D+}+V_{TX-D-}\|/2$ | 0 | — | 2.2 | V |
| $V_{TX-C}$ | Common-Mode Voltage | $\|V_{TX-D+}+V_{TX-D-}\|/2$ | VDD-2V | — | VDD | V |
| $V_{TX-CM-AC-PP-Active}$ | Active Mode TX AC Common Mode Voltage | $V_{TX-D+}+V_{TX-D-}$ for both time and amplitude | — | — | 100 | mVpp |
| $V_{TX-CM-DC-Active\_Idle-Delta}$ | Common Mode Delta Voltage $\|Avg_{uo}(\|V_{TEX-D+} + V_{TX-D-}\|)/2 - Avg_{u1}(\|V_{TX-D+} + V_{TX-D-}\|)/2\|$ | Between U0 to U1 | — | — | 200 | mV-peak |
| $V_{TX-Idle-Diff-AC-pp}$ | Idle Mode AC Common Mode Delta Voltage $\|V_{TX-D+}-V_{TX-D-}\|$ | Between Tx+ and Tx- in idle mode.<br>Use the HPF to remove DC components. =1/LPF.<br>No AC and DC signals are applied to Rx terminals. | — | — | 10 | mVppd |
| $V_{TX-Idle-Diff-DC}$ | Idle Mode DC Common Mode Delta Voltage $\|V_{TX-D+}-V_{TX-D-}\|$ | Between Tx+ and Tx- in idle mode.<br>Use the LPF to remove DC components. =1/HPF.<br>No AC and DC signals are applied to Rx terminals. | — | — | 10 | mV |
| $G_p$ | Peaking Gain (Compensation at 5GHz, Relative to 100MHz, 100m$V_{p-p}$ Sine Wave Input) | EQ<3:0>=0000<br>EQ<3:0>=0101<br>EQ<3:0>=1010<br>EQ<3:0>=1111 | — | 7.0<br>9.5<br>11.77<br>13.54 | — | dB |
| | | Variation around typical | -3 | — | +3 | dB |
| $G_F$ | Flat Gain (100MHz, EQ<3:0>=0000, SW<1:0>=01) | FG<1:0>=00<br>FG<1:0>=01<br>FG<1:0>=10<br>FG<1:0>=11 | — | -2.07<br>-0.24<br>+0.5<br>+1.77 | — | dB |
| | | Variation around typical | -3 | — | +3 | dB |
| $V_{SW\_100M}$ | -1dB Compression Point Output Swing (at 100MHz) | SW<1:0>=00<br>SW<1:0>=01 | — | 900<br>1000 | — | mVppd |
| $V_{SW\_5G}$ | -1dB Compression Point Output Swing (at 5GHz) | SW<1:0>=00<br>SW<1:0>=01 | — | 600<br>750 | — | mVppd |
| $DD_{NEXT}$[Note3] | Differential Near-End Crosstalk | 100MHz to 5GHz | — | -35 | — | dB |
| $DD_{FEXT}$[Note3] | Differential Far-End Crosstalk | 100MHz to 5GHz | — | -35 | — | dB |
| $V_{NOISE-INPUT}$ | Input-Referred Noise | 100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01 | — | 0.6 | — | $mV_{RMS}$ |
| | | 100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01 | — | 0.5 | — | |
| $V_{NOISE-OUTPUT}$ | Output-Referred Noise[2] | 100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=0000, SW<1:0>=01 | — | 0.8 | — | $mV_{RMS}$ |
| | | 100MHz to 5GHz, FG<1:0>=11, EQ<3:0>=1111, SW<1:0>=01 | — | 1 | — | |
| S11 | Input Return Loss | 10MHz to 5GHz differential | — | -13.0 | — | dB |
| | | 1GHz to 5GHz common mode | — | -6.0 | — | |
| S22 | Output Return Loss | 10MHz to 5GHz differential | — | -15 | — | dB |
| | | 1GHz to 5GHz common mode | — | -6.0 | — | |

| Signal and Frequency Detectors | | | | | | |
|---|---|---|---|---|---|---|
| $V_{TH\_UPM}$ | Unplug Mode Detector Threshold | Threshold of LFPS when the input impedance of the ReDriver is 67kΩ to VbiasRx only. Used in the unplug mode. | 200 | — | 800 | mVppd |
| $V_{TH\_DSM}$ | Deep Slumber Mode Detector Threshold | LFPS signal threshold in Deep slumber mode | 100 | — | 600 | mVppd |
| $V_{TH\_AM}$ | Active Mode Detector Threshold | Signal threshold in Active and slumber mode | 65 | — | 175 | mVppd |
| $F_{TH}$ | LFPS Frequency Detector | Detect the frequency of the input CLK pattern | 100 | — | 400 | MHz |
| $T_{ON\_UPM}$ | Turn on of Unplug Mode | TX pin to RX pin latency when input signal is LFPS | — | — | 3 | mS |
| $T_{ON\text{-}DSM}$ | Turn on of Deep Slumber Mode | | — | — | 5 | µS |
| $T_{ON\_SM}$ | Turn on of Slumber Mode | | — | — | 20 | ns |

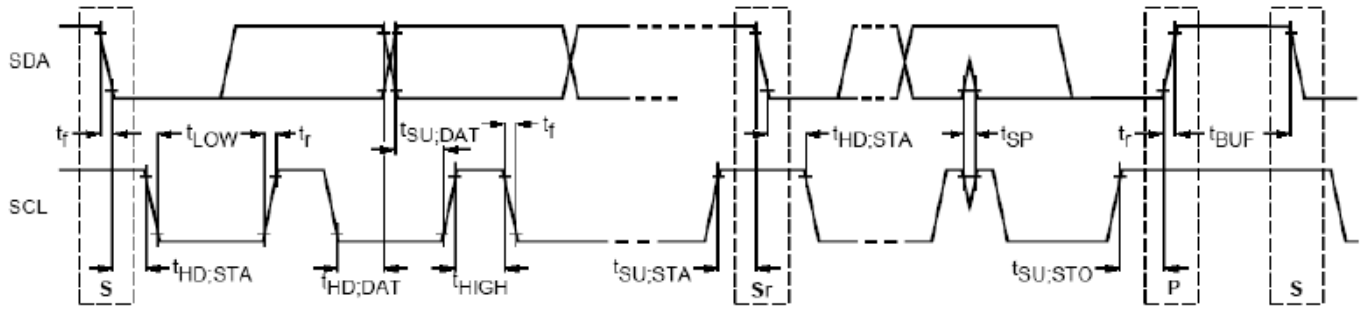
Note:
1. Measured using a vector-network analyzer (VNA) with -15dbm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.
2. Guaranteed by design and characterization.
3. Subtract the Channel Gain from the Total Gain to get the Actual Crosstalk.

## I²C AC Electrical Characteristics

| Symbol | Parameter | Standard Mode I²C | | Fast Mode I²C | | Fast Mode Plus I²C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $f_{SCL}$ | SCL Clock Frequency | 0 | 100 | 0 | 400 | 0 | 1000 | kHz |
| $t_{BUF}$ | Bus Free Time Between a STOP and START Condition | 4.7 | — | 1.3 | — | 0.5 | — | µs |
| $t_{HD;STA}$ | Hold Time (Repeated) START Condition | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| $t_{SU;STA}$ | Setup Time for a Repeated START Condition | 4.7 | — | 0.6 | — | 0.26 | — | µs |
| $t_{SU;STO}$ | Setup Time for STOP Condition | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| $t_{VD;ACK}$[1] | Data Valid Acknowledge Time | — | 3.45 | — | 0.9 | — | 0.45 | µs |
| $t_{HD;DAT}$[2] | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| $t_{VD;DAT}$ | Data Valid Time | — | 3.45 | — | 0.9 | — | 0.45 | ns |
| $t_{SU;DAT}$ | Data Setup Time | 250 | — | 100 | — | 50 | — | ns |
| $t_{LOW}$ | LOW Period of the SCL Clock | 4.7 | — | 1.3 | — | 0.5 | — | µs |
| $t_{HIGH}$ | HIGH Period of the SCL Clock | 4.0 | — | 0.6 | — | 0.26 | — | µs |
| $t_f$ | Fall Time of both SDA and SCL Signals | — | 300 | — | 300 | — | 120 | ns |
| $t_r$ | Rise Time of Both SDA and SCL Signals | — | 1000 | — | 300 | — | 120 | ns |
| $t_{SP}$ | Pulse Width of Spikes that must be Suppressed by the Input Filter | — | 50 | — | 50 | — | 50 | ns |

**Notes:**

1. A fast-mode I²C-bus device can be used in a standard-mode I²C-bus system, but the requirement $t_{SETDAT} \geq 250ns$ must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr_max + $t_{SETDAT}$ = 1000 + 250 = 1250ns (according to the standard-mode I²C bus specification) before the SCL line is released.
2. $C_b$ equals the total capacitance of one BUS line in pF. If mixed with high-speed devices, faster fall times are allowed according to the I²C specification.

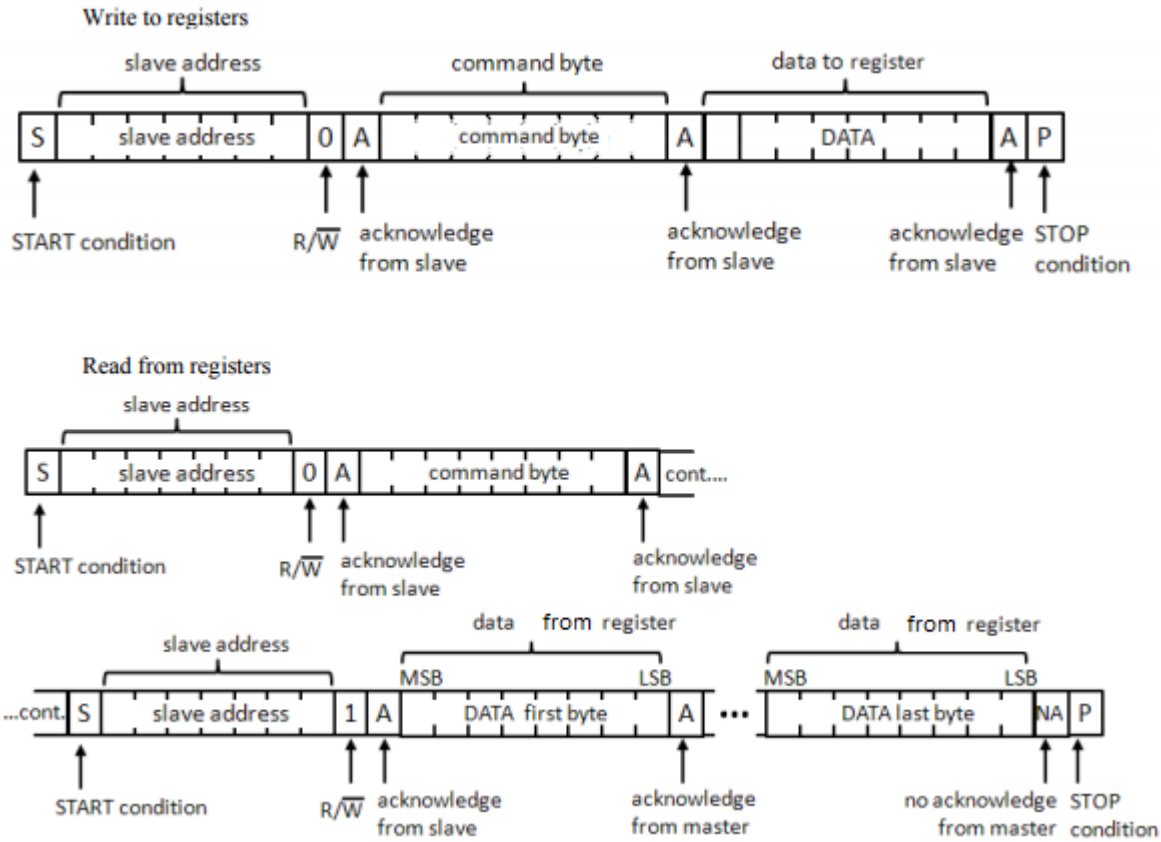



**Definition of Timing for Full-Speed Mode Devices on the I²C Bus**

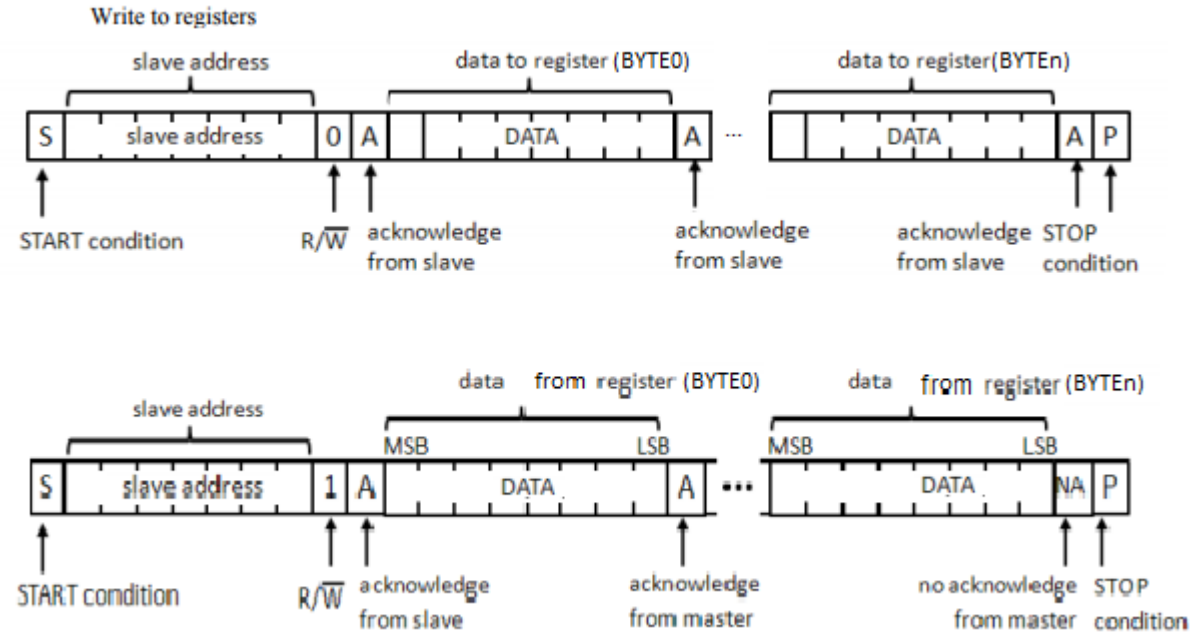
## I²C Slave Address

| ADDR1 | ADDR0 | USB-C Detector I2C Slave Address | ReDriver I2C Slave Address |
|---|---|---|---|
| VDD | VDD3P3 | CAh | A4h |
| 24KΩ to GND | VDD3P3 | 8Ah | A0h |
| 16KΩ to GND | VDD3P3 | EAh | A6h |
| 8.2KΩ to GND | VDD3P3 | AAh | A2h |
| VDD | GND | CAh | Pin Mode |
| 24KΩ to GND | GND | 8Ah | Pin Mode |
| 16KΩ to GND | GND | EAh | Pin Mode |
| 8.2KΩ to GND | GND | AAh | Pin Mode |
| GND | GND | Pin Mode | Pin Mode |

## I²C Data Transfer (USB-C Detector Registers)



## I²C Data Transfer (ReDriver Registers)




***Registers of ReDriver can be Read/Written in Bulk Mode Only**

# USB-C Detector

## Detailed Description

The PI3EQX10312 includes a cost-effective plug-in detector for USB 3.1 Gen2 Type-C connector. It flexibly supports both I2C and pin control mode to configure the port and report the detection results.

### ADDR1

ADDR1 is a five-level input pin to indicate I2C or pin control mode of USB-C detector. When ADDR1 pin shorts to GND, the detector sets to pin control mode. When ADDR1 is connected via various resistors to GND or pulled up to VDD, I2C mode is enabled, and I2C address is set according to the connection of ADDR1 (see Table of I2C Slave Address).

### I2C Mode Configuration

The PI3EQX10312 requires minimal configuration for proper detection and reporting. Write register 01H (control register) to configure different charging profiles and port settings.

### Processor Communication

Typical communication steps between the processor and the PI3EQX10312 during plug detection are:

1. INTB asserted LOW, which indicates changes in register 02H (interrupt register) or register 03H & 04H (status registers).
2. Processor reads interrupt registers to determine which event occurred. Interrupt register (02H) latches attach, detach, or fault event occurred. All interrupt flags in interrupt register (02H) clears after the I2C read action.
3. Processor reads CC status registers (03H & 04H) to determine real-time plugin details, charging profile, and fault condition. Processor can configure the power and USB channels according to information in status registers.
4. After reading register 02H, 03H & 04H, INTB becomes hi-z again.
5. Processor shall configure PI3EQX10312 ReDriver via I2C, if applicable.

### Interrupts

The baseband processor recognizes interrupt signals by observing the INTB signal, which is active LOW. Interrupts are masked upon bit 0 of control register 01H (interrupt mask bit). After the interrupt mask bit is cleared by the baseband processor, the INTB pin is hi-z in preparation for a future interrupt. When an interruptible event occurs, INTB transitions LOW and returns hi-z when the processor reads the interrupt register (02H) and status registers (03H & 04H). Subsequent to the initial power up or reset, if the processor writes a "1" to interrupt mask bit when the system is already powered up, the INTB pin stays hi-z and ignores all interrupts until the interrupt mask bit is cleared.

Aside from monitoring the I2C registers, the system can also monitor ID pin and VBUS for connector status. If the port is configured as a device (or dual-role acting as device), VBUS goes to 5V when host attachment is detected; if the port is configured as a host (or dual-role acting as host), ID pin pulls low when device attachment is detected, and system should assert VBUS.

### Port Setting (Host/Device/Dual-Role)

When power is applied to VDD, an internal power-on reset (POR) holds the PI3EQX10312 in a reset condition until VDD reaches 2.65V. At that point, the reset condition is released, the PI3EQX10312 registers, and $I^2C$-bus state machine will initialize to their default states. Upon power up, Bit [4:1] and Bit [6:5] of register 01H are initialized according to the connections of the pins PORT0, PORT1, and SRC_CUR as follows:

**Port Setting and Register Initial Values**

| PORT1 | PORT0 | Port Setting | Bit [4:1] of Register 01H |
|---|---|---|---|
| Float | VDD | SRC with Accessory Support | 0010 |
| GND | VDD | SRC without Accessory Support | 1010 |
| VDD | Float | DRP with Accessory Support | 0100 |
| VDD | GND | DRP without Accessory Support | 0011 |
| Float | Float | DRP with Try.SRC and Accessory Support | 0110 |
| Float | GND | SINK with Accessory Support | 0001 |
| GND | Float | DRP with Try.SNK and Accessory Support | 0101 |
| GND | GND | SINK without Accessory Support | 0000 |

PI3EQX10312 can be configured through I2C as host, device, or dual-role port per the register table. After power up, the port setting can then be changed by I2C writes to bits [4:1] of control register (01H). Thereafter, VDD must be lowered below 1.0V to reset the device (both registers and I2C-bus state machine).

PI3EQX10312 connects current sources to CC1 and CC2 when operating in host mode. It also sets the current level according to the charging current setting.

**SRC_CUR Setting and Register Initial Values**

| SRC_CUR | SOURCE Current Mode Setting | Bit [6:5] of Register 01H |
|---|---|---|
| VDD | 3A | 10 |
| No Connection | 1.5A | 01 |
| GND | Default | 00 |

This initialization only happens once when PI3EQX10312 is powered up. Register 01H can be changed by I2C commands afterwards.

In device mode, PI3EQX10312 connects two integrated resistor Rd1 and Rd2 to CC1 and CC2 respectively. Dual-role mode enables CC1 and CC2 toggle between host mode and device mode alternatively every 50ms. The toggling stops after connection is made and role negotiated.

**Current Mode Setting and Detection**

PI3EQX10312 can be configured as different current modes per CC1/CC2 setting. Host mode (or dual role acting as host) allows the system to configure between high-current mode (3A), medium-current mode (1.5A) and default-current mode. Different current modes can be set by writing control register (01H). The initial setting depends on SRC_CUR during POR. When in device mode (or dual role acting as device), CC1/CC2 pins allow the system to detect the host charging capability. The charging capability is reported in CC status registers (03H & 04H), which can help the system to configure the charging current accordingly.

**ID**

When PI3EQX10312 is configured as host mode (or dual role acting as host), ID pin is pulled low when a device is attached to the USB-C connector. The ID pin works as an interrupt signal to acknowledge system when there is device attachment. It should be noted the ID pin is not to be driven low when an audio accessory is detected, and ID pin always stays hi-z when port is in device mode.

**Audio Adapter Accessory and Debug Accessory Mode**

PI3EQX10312 can detect analog audio adapter or debug accessory attachment as per CC1/CC2 setting. This is reported in CC status registers (03H & 04H) to help system to configure audio adapter accessory and debug accessory mode accordingly.

**Debug Accessory Detection (DEBUG)**

PI3EQX10312 can detect debug accessory attachment as per CC1/CC2 setting. This is reported by the DEBUG pin in both I2C and pin control modes. DEBUG is pulled low when debug accessory attachment is detected. Otherwise, DEBUG stays hi-z.

**Debug Accessory Detection**

| Debug Accessory | DEBUG |
|---|---|
| Detected | Low |
| Not Detected | Hi-Z |

**VBUS Detection**

PI3EQX10312 detects VBUS to determine the attached state when port is a device.

## USB-C Detector Register Table

| Command | Register | Type | Reset Value | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00H | Device ID | Read | 00000100 | Version ID 00000 | | | | | Vendor ID(Pericom): 100 | | |
| 01H | Control | Read/Write | 0XXXXXX0 | Power Saving | Charging Current Mode (SOURCE/DRPs) | | Port Setting | | | | Interrupt Mask |
| | | | | 0: No Power Saving<br>1: Power Saving | 00: Default<br>01: Medium<br>10: High<br><br>(Initialization from SRC_CUR pin during Power up) | | 0000: SINK without Accessory Support<br>0001: SINK with Accessory Support<br>1010: SRC without Accessory Support<br>0010 :SRC with Accessory Support<br>0011: DRP without Accessory Support<br>0100: DRP with Accessory Support<br>0110: DRP with Try.SRC and Accessory Support<br>0101: DRP with Try.SNK and Accessory Support | | | | 0: Does not Mask Interrupts<br><br>1: Mask Interrupts |
| 02H | Interrupt | Read/Clear | 00000000 | Fault Recovery | OCP Event | OVP Event | Reserved | OTP Event | — | Detach | Attach |
| | | | | 0: Fault Event not Recovered | 0: No OCP Event | 0: No OVP Event | | 0: No OTP Event | — | 0: No Interrupt | |
| | | | | 1: Fault Event Recovered | 1: OCP Event | 1: OVP Event | | 1: OTP Event | — | 1: detachable | 1: attached |
| 03H | Status 1 | Read | 00000000 | VBUS Detection (Port is a Device or in Accessory Mode) | Charging Current Detection (Port is a Device) | | Attached Port Status | | | Plug Polarity | |
| | | | | 0: Vbus not Detected<br>1: Vbus Detected | 00: Standby<br>01: Default<br>10: Medium<br>11: High | | 000: Standby<br>001: SINK (attached.SRC)<br>010: SOURCE (attached.SNK)<br>011: AUDIO<br>100: DEBUGACC.SNK<br>101: DEBUGACC.SRC | | | 00: Standby<br>01: CC2 connected (for attached.SNK,SRC, DebugAcc.SNK or Oriented DebugAcc.SRC)<br>10: CC1 connected (for attached.SNK, DebugAcc.SNK or Oriented DebugAcc.SRC)<br>11: undetermined | |
| 04H | Status 2 | Read | 00000000 | Fault Occurring* | Reserved | | | | | | |
| | | | | 0: No Fault is Occurring | | | | | | | |
| | | | | 1: Fault(s) is Occurring | | | | | | | |

## USB-C Detector Pin Control Functional Description

**Type-C Connector Port Setting (PORT1, PORT0)**

For pin control without I2C, PI3EQX10312 can be configured as different ports by changing PORT1 and PORT0 pins' voltage levels.

**Port Setting**

| PORT1 | PORT0 | Port Setting |
|---|---|---|
| Float | VDD | SRC with Accessory Support |
| GND | VDD | SRC without Accessory Support |
| VDD | Float | DRP with Accessory Support |
| VDD | GND | DRP without Accessory Support |
| Float | Float | DRP with Try.SRC and Accessory Support |
| Float | GND | SINK with Accessory Support |
| GND | Float | DRP with Try.SNK and Accessory Support |
| GND | GND | SINK without Accessory Support |

**SRC_CUR**

When PI3EQX10312 is configured as a host, it can be set to different current mode according to the connection of SRC_CUR pin.

**SRC_CUR Setting**

| SRC_CUR | SOURCE Current Mode Setting |
|---|---|
| VDD | 3A |
| No Connection | 1.5A |
| GND | Default |

**Type-C Connector Current Mode Detection (OUT1, OUT2)**

Type-C connector can detect different host current modes and other accessories per CC1/CC2 setting. When PI3EQX10312 operates in device mode (or dual-role mode acting as device), it detects CC1/CC2 status to determine host charging current modes and reports to the system using OUT1 and OUT2 pins. OUT1 and OUT2 always stays hi-z unless medium- or high-current mode is detected.

**Current Mode Detection**

| | OUT2 | OUT1 |
|---|---|---|
| Default Current Mode | Hi-Z | Hi-Z |
| Medium Current Mode (1.5A) | Hi-Z | Low |
| High Current Mode (3A) | Low | Low |

**Audio Adapter Accessory Detection (OUT3)**

PI3EQX10312 detects analog audio adapter attachment as per CC1/CC2 setting. This is reported by the OUT3 pin. OUT3 is pulled low when an analog audio adapter attachment is detected. Otherwise, OUT3 stays hi-z.

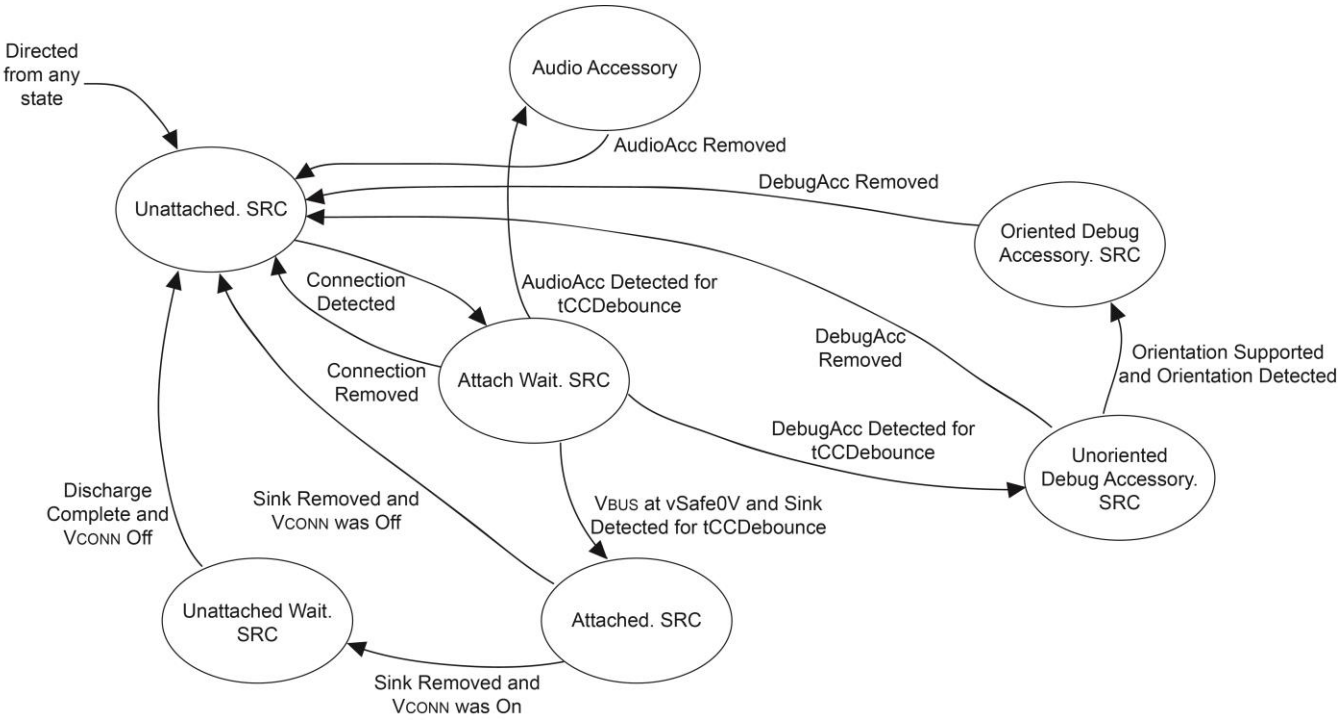
**Audio Adapter Accessory Detection**

| Audio Accessory | OUT3 |
|---|---|
| Detected | Low |
| Not Detected | Hi-Z |

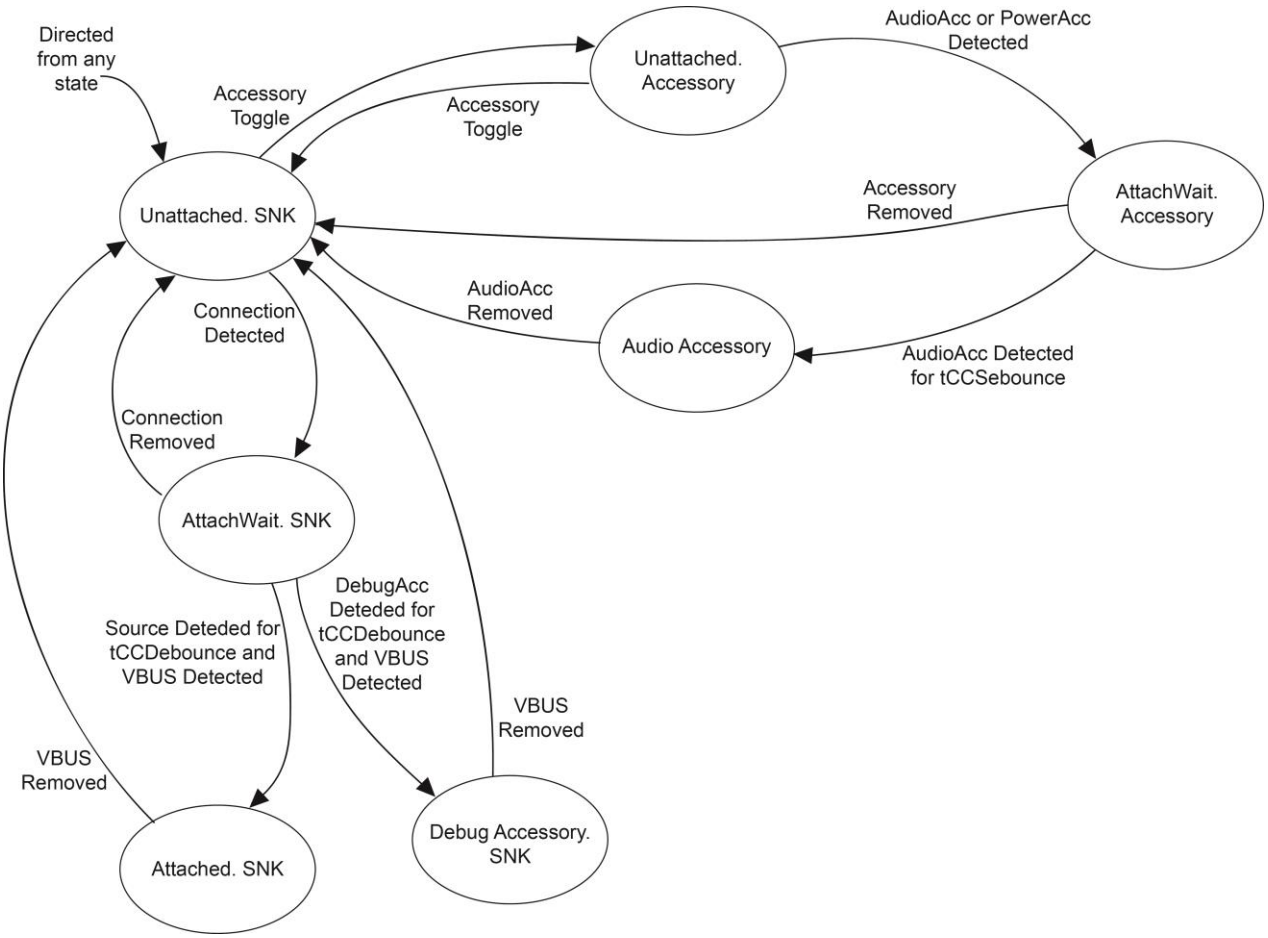
**ADDR1, ID, ENB Pins**

Functionality of the ADDR1, ID, and ENB pins are the same for pin control or I2C control modes. Refer to previous section for detail description.

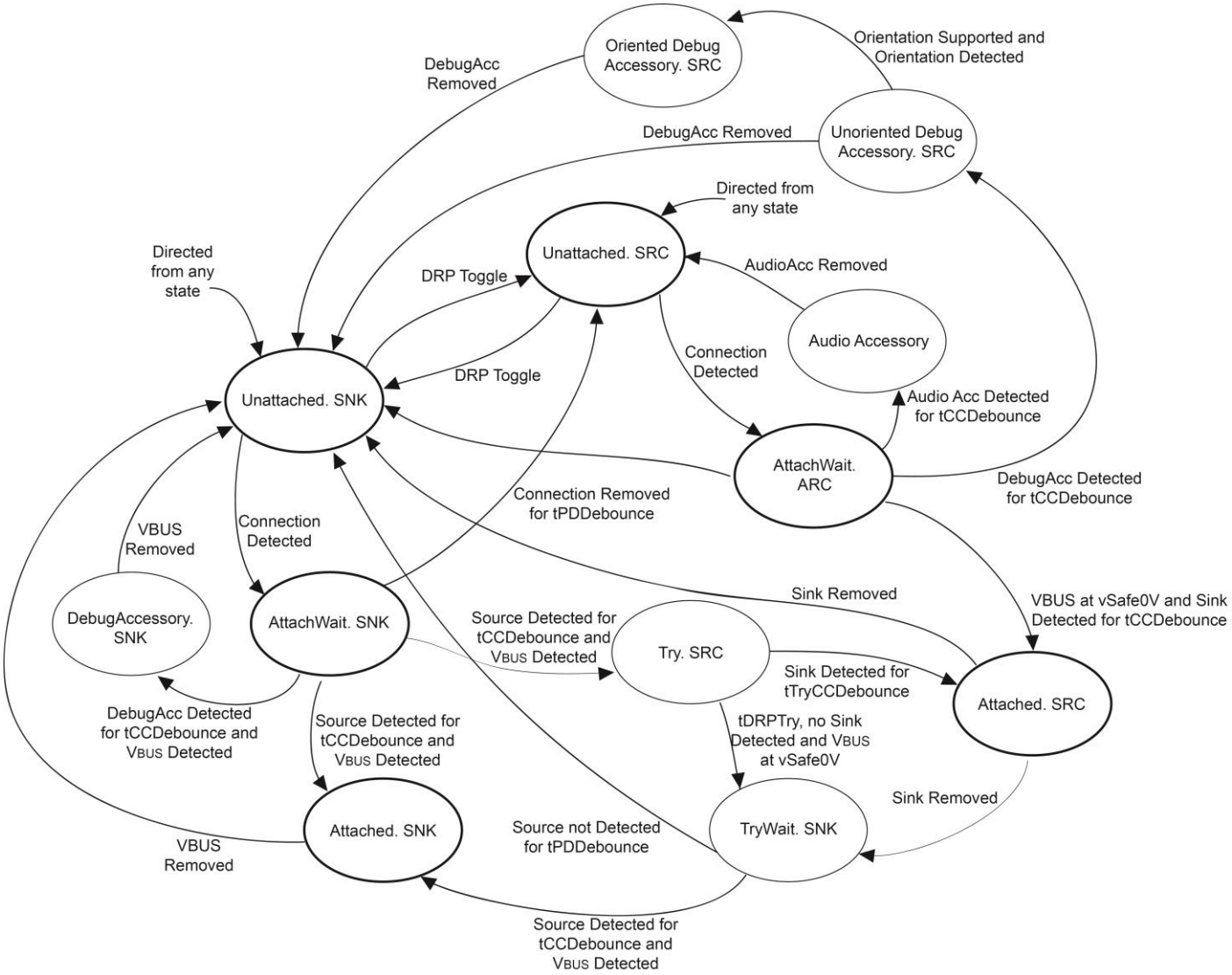
## Connection State Diagram: SRC with Accessory Support




## Connection State Diagram: SNK with Accessory Support



## Connection State Diagram: DRP with Try.SRC with Accessory Support



## ReDriver Detailed Description

### ReDriver Register Table

**(Accessible only when "Attached with plug polarity determined" by USB-C Detector. Register values will be reset when "Unattached")**

| **Register Assignment** | | | | |
|---|---|---|---|---|
| **BYTE 0** (Revision and Vendor ID Register) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | RO | 0 | Revision ID | Rev# = 0000 |
| 6 | RO | 0 | | |
| 5 | RO | 0 | | |
| 4 | RO | 0 | | |
| 3 | RO | 0 | Vendor ID | Pericom ID = 0011 |
| 2 | RO | 0 | | |
| 1 | RO | 1 | | |
| 0 | RO | 1 | | |
| **BYTE 1** (Device Type/ Device ID Register) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | RO | 0 | Device Type | Device Type<br>0000 = Passive MUX<br>0001 = Active MUX |
| 6 | RO | 0 | | |
| 5 | RO | 0 | | |
| 4 | RO | 1 | | |
| 3 | RO | 0 | Device ID | Device ID = 0001 |
| 2 | RO | 0 | | |
| 1 | RO | 0 | | |
| 0 | RO | 1 | | |
| **BYTE 2** (Byte count Register 32 Bytes) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | RO | 0 | Register Byte count | I2C byte count = 32 bytes |
| 6 | RO | 0 | | |
| 5 | RO | 1 | | |
| 4 | RO | 0 | | |
| 3 | RO | 0 | | |
| 2 | RO | 0 | | |
| 1 | RO | 0 | | |
| 0 | RO | 0 | | |
| **BYTE 3** (Channel Assignment and Receiver Detection Enable Control) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | R/W | 0 | — | Reserved |
| 6 | R/W | 1 | CONF<2> | Channel Assignment |
| 5 | R/W | 0 | CONF<1> | |
| 4 | R/W | 1 | CONF<0> | |
| 3 | R/W | 0 | | Reserved |
| 2 | R/W | 0 if RXDET_EN pin=1;<br>1 if RXDET_EN pin=0 | RXDET_EN# | Far-end receiver detection enable/disable<br>0 = Enable<br>1 = Disable |
| 1 | R/W | 1 | — | Reserved |
| 0 | R/W | 0 | — | Reserved |
| **BYTE 4** (Power Down Control) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | R/W | 0 | PD_CON_Rx1 | CONx power override<br>0 – Normal operation<br>1 – Force the CONx to power down state |
| 6 | R/W | 0 | PD_CON_Tx1 | |
| 5 | R/W | 0 | PD_CON_Tx2 | |
| 4 | R/W | 0 | PD_CON_Rx2 | |
| 3 | R/W | 0 | — | Reserved |
| 2 | R/W | 0 | — | Reserved |
| 1 | R/W | 0 | — | Reserved |
| 0 | R/W | 0 | — | Reserved |
| **BYTE 5** (Equalization, Flat Gain and -1dB Linear Swing Setting of CON_Rx2) | | | | |

| Bit | Type | Power-up Condition | Control Affected | Comment |
|---|---|---|---|---|
| 7 | R/W | 0 | CON_Rx2_EQ<3> | CON_Rx2 setting configuration<br><br>Equalizer<br>Flat Gain<br>Swing |
| 6 | R/W | 0 | CON_Rx2_EQ<2> | |
| 5 | R/W | 0 | CON_Rx2_EQ<1> | |
| 4 | R/W | 0 | CON_Rx2_EQ<0> | |
| 3 | R/W | 0 | CON_Rx2_FG<1> | |
| 2 | R/W | 1 | CON_Rx2_FG<0> | |
| 1 | R/W | 0 | CON_Rx2_SW<1> | |
| 0 | R/W | 1 | CON_Rx2_SW<0> | |
| **BYTE 6** (Equalization, Flat Gain and -1dB Linear Swing Setting of CON_Tx2) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | R/W | 0 | CON_Tx2_EQ<3> | CON_Tx2 setting configuration<br><br>Equalizer<br>Flat Gain<br>Swing |
| 6 | R/W | 0 | CON_Tx2_EQ<2> | |
| 5 | R/W | 0 | CON_Tx2_EQ<1> | |
| 4 | R/W | 0 | CON_Tx2_EQ<0> | |
| 3 | R/W | 0 | CON_Tx2_FG<1> | |
| 2 | R/W | 1 | CON_Tx2_FG<0> | |
| 1 | R/W | 0 | CON_Tx2_SW<1> | |
| 0 | R/W | 1 | CON_Tx2_SW<0> | |
| **BYTE 7** (Equalization, Flat Gain and -1dB Linear Swing Setting of CON_Tx1) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | R/W | 0 | CON_Tx1_EQ<3> | CON_Tx1 setting configuration<br><br>Equalizer<br>Flat Gain<br>Swing |
| 6 | R/W | 0 | CON_Tx1_EQ<2> | |
| 5 | R/W | 0 | CON_Tx1_EQ<1> | |
| 4 | R/W | 0 | CON_Tx1_EQ<0> | |
| 3 | R/W | 0 | CON_Tx1_FG<1> | |
| 2 | R/W | 1 | CON_Tx1_FG<0> | |
| 1 | R/W | 0 | CON_Tx1_SW<1> | |
| 0 | R/W | 1 | CON_Tx1_SW<0> | |
| **BYTE 8** (Equalization, Flat Gain and -1dB Linear Swing Setting of CON_Rx1) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | R/W | 0 | CON_Rx1_EQ<3> | CON_Rx1 setting configuration<br><br>Equalizer<br>Flat Gain<br>Swing |
| 6 | R/W | 0 | CON_Rx1_EQ<2> | |
| 5 | R/W | 0 | CON_Rx1_EQ<1> | |
| 4 | R/W | 0 | CON_Rx1_EQ<0> | |
| 3 | R/W | 0 | CON_Rx1_FG<1> | |
| 2 | R/W | 1 | CON_Rx1_FG<0> | |
| 1 | R/W | 0 | CON_Rx1_SW<1> | |
| 0 | R/W | 1 | CON_Rx1_SW<0> | |
| **BYTE 9-11 (Reserved)** | | | | |
| **BYTE 12** (Threshold, Feature Enable/ Disable and Timing Setting) | | | | |
| **Bit** | **Type** | **Power-up Condition** | **Control Affected** | **Comment** |
| 7 | R/W | 0 | IDET_VTH<1> | High-Speed channel signal detector threshold setting:<br>00 50mVppd<br>01 65mVppd (Default)<br>10 80mVppd<br>11 95mVppd |
| 6 | R/W | 1 | IDET_VTH<0> | |
| 5 | R/W | 1 | Reserved | — |
| 4 | R/W | 1 | Reserved | — |
| 3 | R/W | 0 | Reserved | — |
| 2 | R/W | 0 | Reserved | — |
| 1 | R/W | 0 | Reserved | — |
| 0 | R/W | 1 | Reserved | — |
| **BYTE 13-31 (Reserved)** | | | | |

### Equalization Setting (dB):

| EQ1pin | EQ0pin | EQ3 | EQ2 | EQ1 | EQ0 | @ 2.5GHz | @ 3GHz | @ 4GHz | @ 5GHz | @ 6GHz | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | F | 0 | 0 | 0 | 0 | 3.57 | 4.22 | 5.44 | 6.42 | 7.27 | Default |
| 0 | 1 | 0 | 0 | 0 | 1 | 3.83 | 4.56 | 5.93 | 7.04 | 8.00 | — |
| 0 | 0 | 0 | 0 | 1 | 0 | 4.13 | 4.93 | 6.47 | 7.71 | 8.76 | — |
| 0 | R | 0 | 0 | 1 | 1 | 4.41 | 5.29 | 6.95 | 8.29 | 9.42 | — |
| R | 1 | 0 | 1 | 0 | 0 | 4.98 | 5.89 | 7.61 | 8.99 | 10.14 | — |
| R | F | 0 | 1 | 0 | 1 | 5.25 | 6.23 | 8.05 | 9.50 | 10.70 | — |
| R | R | 0 | 1 | 1 | 0 | 5.55 | 6.59 | 8.51 | 10.04 | 11.28 | — |
| R | 0 | 0 | 1 | 1 | 1 | 5.82 | 6.92 | 8.93 | 10.51 | 11.78 | — |
| F | 0 | 1 | 0 | 0 | 0 | 6.39 | 7.44 | 9.39 | 10.93 | 12.16 | — |
| F | R | 1 | 0 | 0 | 1 | 6.63 | 7.74 | 9.76 | 11.34 | 12.60 | — |
| F | F | 1 | 0 | 1 | 0 | 6.90 | 8.05 | 10.14 | 11.77 | 13.05 | — |
| F | 1 | 1 | 0 | 1 | 1 | 7.14 | 8.34 | 10.49 | 12.15 | 13.44 | — |
| 1 | R | 1 | 1 | 0 | 0 | 7.51 | 8.71 | 10.87 | 12.53 | 13.81 | — |
| 1 | 0 | 1 | 1 | 0 | 1 | 7.74 | 8.97 | 11.18 | 12.87 | 14.15 | — |
| 1 | 1 | 1 | 1 | 1 | 0 | 7.98 | 9.25 | 11.51 | 13.23 | 14.51 | — |
| 1 | F | 1 | 1 | 1 | 1 | 8.20 | 9.51 | 11.81 | 13.54 | 14.82 | — |

### Flat Gain Setting:

FGpin is the selection pin for the DC gain

| FGpin | FG<1:0> | Flat Gain Setting (dB) |
|---|---|---|
| R | 00 | -2.07 |
| F | 01 | -0.24 (Default) |
| 0 | 10 | 0.5 |
| 1 | 11 | 1.77 |

### Swing -1dB Compression Point Output Swing Setting:

SWpin is the selection pin for SW

| SWpin | SW<1:0> | Flat Gain Setting |
|---|---|---|
| 0 | 00 | 900m Vppd |
| 1 | 01 | 1000m Vppd (Default) |
| NA | 10 | 1100m Vppd |
| NA | 11 | 1200m Vppd |

### ReDriver Connection in Pin Mode

| USB-C Status | ReDriver Status |
|---|---|
| Unattached | Inactive |
| Attached and CC1 connected | TX_CON1/RX_CON1 Active |
| Attached and CC2 connected | TX_CON2/RX_CON2 Active |

### ReDriver Connection in I2C Mode

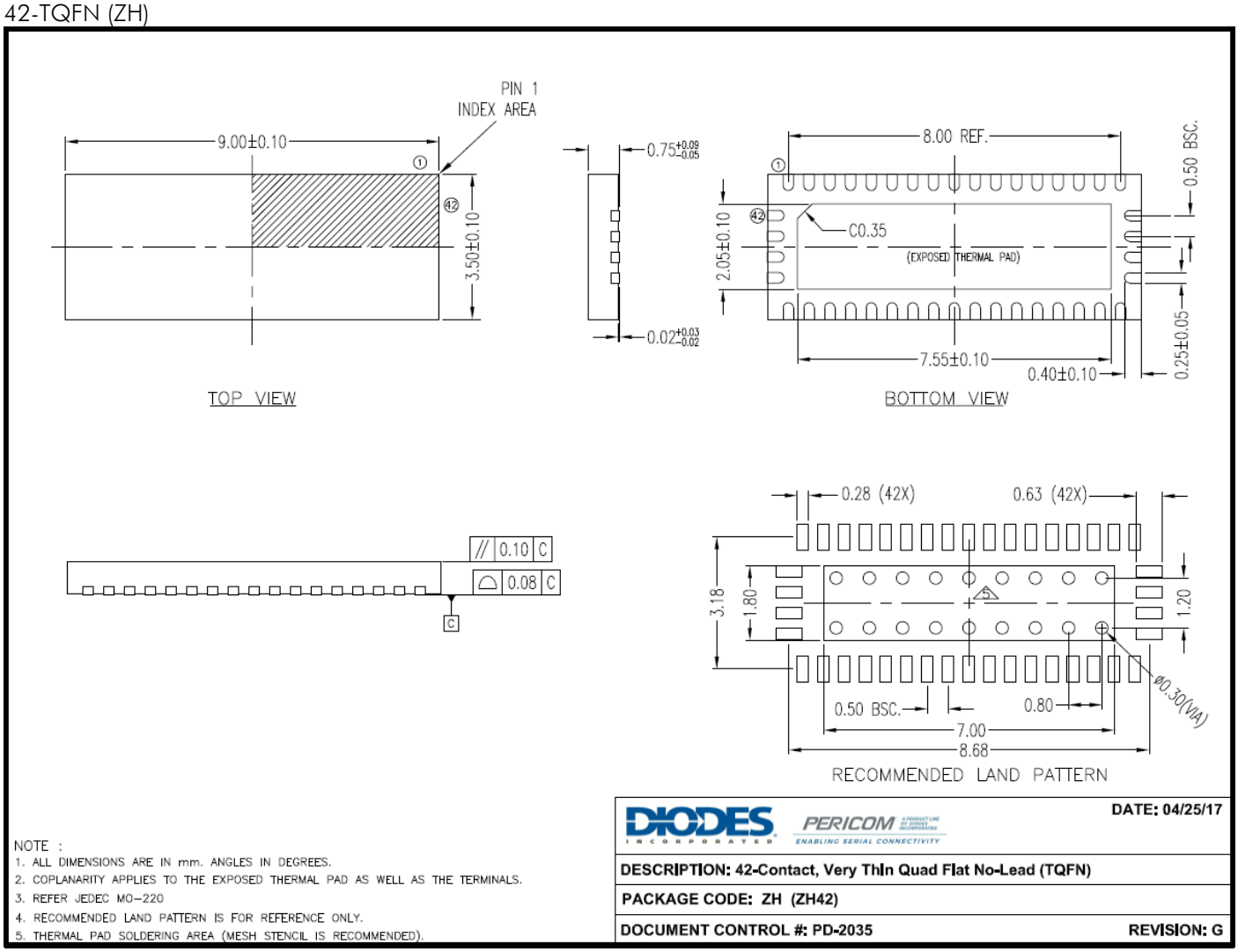
| USB-C Status | BYTE3 CONF<2:0> | ReDriver Status |
|---|---|---|
| Unattached | X | Inactive |
| Attached | 100 | TX_CON1/RX_CON1 Active |
| Attached | 101 (Default) | TX_CON2/RX_CON2 Active |

## Part Marking

Top mark not available at this time. To obtain advanced information regarding the top mark, contact your local sales representative.

## Packaging Mechanical

42-TQFN (ZH)




17-0266

**For latest package information:**

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

## Ordering Information

| Orderable Part Number | Package Code | Package Description |
|---|---|---|
| PI3EQX10312ZHEX | ZH | 42-Contact, Very Thin Quad Flat No-Lead (TQFN) |

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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