

# SM802XXX

# Flexible Ultra-Low Jitter Clock Synthesizer

#### **Features**

- 115 fs at 156.25 MHz (1.875 MHz to 20 MHz)
- 265 fs at 156.25 MHz (12 kHz to 20 MHz)
- PCle Gen 1/2/3/4/5/6 Compliant
- On-Chip Power Supply Regulation for Excellent Board-Level Power Supply Noise Immunity
- Generates up to 8 Combinations of Differential or 16 Single-Ended Clock Outputs
  - LVPECL, LVDS, HCSL, LVCMOS (SE or Diff)
- · Selectable Input:
  - Crystal: 11.4 MHz to 27 MHz
  - Reference Input: 11.4 MHz to 80 MHz
- No External Crystal Oscillator Capacitors Required
- · 2.5V or 3.3V Operating Power Supply
- · Available in Industrial Temperature Range
- Available in Green, RoHS, and PFOS Compliant VQFN Packages:
  - 44-pin, 7 mm × 7 mm
  - 32-pin, 5 mm × 5 mm
  - 24-pin, 4 mm × 4 mm
  - 16-pin, 3 mm × 3.5 mm

### **Applications**

- Ethernet 100/400/800G
- SONET/SDH
- PCI Express
- · CPRI/OBSAI Wireless Base Station
- Fibre Channel
- SAS/SATA
- DIMM

### **General Description**

The SM802xxx series is a member of the ClockWorks<sup>®</sup> family of devices from Microchip and provide an extremely low-noise timing solution for applications such as (1-100) Gigabit Ethernet, SONET, wireless base station, satellite communication, Fibre Channel, SAS/SATA, and PCIe. It is based upon a unique PLL architecture that provides less than 250 fs phase jitter.

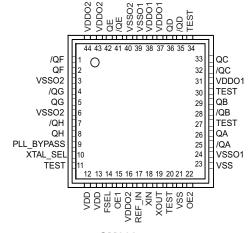
The devices operate from a 2.5V or 3.3V power supply and synthesize up to 8 different combinations (LVPECL, LVDS, HCSL) of differential or 16 single-ended output clocks. The devices accept an external reference clock or crystal input.

The SM802xxx series is fully programmable and a web tool is available to configure a part for samples at the ClockWorks Configurator tool.

## **Package Types**

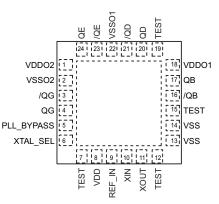
# SM802xxx

Option 1: 44-Pin 7 mm x 7 mm VQFN (Top View)



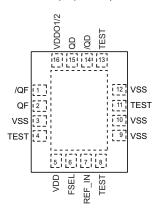
#### SM802xxx

Option 3: 24-Pin 4 mm x 4 mm VQFN (Top View)



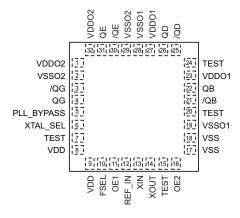
### SM802xxx

Option 5: 16-Pin 3 mm x 3.5 mm VQFN (Top View)



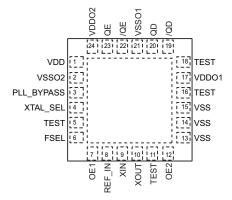
#### SM802xxx

Option 2: 32-Pin 5 mm x 5 mm VQFN (Top View)



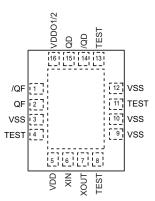
#### SM802xxx

Option 4: 24-Pin 4 mm x 4 mm VQFN (Top View)

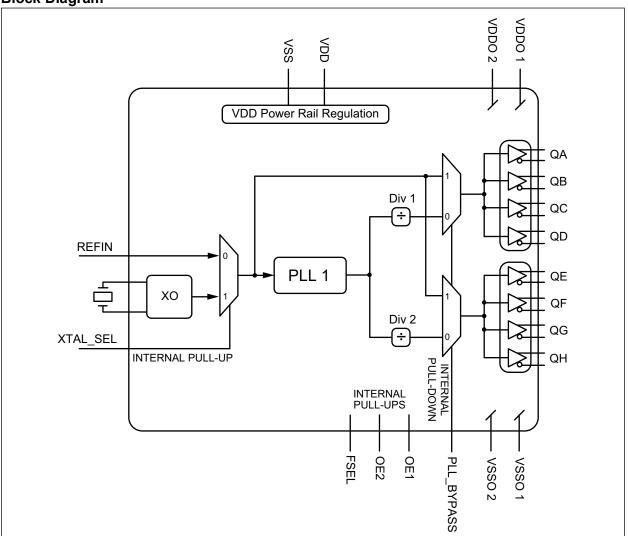


## SM802xxx

Option 6: 16-Pin 3 mm x 3.5 mm VQFN (Top View)



# **Block Diagram**



# 1.0 ELECTRICAL CHARACTERISTICS

## **Absolute Maximum Ratings †**

## **Operating Ratings ††**

Supply Voltage (V<sub>DD</sub>, V<sub>DDO1/2</sub>).....+2.375V to +3.465V

**† Notice:** Exceeding the absolute maximum ratings may damage the device.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

# DC ELECTRICAL CHARACTERISTICS (Note 1)

**Electrical Characteristics:**  $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $V_{A} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

20.76, 14, 10.00.00.00.									
Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions			
3.3V Operating Voltage	V <sub>DD</sub> ,	3.135	3.3	3.465	.,,	V -V			
2.5V Operating Voltage	V <sub>DDO1/2</sub>	2.375	2.5	2.625	V	$V_{DDO1} = V_{DDO2}$			
Total Supply Current, VDD + VDDO		_	275	345		8 LVPECL, 312.5 MHz (44-pin VQFN) Outputs open			
	I <sub>DD</sub>	_	150	185	mA	4 HCSL (PCIe), 100 MHz (32-pin or 24-pin VQFN) Outputs 50Ω to $V_{SS}$			
		_	70	90		2 LVCMOS, 125 MHz (16-pin VQFN) Outputs open			

**Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

# LVCMOS INPUTS (OE1, OE2, PLL\_BYPASS, XTAL\_SEL, FSEL) DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: $V_{DD} = 3.3V \pm 5\%$ or 2.5V $\pm 5\%$ ; $T_A = -40$ °C to $+85$ °C.									
Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions			
Input High Voltage	V <sub>IH</sub>	2	_	V <sub>DD</sub> + 0.3	V	_			
Input Low Voltage	V <sub>IL</sub>	-0.3	_	0.8	V	_			
Input High Current	I <sub>IH</sub>	_	_	150	μA	V <sub>DD</sub> = V <sub>IN</sub> = 3.465V			
Input Low Current	I <sub>IL</sub>	-150	_	_	μΑ	V <sub>DD</sub> = 3.465V, V <sub>IN</sub> = 0V			

**Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

## LVDS OUTPUT DC ELECTRICAL CHARACTERISTICS (Note 1)

**Electrical Characteristics:**  $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ;  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ;  $V_{A} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .  $R_{L} = 100\Omega$  across Q1 and /Q1.

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions			
Differential Output Voltage	V <sub>OD</sub>	275	350	475	mV	Figure 5-8			
V <sub>OD</sub> Magnitude Change	$\Delta V_{OD}$	_	1	40	mV	_			
Offset Voltage	Vos	1.15	1.25	1.50	V	_			
V <sub>OS</sub> Magnitude Change	$\Delta V_{OS}$	_	1	50	mV	_			

**Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

# **HCSL OUTPUT DC ELECTRICAL CHARACTERISTICS (Note 1)**

**Electrical Characteristics:**  $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $V_{A} = -40$ °C to +85°C.  $R_{I} = 50\Omega$  to  $V_{SS}$ .

2076, 1A 10 0 to 00 01.1L 0011 to 1555.									
Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions			
Output High Voltage	V <sub>OH</sub>	660	700	850	mV	_			
Output Low Voltage	V <sub>OL</sub>	-150	0	27	mV	_			
Output Voltage Swing	V <sub>SWING</sub>	250	350	550	mV	_			

**Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

# LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS (Note 1)

**Electrical Characteristics:**  $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $T_{\Delta} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .  $R_{L} = 50\Omega$  to  $V_{DDO} - 2V$ .

2070, 1A 10 0 10 100 0. TL 0012 10 VDDO 2V.										
Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions				
Output High Voltage	V <sub>OH</sub>	V <sub>DDO</sub> – 1.145	V <sub>DDO</sub> – 0.97	V <sub>DDO</sub> – 0.845	V	_				
Output Low Voltage	V <sub>OL</sub>	V <sub>DDO</sub> – 1.945	V <sub>DDO</sub> - 1.77	V <sub>DDO</sub> – 1.645	<b>V</b>	_				
Output Voltage Swing	V <sub>SWING</sub>	0.6	0.8	1.0	V	_				

**Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

# LVCMOS OUTPUT DC ELECTRICAL CHARACTERISTICS (Note 1)

**Electrical Characteristics:**  $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO1/2} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ;  $V_{A} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .  $R_{L} = 50\Omega$  to  $V_{DDO}/2$ .

73						
Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Output High Voltage	V <sub>OH</sub>	V <sub>DDO</sub> – 0.7	_	_	V	Figure 5-9
Output Low Voltage	V <sub>OL</sub>	_	_	0.6	V	Figure 5-9

**Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

# REF\_IN DC ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Characteristics: V <sub>DD</sub> = 3.3V ±5% or 2.5V ±5%; T <sub>A</sub> = -40°C to +85°C.								
Parameter Symbol Min. Typ. Max. Units Conditions								
Input High Voltage	V <sub>IH</sub>	1.1	_	V <sub>DD</sub> + 0.3	V	_		
Input Low Voltage	V <sub>IL</sub>	-0.3	_	0.6	V	_		
Input Current	I <sub>IN</sub>	<b>-</b> 5	_	5	μA	$XTAL\_SEL = V_{IL}, V_{IN} = 0V \text{ to } V_{DD}$		
		_	20	_	μΑ	XTAL_SEL = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>DD</sub>		

**Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.

## **CRYSTAL CHARACTERISTICS**

Electrical Characteristics: $V_{DD} = 3.3V \pm 5\%$ or 2.5V $\pm 5\%$ ; $T_A = -40$ °C to $+85$ °C.								
Parameter	Min.	Тур.	Max.	Units	Conditions			
Mode of Oscillation	Funda	mental, presonant		_	10 pF load capacitance			
Frequency	11.4	_	27	MHz	_			
Equivalent Series Resistance (ESR)	_	_	30	Ω	_			
Shunt Capacitance, C0	_	2	5	pF	_			
Correlation Drive Level	_	10	100	μW	_			

# LVPECL AC ELECTRICAL CHARACTERISTICS (Note 1, Note 2, Note 3, Note 4)

**Electrical Characteristics:**  $V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V$  or  $3.3V \pm 5\%$ ,  $T_{A} = -40$ °C to +85°C, unless otherwise noted.

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions		
Output Frequency	F <sub>OUT</sub>	11	_	840	MHz	_		
LVPECL Output Rise/Fall Time	t <sub>r</sub> /t <sub>f</sub>	80	175	350	ps	20% - 80%		
Output Duty Cycle	ODC	48	50	52	%	< 350 MHz		
		45	50	55	%	≥ 350 MHz		
Output-to-Output Skew	T <sub>SKEW</sub>	_	_	45	ps	Note 5		
PLL Lock Time	T <sub>LOCK</sub>	_	_	20	ms	_		
RMS Phase Jitter @ 156.25 MHz	$T_{jit(\emptyset)}$	_	265	_	fs	Integration Range (12 kHz to 20 MHz)		
		_	115	_	fs	Integration Range (1.875 MHz to 20 MHz)		

- **Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.
  - 2: See Figure 5-6 through Figure 5-9 for load test circuit examples.
  - 3: All phase noise measurements were taken with an Agilent 5052B phase noise system.
  - **4:** Output load is  $50\Omega$  to  $V_{DD} 2V$ .
  - **5:** Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.

## LVDS AC ELECTRICAL CHARACTERISTICS (Note 1, Note 2, Note 3, Note 4)

**Electrical Characteristics:**  $V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V$  or  $3.3V \pm 5\%$ ,  $T_{A} = -40^{\circ}$ C to  $+85^{\circ}$ C, unless otherwise noted.

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Output Frequency	f <sub>OUT</sub>	11.4	_	840	MHz	_
LVDS Output Rise/Fall Time	t <sub>r</sub> /t <sub>f</sub>	100	160	400	ps	20% - 80%
Output Duty Cycle	ODC	48	50	52	%	< 350 MHz
		45	50	55	%	≥ 350 MHz
Output-to-Output Skew	t <sub>SKEW</sub>	_	_	45	ps	Note 5
PLL Lock Time	t <sub>LOCK</sub>	_	_	20	ms	_
RMS Phase Jitter @ 156.25 MHz	t <sub>jit(Ø)</sub>	_	110	_	fs	Integration Range (1.875 MHz to 20 MHz)
PCle Refclk Jitter	t <sub>jphPCle6_CC</sub>	_	6	12	fs <sub>RMS</sub>	PCIe Gen 6 (64 GT/s) in Clock Generator Mode

- **Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.
  - 2: See Figure 5-6 through Figure 5-9 for load test circuit examples.
  - 3: All phase noise measurements were taken with an Agilent 5052B phase noise system.
  - **4:** Outputs terminated  $100\Omega$  between Q and /Q. All unused outputs must be terminated.
  - **5:** Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.

# HCSL AC ELECTRICAL CHARACTERISTICS (Note 1, Note 2, Note 3, Note 4)

**Electrical Characteristics:**  $V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ,  $V_{DDO} = 2.5V$  or 3.3V  $\pm 5\%$ ,  $T_A = -40^{\circ}$ C to  $+85^{\circ}$ C, unless otherwise noted.

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions		
Output Frequency	f <sub>OUT</sub>	11.4	_	840	MHz	_		
Output Rise/Fall Time	t <sub>r</sub> /t <sub>f</sub>	150	300	450	ps	20% - 80%		
Output Duty Cycle	ODC	48	50	52	%	< 350 MHz		
		45	50	55	%	≥ 350 MHz		
Output-to-Output Skew	t <sub>SKEW</sub>	_	_	50	ps	Note 5		
PLL Lock Time	t <sub>LOCK</sub>	_	_	20	ms	_		
RMS Phase Jitter @ 100 MHz	t <sub>jit(Ø)</sub>	_	265	_	fs	Integration Range (12 kHz to 20 MHz)		
		_	115	_	fs	Integration Range (1.875 MHz to 20 MHz)		
PCIe Refclk Jitter	t <sub>jphPCle6_CC</sub>	_	6	12	fs <sub>RMS</sub>	PCIe Gen 6 (64 GT/s) in Clock Generator Mode		

- **Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.
  - 2: See Figure 5-6 through Figure 5-9 for load test circuit examples.
  - 3: All phase noise measurements were taken with an Agilent 5052B phase noise system.
  - 4: Output load is  $50\Omega$  to  $V_{DD}$  / 2.
  - **5:** Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.

# LVCMOS AC ELECTRICAL CHARACTERISTICS (Note 1, Note 2, Note 3, Note 4)

**Electrical Characteristics:**  $V_{DDA} = V_{DD} = 3.3V \pm 5\%$  or 2.5V  $\pm 5\%$ ,  $V_{DDO} = 2.5V$  or 3.3V  $\pm 5\%$ ,  $T_{A} = -40$ °C to +85°C, unless otherwise noted.

Parameter	Symbol	Min.	Тур.	Max.	Units	Conditions
Output Frequency	F <sub>OUT</sub>	11.4	_	250	MHz	_
REF_IN Frequency	F <sub>REF</sub>	11	_	80	MHz	_
Output Rise/Fall Time	t <sub>r</sub> /t <sub>f</sub>	100	_	500	ps	20% - 80%
Output Duty Cycle	ODC	45	50	55	%	_
Output-to-Output Skew	T <sub>SKEW</sub>	_	_	60	ps	Note 5
PLL Lock Time	T <sub>LOCK</sub>	_	_	20	ms	_
RMS Phase Jitter @ 125 MHz	$T_{jit(\varnothing)}$	_	115	_	fs	Integration Range (1.875 MHz to 20 MHz)

- **Note 1:** The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics tables after thermal equilibrium has been established.
  - 2: See Figure 5-6 through Figure 5-9 for load test circuit examples.
  - 3: All phase noise measurements were taken with an Agilent 5052B phase noise system.
  - **4:** Output load is  $50\Omega$  to  $V_{DD}$  / 2.
  - **5:** Defined as skew between outputs at the same supply voltage and with equal load conditions; Measured at the output differential crossing points.

# **TEMPERATURE SPECIFICATIONS**

Parameters	Sym.	Min.	Тур.	Max.	Units	Conditions		
Temperature Ranges								
Ambient Temperature Range	T <sub>A</sub>	-40	_	+85	°C	_		
Lead Temperature	_	_	_	+260	°C	Soldering, 20s		
Case Temperature		_	_	+115	°C	_		
Storage Temperature Range	T <sub>S</sub>	-65	_	+150	°C	_		
Package Thermal Resistances (Note	1)				-			
Junction Thermal Resistance, 7 x 7 VQFN-44Ld	$\theta_{\sf JA}$	_	24	_	°C/W	_		
Junction Thermal Resistance, 5 x 5 VQFN-32Ld	$\theta_{\sf JA}$	_	34	_	°C/W	_		
Junction Thermal Resistance, 4 x 4 VQFN-24Ld	θ <sub>JA</sub>	_	50	_	°C/W	_		
Junction Thermal Resistance, 3 x 3.5 VQFN-16Ld	$\theta_{JA}$	_	60	_	°C/W	_		

**Note 1:** Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

# 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

F	Pin Num	bers by	Packag	e Optio	n	D:		D:	
#1 44-pin	#2 32-pin	#3 24-pin	#4 24-pin	#5 16-pin	#6 16-pin	Pin Name	Pin Type	Pin Level	Pin Function
18	13	10	9	_	6	XIN	I,O (SE)		Crystal connections.
19	14	11	10	_	7	XOUT	1,0 (32)	_	Crystal confidentions.
17	12	9	8	7	_	REF_IN	I, (SE)	LVCMOS	Reference clock input.
14	10	_	6	6	_	FSEL	I, (SE)	LVCMOS	Frequency Select, divides output frequencies by 2. 0 = FREQ, 1 = FREQ/2, 45 kΩ pull-up
10	6	6	4	_		XTAL SEL	I, (SE)	LVCMOS	XTAL Select, selects between XTAL and REF_IN 0 = REF_IN, 1 = XTAL, 45 kΩ pull-up
9	5	5	3	_		PLL BYPASS	I, (SE)	LVCMOS	Bypasses the PLL and switches the XTAL or REF_IN frequency to all outputs $0$ = PLL mode, $1$ = Bypass mode, $45 \text{ k}\Omega$ pull-down
25	_	_			_	/QA	0	Various	
26	_	_		_	_	QA		various	
28	21	16		_	_	/QB	0	Various	Clock Outputs from Bank 1
29	22	17	_		_	QB		Various	Each output can be programmed to its own logic
32						/QC	0	Various	type: LVPECL, LVDS, HCSL, or
33	_	_	_		_	QC	_		LVCMOS (Note 1)
35	25	20	19	14	14	/QD	0	Various	
36	26	21	20	15	15	QD		70	
41	30	23	22		_	/QE	0	Various	
42	31	24	23		_	QE			
1	<u> </u>	_		1	1	/QF	0	Various	Clock Outputs from Bank 2 Each output can be
2		_		2	2	QF			programmed to its own logic
4	3	3			_	/QG	0	Various	type: LVPECL, LVDS, HCSL, or
5	4	4			_	QG			LVCMOS (Note 1)
7	_	_			_	/QH	0	Various	
8		40	47		40	QH			
31	23	18	17	16	16	W	DVVD		Power Supply for the outputs on
37	27	_			_	V <sub>DDO1</sub>	PWR	_	Bank 1.
38 16	1	_	24	16	16				
43		1	24	16	16	\ \/	DIAID		Power Supply for the outputs on
43	32	_			_	$V_{DDO2}$	PWR	_	Bank 2.
24		22	21						Dower Cumply Crawed for the
39	28					V <sub>SSO1</sub>	PWR	_	Power Supply Ground for the outputs on Bank 1.
J9		_	_		_				Suputo on Bunk 1.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

F	Pin Num	bers by	Packag	e Optio	n	Pin		Pin	
#1 44-pin	#2 32-pin	#3 24-pin	#4 24-pin	#5 16-pin	#6 16-pin	Name	Pin Type	Level	Pin Function
3	2	2	2	_	_				
6	29	_		_	_	$V_{SSO2}$	PWR	_	Power Supply Ground for the outputs on Bank 2.
40	_	_		_	_				Outputs on Bank 2.
11	7	7	5	4	4				
20	15	12	11	8	8				Used for production test.
27	20	15	16	11	11	TEST	_	_	Do not connect anything to
30	24	19	18	13	13				these pins.
34	_	_	_	_	_				
12	8	8	1	5	5	\/	PWR		Care newer cumply
13	9	_		_	_	$V_{DD}$	FVVK	_	Core power supply.
21	17	13	13	3	3				
23	18	14	14	9	9	$V_{SS}$	PWR	_	Core power supply ground.
	_	_	15	10	10	۷SS	1 4414		
_	_	_		12	12				
_	_	_	_	_	_	EPAD	_	_	The exposed pad must be connected to the V <sub>SS</sub> ground plane.
15	11	_	7	_	_	OE1	I, (SE)	LVCMOS	Output Enable 1, OUT1–8 disables to tri-state, 0 = Disabled, 1 = Enabled, 45 kΩ pull-up
22	16	_	12	_	_	OE2	I, (SE)	LVCMOS	Output Enable 2, OUT9–16 disables to tri-state, 0 = Disabled, 1 = Enabled, 45 kΩ pull-up

Note 1: In the case of LVCMOS, an output pair can provide two single-ended LVCMOS outputs.

TABLE 2-2: TRUTH TABLE

Control Pin	Internal Resistor (Note 1)	0 Level (Low)	1 Level (High)
OE1	Pull-Up	Outputs QA~QD disabled to Hi Z (Tri-State)	Outputs QA~QD enabled
OE2	Pull-Up	Outputs QE~QH disabled to Hi Z (Tri-State)	Outputs QE~QH enabled
XTAL_SEL	Pull-Up	External reference clock input is selected	Crystal is selected
FSEL; (Note 2)	Pull-Up	Output = Target Frequency x2 or /2	Output = Target Frequency
PLL_BYPASS	Pull-Down	PLL frequency is connected to outputs	PLL is bypassed, Crystal or Ref-in is connected to outputs

- **Note 1:** The internal resistor sets the default logic level on the control pin when the pin is left open. Pull up will set default logic 1 and pull down will set default logic 0. When the pin is not available on a specific configuration, the level will be the default logic level.
  - 2: The FSEL pin behavior can be programmed between two types:
    - At FSEL=0 (low), the output frequency changes to multiply by 2.
    - At FSEL=0 (low), the output frequency changes to divide by 2.

The FSEL function affects all outputs the same way, all outputs change when the FSEL pin level changes.

## 3.0 PHASE NOISE PLOTS

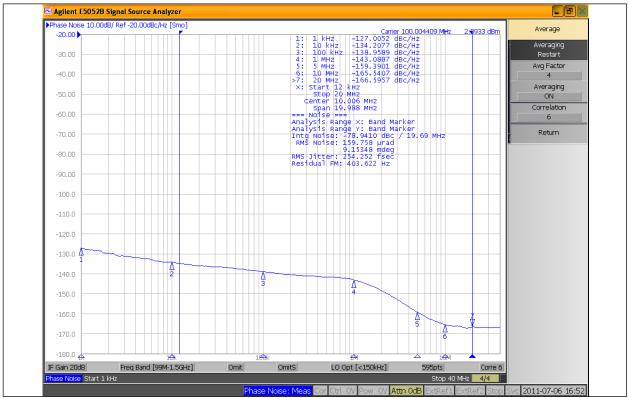


FIGURE 3-1: 100 MHz HCSL, 254 fs<sub>RMS</sub> for 12 kHz to 20 MHz Integration Range.

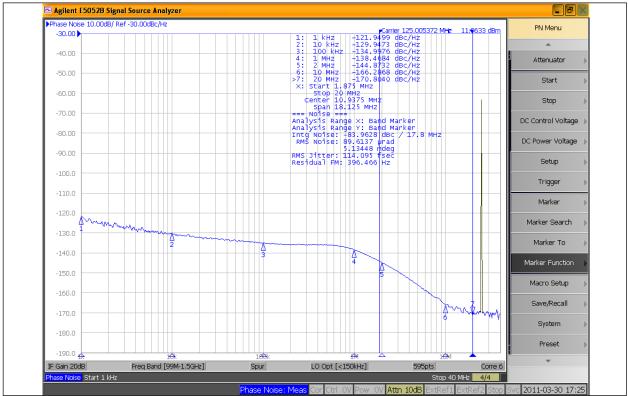


FIGURE 3-2: 125 MHz LVCMOS, 114 fs<sub>RMS</sub> for 1.875 MHz to 20 MHz Integration Range.

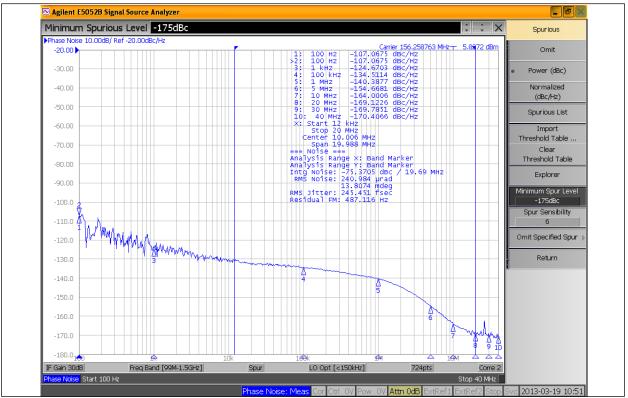


FIGURE 3-3: 156.25 MHz LVPECL, 245fs<sub>RMS</sub> for 12 kHz to 20 MHz Integration Range.

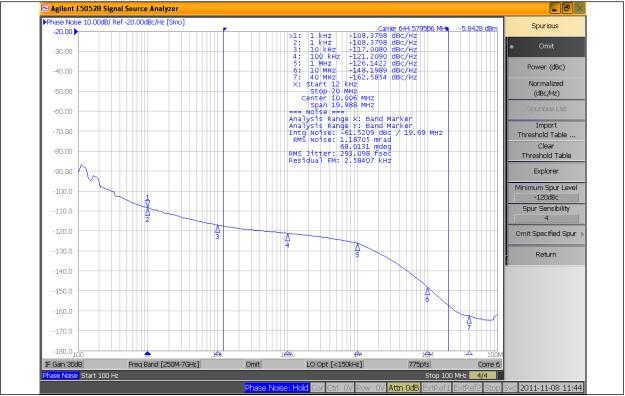


FIGURE 3-4: 644.53125 MHz LVDS, 293fs<sub>RMS</sub> for 12 kHz to 20 MHz Integration Range.

## 4.0 APPLICATION INFORMATION

## 4.1 Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF IN.

## 4.2 Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal. Crystal load capacitance is built inside the die, so no external capacitance is needed. See the Microchip application note ANTC207 for further details.

## 4.3 Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7 nF above) between the  $V_{DD}$  and  $V_{SS}$  pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from  $V_{DD}$  to capacitor and back from capacitor to  $V_{SS},$  the more effective the decoupling. Use one 4.7 nF capacitor for each  $V_{DD}$  pin on the SM802xxx.

The impedance value of the ferrite bead (FB) needs to be between  $80\Omega$  and  $240\Omega$  with a saturation current  $\geq 150$  mA.

The  $V_{DDO1}$  and  $V_{DDO2}$  pins connect directly to the  $V_{DD}$  plane. All  $V_{DD}$  pins on the SM802xxx connect to  $V_{DD}$  after the power supply filter.

## 4.4 Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a  $30\Omega$  resistor in series with the output, as close as possible to the output pin, and start a  $50\Omega$  trace on the other side of the resistor.

For differential traces, you can either use a differential design or two separate  $50\Omega$  traces. For EMI reasons, it is better to use a differential design.

LVDS can be AC-coupled or DC-coupled to its termination.

## 5.0 POWER SUPPLY FILTERING RECOMMENDATIONS

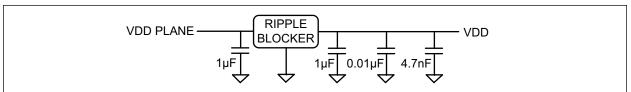


FIGURE 5-1: Preferred Filter, Using the MIC94300 or MIC94310 Ripple Blocker.

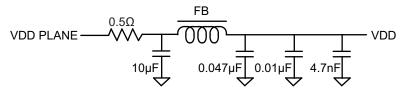


FIGURE 5-2: Alternative, Traditional Filter, Using a Ferrite Bead.

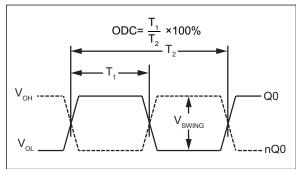


FIGURE 5-3: Duty Cycle Timing.

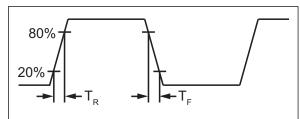


FIGURE 5-4: All Outputs Rise/Fall Time.

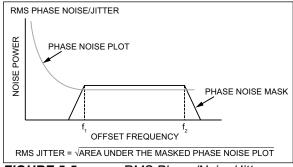


FIGURE 5-5: RMS Phase/Noise/Jitter.

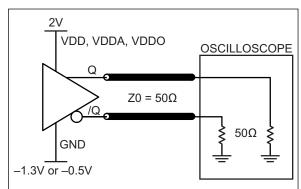


FIGURE 5-6: LVPECL Output Load and Test Circuit.

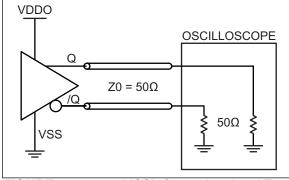


FIGURE 5-7: HCSL Output Load and Test Circuit.

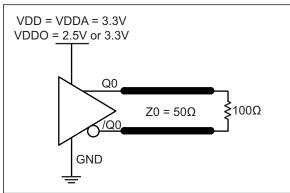


FIGURE 5-8: LVDS Output Load and Test Circuit.

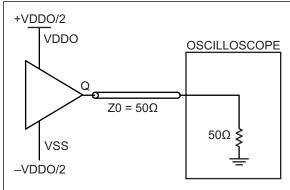


FIGURE 5-9: LVCMOS Output Load and Test Circuit.

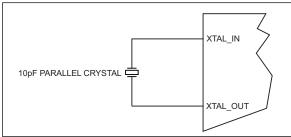


FIGURE 5-10: Crystal Input Interface.

#### 6.0 PACKAGING INFORMATION

#### 6.1 **Package Marking Information**

16-Lead VQFN\*

**XXXX WWNNN** XXXXXX Example

2003 2319E 802365 24-Lead VQFN\*

XXXX **WWNNN** XXXXXX Example

2005 41B6R

802429

32- or 44-Lead VQFN\*



2001 2410SC80000 12G4Z 802384

Example

Legend: XX...X Product code or customer-specific information

> Υ Year code (last digit of calendar year) ΥY Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') WW Alphanumeric traceability code NNN

Pb-free JEDEC® designator for Matte Tin (Sn) (e3)

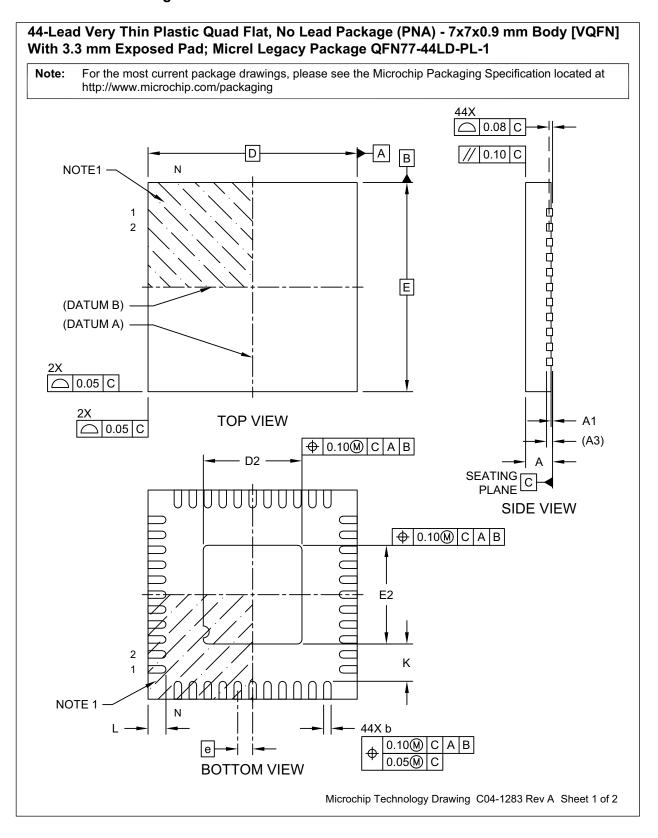
This package is Pb-free. The Pb-free JEDEC designator (@3)) can be found on the outer packaging for this package.

•, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

In the event the full Microchip part number cannot be marked on one line, it will Note: be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

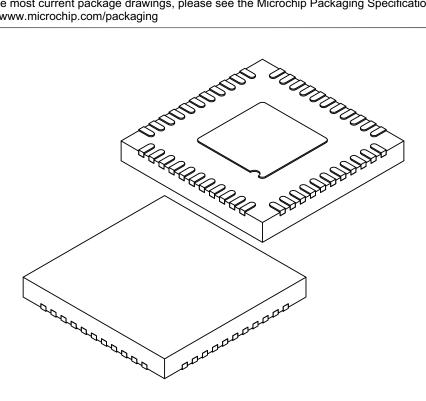
Underbar (\_) and/or Overbar (\_) symbol may not be to scale.

## 44-Lead VQFN Package Outline and Recommended Land Pattern



# 44-Lead Very Thin Plastic Quad Flat, No Lead Package (PNA) - 7x7x0.9 mm Body [VQFN] With 3.3 mm Exposed Pad; Micrel Legacy Package QFN77-44LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			S	
Dimensior	Limits	MIN	NOM	MAX	
Number of Terminals	N		44		
Pitch	е		0.50 BSC		
Overall Height	Α	0.80	0.85	0.90	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.20 REF			
Overall Length	D		7.00 BSC		
Exposed Pad Length	D2	3.20	3.30	3.40	
Overall Width	Е		7.00 BSC		
Exposed Pad Width	E2	3.20	3.30	3.40	
Terminal Width	b	0.20	0.25	0.30	
Terminal Length	Ĺ	0.55	0.60	0.65	
Terminal-to-Exposed-Pad	K	0.20	_	_	

#### Notes:

- 1. Pin 1 visual index feature may vary but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M

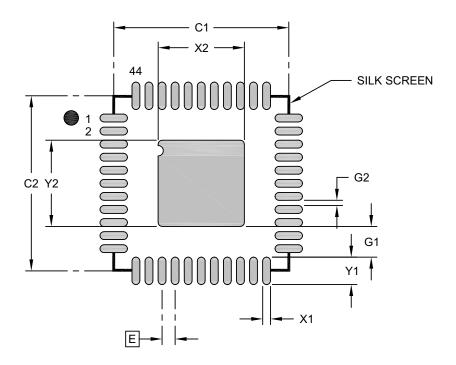
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1283 Rev A Sheet 2 of 2

# 44-Lead Very Thin Plastic Quad Flat, No Lead Package (PNA) - 7x7x0.9 mm Body [VQFN] With 3.3 mm Exposed Pad; Micrel Legacy Package QFN77-44LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	Units			S
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	Е		0.50 BSC	
Center Pad Width	X2			3.40
Center Pad Length	Y2			3.40
Contact Pad Spacing	C1		6.70	
Contact Pad Spacing	C2		6.70	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			1.05
Contact Pad to Center Pad (Xnn)	G1		1.17	
Contact Pad to Contact Pad (Xnn)	G2	0.20		

### Notes:

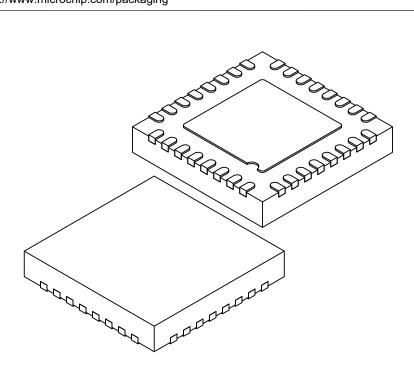
- Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. For best soldering results, please refer to current industry standard IPC-7093.

Microchip Technology Drawing C04-3283 Rev A

# 32-Lead Very Thin Plastic Quad Flat, No Lead Package (PEA) - 5x5x0.9 mm Body [VQFN] Micrel Legacy Package QFN55-32LD-PL-1 For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging 16X 0.08 C 0.10 C NOTE 1 N E (DATUM B) (DATUM A) ○ 0.10 C **TOP VIEW** Α1 0.10 C ⊕ 0.10M C A B (A3)SEATING C Κ SIDE VIEW E2 ♦ 0.10M C A B NOTE 1 Ν 32X b 0.10M C A B 0.05(M) **BOTTOM VIEW** Microchip Technology Drawing C04-1118-PEA Rev A Sheet 1 of 2

# 32-Lead Very Thin Plastic Quad Flat, No Lead Package (PEA) - 5x5x0.9 mm Body [VQFN] Micrel Legacy Package QFN55-32LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX			
Number of Terminals	N		32				
Pitch	е		0.50 BSC				
Overall Height	Α	0.80	0.85	0.90			
Standoff	A1	0.00	0.02	0.05			
Terminal Thickness	A3	0.203 REF					
Overall Length	D	5.00 BSC					
Exposed Pad Length	D2	3.05	3.10	3.15			
Overall Width	Е	5.00 BSC					
Exposed Pad Width	E2	3.05	3.10	3.15			
Terminal Width	b	0.20	0.25	0.30			
Terminal Length	L	0.35	0.40	0.45			
Terminal-to-Exposed-Pad	K	0.20	-	-			

#### Notes

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

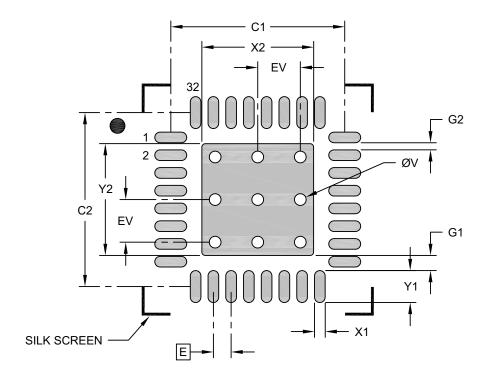
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1118-PEA Rev A Sheet 2 of 2

# 32-Lead Very Thin Plastic Quad Flat, No Lead Package (PEA) - 5x5x0.9 mm Body [VQFN] Micrel Legacy Package QFN55-32LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	Dimension Limits			MAX
Contact Pitch	Е		0.50 BSC	
Optional Center Pad Width	X2			3.15
Optional Center Pad Length	Y2			3.15
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.90
Contact Pad to Center Pad (Xnn)	G1	0.43		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

### Notes:

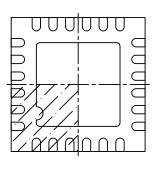
- 1. Dimensioning and tolerancing per ASME Y14.5M
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3118-PEA Rev A

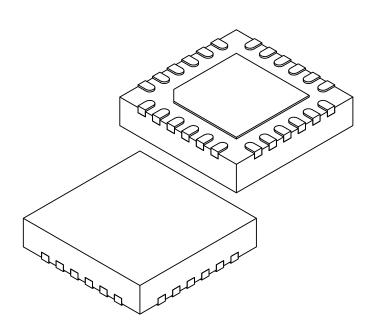
# 24-Lead Very Thin Quad Flat, No Lead Package (NYA) - 4x4x0.9 mm Body [VQFN] With 2.5 mm Exposed Pad; Micrel Legacy Package Code QFN44-24LD-PL-1 For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging 0.08 C 0.10 C D Ν NOTE1 E (DATUM B) (DATUM A) 0.05 C **TOP VIEW** ○ 0.05 C (A3)♦ 0.10 M C A B SEATING C-SIDE VIEW E2 ▼ 0.10M C A B 24X b NOTE 1 0.10M C A B 0.05(M)**BOTTOM VIEW** Microchip Technology Drawing C04-1113-NYA Rev A Sheet 1 of 2

# 24-Lead Very Thin Quad Flat, No Lead Package (NYA) - 4x4x0.9 mm Body [VQFN] With 2.5 mm Exposed Pad; Micrel Legacy Package Code QFN44-24LD-PL-1

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



**DETAIL A ALTERNATE PIN 1 INDEX** 



	Units	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Terminals	N		24		
Pitch	е		0.50 BSC		
Overall Height	Α	0.80	0.85	0.90	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.203 REF			
Overall Length	D	4.00 BSC			
Exposed Pad Length	D2	2.45	2.50	2.55	
Overall Width	Е		4.00 BSC		
Exposed Pad Width	E2	2.45	2.50	2.55	
Terminal Width	b	0.20	0.25	0.30	
Terminal Length	Ĺ	0.35 0.40 0.45			
Terminal-to-Exposed-Pad	K		0.35 REF		

#### Notes:

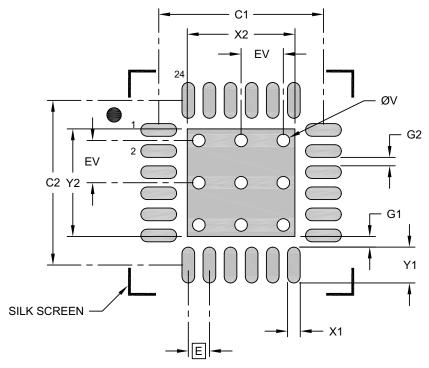
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1113-NYA Rev A Sheet 2 of 2

# 24-Lead Very Thin Quad Flat, No Lead Package (NYA) - 4x4x0.9 mm Body [VQFN] With 2.5 mm Exposed Pad; Micrel Legacy Package Code QFN44-24LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



## RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	Е		0.50 BSC	
Center Pad Width	X2			2.55
Center Pad Length	Y2			2.55
Contact Pad Spacing	C1		3.90	
Contact Pad Spacing	C2		3.90	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.25		
Contact Pad to Contact Pad (X20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

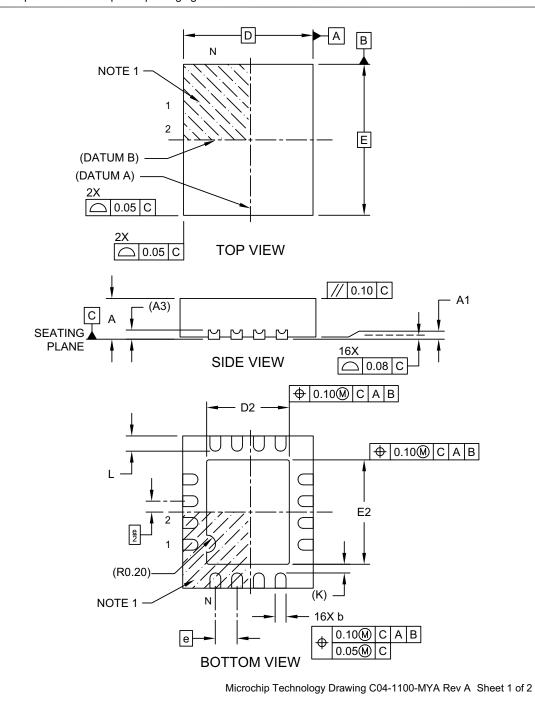
#### Notes:

- Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3113-NYA Rev A

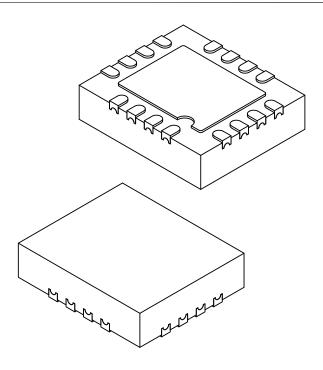
# 16-Lead Very Thin Plastic Quad Flat, No Lead Package (MYA) 3.0x3.5 mm Body [VQFN] With 1.9x2.4 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# 16-Lead Very Thin Plastic Quad Flat, No Lead Package (MYA) 3.0x3.5 mm Body [VQFN] With 1.9x2.4 mm Exposed Pad

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX	
Number of Terminals	N		16		
Pitch	е		0.50 BSC		
Overall Height	Α	0.80	0.85	0.90	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.203 REF			
Overall Length	D	3.00 BSC			
Exposed Pad Length	D2	1.85	1.90	1.95	
Overall Width	Е		3.50 BSC		
Exposed Pad Width	E2	2.35	2.40	2.45	
Terminal Width	b	0.20	0.25	0.30	
Terminal Length	Ĺ	0.30	0.35	0.40	
Terminal-to-Exposed-Pad	K		0.20 REF		

### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated

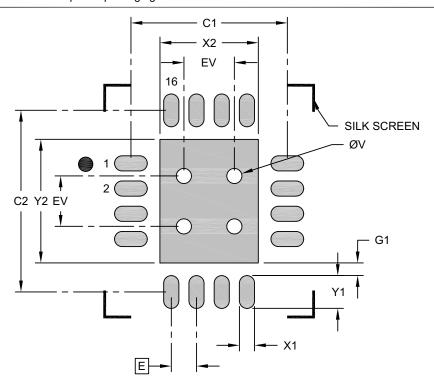
Dimensioning and tolerancing per ASME Y14.5M
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1100-MYA Rev A Sheet 2 of 2

# 16-Lead Very Thin Plastic Quad Flat, No Lead Package (MYA) 3.0x3.5 mm Body [VQFN] With 1.9x2.4 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# RECOMMENDED LAND PATTERN

	MILLIMETERS			
Dimension	Units	MIN	NOM	MAX
Contact Pitch	Е		0.50 BSC	!
Center Pad Width	X2			1.95
Center Pad Length	Y2			2.45
Contact Pad Spacing	C1		3.10	
Contact Pad Spacing	C2		3.60	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.65
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

## Notes:

- Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- 2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3100-MYA Rev A



NOTES:

## APPENDIX A: REVISION HISTORY

## Revision A (March 2019)

- Converted Micrel document SM802xxx to Microchip data sheet DS20006176B.
- · Minor text changes throughout.
- Updated the Crystal and Reference Input frequency ranges in the Features section and in Crystal Characteristics table.
- Updated ESR value in Crystal Characteristics table.
- Updated the 12 kHz to 20 MHz Phase Jitter to 265 fs in the Features and in LVPECL AC Electrical Characteristics (Note 1, Note 2, Note 3, Note 4).
- Updated Output Frequency minimum and typical Phase Jitter in LVDS AC Electrical Characteristics (Note 1, Note 2, Note 3, Note 4), HCSL AC Electrical Characteristics (Note 1, Note 2, Note 3, Note 4), and LVCMOS AC Electrical Characteristics (Note 1, Note 2, Note 3, Note 4).
- Corrected the impedance values for using a ferrite bead in Power Supply Decoupling section.

## Revision B (September 2024)

- Added PCIe Compliance bullet to Features.
- · Updated Gigabit Ethernet bullet in Applications.
- Updated all package drawing outlines and added the Package Marking Information section.
- Changed all instances of QFN in the document to VQFN.
- Added PCIe Refclk Jitter value to LVDS AC Electrical Characteristics (Note 1, Note 2, Note 3, Note 4) and HCSL AC Electrical Characteristics (Note 1, Note 2, Note 3, Note 4).



NOTES:

# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO. X X X - X - X | Device Voltage Option Package Type Temperature Processing

**Device:** SM802xxx: Flexible Ultra-Low Jitter Clock Synthesizer

Voltage Option: U = 2.5V/3.3V

Package Type: M = 44-, 32-, 24-, or 16-VQFN; see the Package

Options Table (Note 1).

**Temperature:** G =  $-40^{\circ}$ C to  $+85^{\circ}$ C (NiPdAu Lead Free)

Special Blank = Tray

**Processing:** TR = Tape and Reel

### Examples:

a) SM802xxxUMG:

Flexible Ultra-Low Jitter Clock Synthesizer, 2.5V/3.3V Voltage Option, VQFN Package, -40°C to +85°C Temperature Range, Tray

b) SM802xxxUMG-TR:

Flexible Ultra-Low Jitter Clock Synthesizer, 2.5V/3.3V Voltage Option, VQFN Package, -40°C to +85°C Temperature Range, Tape & Reel

### Package Options Table (Note 1)

Package Option	VQFN Package	# of Outputs	XTAL	REF_IN	XTAL_SEL	FSEL	OE1 OE2	PLL BYPASS
#1	44-Pin 7x7	8 Diff.	Yes	Yes	Yes	Yes	Yes	Yes
#2	32-Pin 5x5	4 Diff.	Yes	Yes	Yes	Yes	Yes	Yes
#3	24-Pin 4x4	4 Diff.	Yes	Yes	Yes	No	No	Yes
#4	24-Pin 4x4	2 Diff.	Yes	Yes	Yes	Yes	Yes	Yes
#5	16-Pin 3x3.5	2 Diff.	No	Yes	No	Yes	No	No
#6	16-Pin 3x3.5	2 Diff.	Yes	No	No	No	No	No

Note 1: Use the web tool at <a href="http://clockworks.microchip.com/micrel/">http://clockworks.microchip.com/micrel/</a> to determine the desired configuration.



NOTES:

#### Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions
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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not
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  continuously improving the code protection features of our products.

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