TEA2209T

Active bridge rectifier controller

Rev. 1.1 — 14 April 2021 | Product data sheet

1 General description

The TEA2209T is a product of a new generation of active bridge rectifier controllers replacing the traditional diode bridge.

Using the TEA2209T with low-ohmic high-voltage external MOSFETs significantly improves the efficiency of the power converter as the typical rectifier diode-forward conduction losses are eliminated. Efficiency can improve up to about 1.4 % at 90 V (AC) mains voltage.

The TEA2209T is designed in a silicon-on insulator (SOI) process.

2 Features and benefits

2.1 Efficiency features

- Forward conduction losses of the diode rectifier bridge are eliminated
- Very low IC power consumption (2 mW)

2.2 Application features

- Integrated high-voltage level shifters
- Directly drives all four rectifier MOSFETs
- Very low external part count
- Integrated X-capacitor discharge (2 mA)
- Self-supplying
- Full-wave drive improving total harmonic distortion (THD)
- S016 package

2.3 Control features

- Disable function for all external power FETs
- Undervoltage lockout (UVLO) for high-side and low-side drivers
- Drain-source overvoltage protection for all external power MOSFETs
- Gate pull-down currents at start-up for all external power MOSFETs

3 Applications

The TEA2209T is intended for power supplies with a boost-type power-factor controller as a first stage. The second stage can be a resonant controller, a flyback controller, or any other controller topology. It can be used in all power supplies requiring high efficiency:

- Adapters
- Power supplies for desktop PC and all-in-one PC
- Power supplies for television
- Power supplies for servers

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA2209T/1	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5 Marking

Table 2. Marking

Type number	Marking code
TEA2209T/1	TEA2209T

6 Block diagram

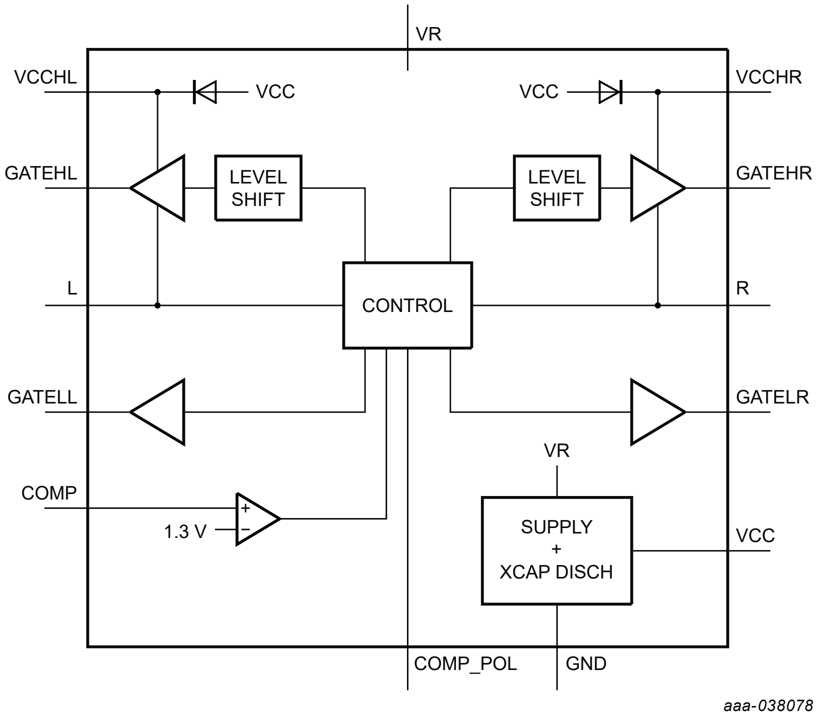


Figure 1. Block diagram

7 Pinning information

7.1 Pinning

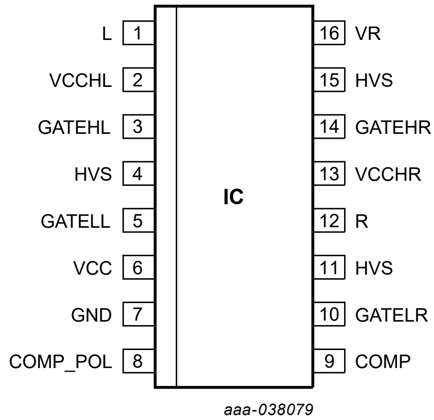


Figure 2. Pinning diagram (SOT109-1)

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
L	1	left input, source of upper left MOSFET
VCCHL	2	left high-side floating supply
GATEHL	3	gate driver left high side
HVS	4	high-voltage spacer; not to be connected
GATELL	5	gate driver left low side
VCC	6	supply voltage
GND	7	ground
COMP_POL	8	comparator polarity setting
COMP	9	comparator input
GATELR	10	gate driver right low side
HVS	11	high-voltage spacer; not to be connected
R	12	right input, source of upper right MOSFET
VCCHR	13	right high-side floating supply
GATEHR	14	gate driver right high side
HVS	15	high-voltage spacer; not to be connected
VR	16	rectified mains voltage

8 Functional description

8.1 Introduction

The TEA2209T is a controller IC for an active bridge rectifier. It can directly drive the four MOSFETs in an active bridge. Figure 3 shows a typical configuration. Since the output is a rectified sine wave, a boost-type power-factor circuit must follow the application.

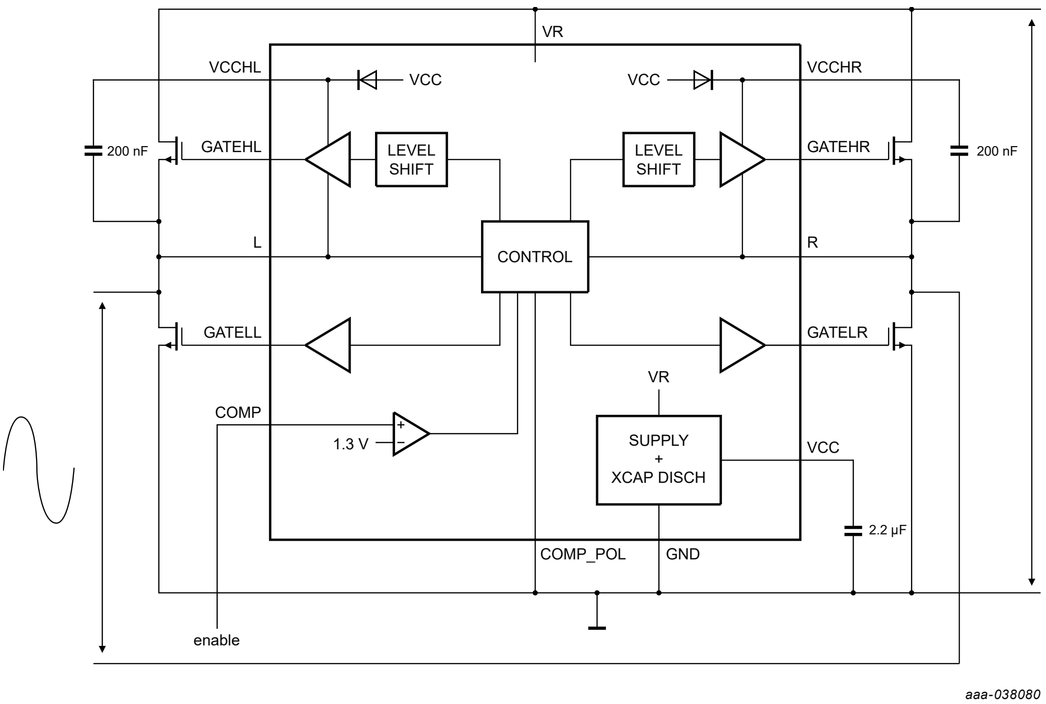


Figure 3. Typical configuration

8.2 Operation

The control circuit of the TEA2209T senses the polarity of the mains voltage between pins L and R. Depending on the polarity, diagonal pairs of power MOSFETs are switched on or off. Depending on the slope polarity, the comparator in the control circuit, which compares the L and R voltages, has thresholds of +250 mV and −250 mV.

The gate drivers are high-current rail-to-rail MOS output drivers. An on-chip supply circuit which draws current from the rectified sine-wave pin VR generates the gate driver voltage. After a zero-crossing of the mains voltage, the supply capacitor C_{VCC} is charged to the regulation level V_{reg}. Then the discharge state is entered. The resulting power dissipation from the mains voltage is about 1 mW, excluding gate charge losses of the external power MOSFETs. These gate charge losses typically add a 1 mW dissipation.

At start-up, the body diodes of the power MOSFETs act as a traditional diode bridge. They cause a peak rectified voltage at pin VR. From this high voltage, the supply capacitor is first charged to the V_{start} voltage and then enters the start-up state. After a next zero-crossing of the mains voltage, the supply capacitor is charged to V_{reg} in the charging state. When the voltage at the supply capacitor exceeds V_{dis}, the gate driver outputs are enabled. The high-side drivers start up later than the low-side drivers. The floating supplies must be charged first and the drain-source voltage of the high-side power MOSFETs must be less than the drain-source protection voltage. When all drivers are active, the MOSFETs take over the role of the diodes. The result is a much lower power loss than with a passive diode rectifier bridge.

In the discharge state, when the mains voltage is disconnected, the internal bias current discharges the supply capacitor. When the voltage at pin VCC drops to below V_{dis} the X-capacitor discharge state is entered, which draws a 2 mA current from pin VR to discharge the X-capacitor. The waiting time, t_d until the X-capacitor discharge starts is:

$$t_d = C_{VCC} * \left(V_{reg} - V_{dis}\right) / 23\,\mu A = 0.11E6 * C_{VCC} \quad (1)$$

Using a typical value of 2.2 μF for C_{VCC} yields about 0.24 s. While the VR pin discharges the X-capacitor, the mains can be reconnected. In that case, the charge mode is entered again.

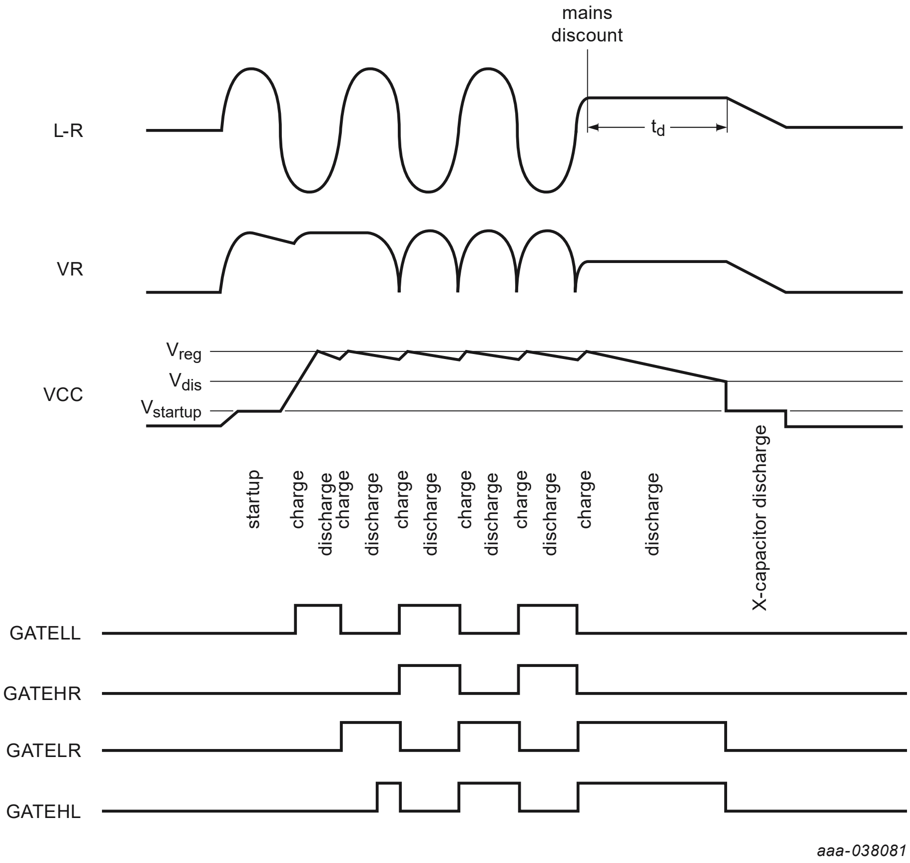


Figure 4. TEA2209T signals

Table 4. TEA2209T states

State	Description	I_{VR}	I_{VCC}
start-up	supply capacitor kept stable at 4.8 V	2 mA	0
charge	supply capacitor is charged from pin VR with 2 mA	+2 mA	−2 mA
discharge	internal bias currents and gate charge losses discharge the supply capacitor	1 µA	20 µA
X-capacitor discharge	supply capacitor and X-capacitor at pin VR are discharged by 2 mA	+2 mA	−2 mA

When there is hardly any load current or no load current at all on pin VR, the dissipation in the capacitor connected between pin VR and GND, although very low by itself, can contribute relatively much to the total low-load power consumption when the TEA2209T is enabled. So, an external control signal at pin COMP can disable the gate drivers. A comparator with 1.3 V input threshold and 350 mV hysteresis is used at pin COMP. Pin COMP_POL can select the polarity of the comparator. Pin COMP has an internal pull-up and pull-down current which pin COMP_POL selects. The selection is such that with an open pin at COMP, the TEA2209T is enabled. Pin COMP_POL has an internal 0.5 µA pull-down current. Connect pin COMP_POL to either GND or VCC. Do not drive the COMP_POL pin with an external signal.

Table 5. COMP functionality

COMP_POL = GND	COMP_POL = VCC
COMP = low: all gate drivers disabled; internal pull-up current = 0.25 µA	COMP = low; all gate drivers enabled; internal pull-down current = 0.5 µA

8.3 Protections

8.3.1 Gate pull-down

All gate driver outputs have a pull-down circuit. It ensures that, if a driver supply voltage is lower than the undervoltage lockout level, the discharge of the gate driver output discharges to less than 2 V.

8.3.2 Power MOSFET drain-source protection

If the drain-source voltage of the external power MOSFET exceeds V_{VCC} − 2 V (low side), V_{VCCHL} − 3.5 V (high side left), or V_{VCCHR} − 3.5 V (high side right), all gate driver outputs are disabled. Disabling the gate driver outputs avoids high dissipation and high current peaks in the power MOSFETs during start-up.

8.3.3 Minimum mains voltage

Only when the voltage at either node L or R exceeds 22 V, the charge state is entered.

9 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 7). Positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated. Current ratings are valid provided the other ratings are not violated. The internal IC clearances comply with all NXP design standards and regulations. Moreover, at final testing every chip is checked against the maximum voltage rating in the data sheet.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VR}	voltage on pin VR	operating	−0.4	440	V
		mains transient: maximum 10 minutes over lifetime	−0.4	700	V
V_{VCCHL}	voltage on pin VCCHL	operating	−0.4	440	V
		mains transient: maximum 10 minutes over lifetime	−0.4	700	V
V_{VCCHR}	voltage on pin VCCHR	operating	−0.4	440	V
		mains transient: maximum 10 minutes over lifetime	−0.4	700	V
V_L	voltage on pin L	operating	−5	+440	V
		mains transient: maximum 10 minutes over lifetime	−5	+700	V
V_R	voltage on pin R	operating	−5	+440	V
		mains transient: maximum 10 minutes over lifetime	−5	+700	V
$\Delta V_{(VR-L)}$	voltage difference between pins VR and L	operating	−10	+440	V
		mains transient: maximum 10 minutes over lifetime	−10	+700	V
$\Delta V_{(VR-R)}$	voltage difference between pins VR and R	operating	−10	+440	V
		mains transient: maximum 10 minutes over lifetime	−10	+700	V
V_{GATEHR}	voltage on pin GATEHR	operating	−5	+440	V
		mains transient: maximum 10 minutes over lifetime	−5	+700	V
V_{GATEHL}	voltage on pin GATEHL	operating	−5	+440	V
		mains transient: maximum 10 minutes over lifetime	−5	+700	V

Table 6. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 7). Positive currents flow into the chip. Voltage ratings are valid provided other ratings are not violated. Current ratings are valid provided the other ratings are not violated. The internal IC clearances comply with all NXP design standards and regulations. Moreover, at final testing every chip is checked against the maximum voltage rating in the data sheet.

Symbol	Parameter	Conditions	Min	Max	Unit
SR_{max}	maximum slew rate	pins VR, L, R, VCCHL, VCCHR, GATEHL, GATEHR	-	50	V/ns
V_{VCC}	voltage on pin VCC		−0.4	14	V
V_{GATELR}	voltage on pin GATELR		−0.4	14	V
V_{GATELL}	voltage on pin GATELL		−0.4	14	V
V_{COMP}	voltage on pin COMP		−0.4	14	V
V_{COMP_POL}	voltage on pin COMP_POL		−0.4	14	V
$V_{DD(float)}$	float supply voltage	pins GATEHL-L, GATEHR-R, VCCHR-R, VCCHL-L	−0.4	14	V
General					
T_j	junction temperature		−40	+125	°C
T_{stg}	storage temperature		−55	+150	°C
Electrostatic discharge (ESD)					
V_{ESD}	electrostatic discharge voltage	human body model (HBM)			
		pins VR, L, R, VCCHL, VCCHR, GATEHL, and GATEHR	−1000	+1000	V
		other pins	−2000	+2000	V
		charge device model (CDM)	−500	+500	V

10 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	in free air [1]	46	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; 1-layer PCB [1]	148	K/W
		in free air; 4-layer PCB; JEDEC test board [1]	106	K/W

[1] Given thermal resistance values are based on simulation results.

11 Characteristics

Table 8. Characteristics

T_{amb} = 25 °C; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VR pin						
I_{on}	on-state current	charging state; X-capacitor discharge state; start-up state	1.5	2	2.75	mA
I_{off}	off-state current	discharge state	0.5	0.8	1.2	µA
V_{start}	start voltage	high-voltage start-up	9	-	-	V
VCC pin						
I_{dch}	discharge current	X-capacitor discharge	3	4	5.5	mA
I_{bias}	bias current	discharge state	15	23	33	µA
I_{ch}	charge current	charge state	1.5	2	2.75	mA
V_{UVLO}	undervoltage lockout voltage		3.6	4.2	4.9	V
$V_{startup}$	start-up voltage	start-up state	4.3	4.8	5.3	V
V_{dis}	disable voltage	high level	9.2	9.7	10.2	V
		hysteresis	1.1	1.5	1.8	V
V_{regd}	regulated output voltage		10.2	10.7	11.2	V
Floating supply pins (VCCHL, VCCHR)						
$I_{I(VCCHL)}$	input current on pin VCCHL	V_L = 0 V	1.4	1.8	2.5	µA
		V_L = 200 V	4	7	12	µA
$I_{I(VCHHR)}$	input current on pin VCCHR	V_L = 0 V	1.4	1.8	2.5	µA
		V_L = 200 V	4	7	12	µA
$V_{DD(float)UVLO}$	undervoltage lockout float supply voltage		3.6	4.2	5.0	V
$V_{d(bs)}$	bootstrap diode voltage	current on diode = 1 mA	0.8	1	1.3	V
Gate driver output pins (GATELL, GATELR, GATEHL, GATEHR)						
I_{source}	source current	V_{VCC} = 12 V; V_{GATELL} = V_{GATEHL} = 6 V; V_{GATELR} = V_{GATEHR} = 6 V [1]	125	200	400	mA
I_{sink}	sink current	V_{VCC} = 12 V; V_{GATELL} = V_{GATEHL} = 6 V; V_{GATELR} = V_{GATEHR} = 6 V [1]	150	200	500	mA
I_{pd}	pull-down current	off-state current; V_{VCC} = 2 V; V_{GATELL} = V_{GATEHL} = 2 V; V_{GATELR} = V_{GATEHR} = 2 V	100	200	250	µA
R_{on}	on-state resistance		11	15	20	Ω
R_{off}	off-state resistance		7	10	14	Ω
$V_{prot(G)}$	gate driver protection voltage	VR-VCCHR; VR-VCCHL	−5	−3.5	−2	V
		L-VCC; R-VCC	−3	−2.3	−1	V

Table 8. Characteristics...*continued*

T_{amb} = 25 °C; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Control circuit (pins L and R)						
V_{th}	threshold voltage	peak detector threshold voltage	15	22	32	V
I_{det}	detection current	peak detector current	0.4	0.5	0.6	μA
V_{offset}	offset voltage	zero-crossing comparator offset voltage	150	250	350	mV
t_d	delay time	zero-crossing comparator delay time				
		dV/dt = 0.1 V/μs [2]	1200	1500	2500	ns
		dV/dt = 10 V/μs [2]	550	700	1200	ns
Disable circuit (pin COMP and COMP_POL)						
$V_{th(COMP)}$	threshold voltage on pin COMP	high level	1.2	1.3	1.4	V
		hysteresis	0.28	0.35	0.42	V
$I_{i(COMP)}$	input current on pin COMP	pull-up current	0.18	0.25	0.32	μA
		pull-down current	0.2	0.44	0.7	μA
$V_{th(COMP\_POL)}$	threshold voltage on pin COMP_POL	high level	3.5	4.2	5.0	V
		hysteresis	0.2	0.27	0.4	V
$I_{i(COMP\_POL)}$	input current on pin COMP_POL	pull-down current	0.33	0.5	0.65	μA

[1] Covered by correlating measurement.
[2] Guaranteed by design and validation.

12 Application information

A switched-mode power supply (SMPS) with the TEA2209T typically consists of a mains filter in front of the TEA2209T followed by a boost-type power factor controller. A resonant controller, flyback controller, or any other topology can follow this boost-type PFC.

Special attention must be given to the connection of the VR, L, and R pins of the TEA2209T. Mains transients or surges must be limited to voltages below 700 V.

If a 2 kV ESD rating is required on all pins, a 100 pF capacitor from pins L, R, and VR to ground can be used to achieve the 2 kV ESD.

Typical values for the three external capacitors are 1 μF to 2.2 μF (supply capacitor) and 100 nF to 220 nF (bootstrap capacitors). Supply capacitors with higher values increase the delay time (t_d) for the X-capacitor discharge. They may also increase the dissipation because the supply capacitor C_{VCC} may not be charged every half-mains cycle. Bootstrap capacitors with lower value may cause a voltage drop that is too high because of the gate charge losses.

When there is hardly any load current or no load current at all on pin VR, the dissipation in the capacitor connected between pins VR and GND, although very low by itself, can contribute relatively much to the total low-load power consumption when the TEA2209T is enabled. So, to minimize power consumption, the TEA2209T can be switched off at low power. Switching off at low power can be done in several ways. One option is a filter connected to the PFC gate signal. The pin COMP_POL is grounded such that, at a low duty cycle of the PFC signal, the voltage at pin COMP is low. It disables the TEA2209T.

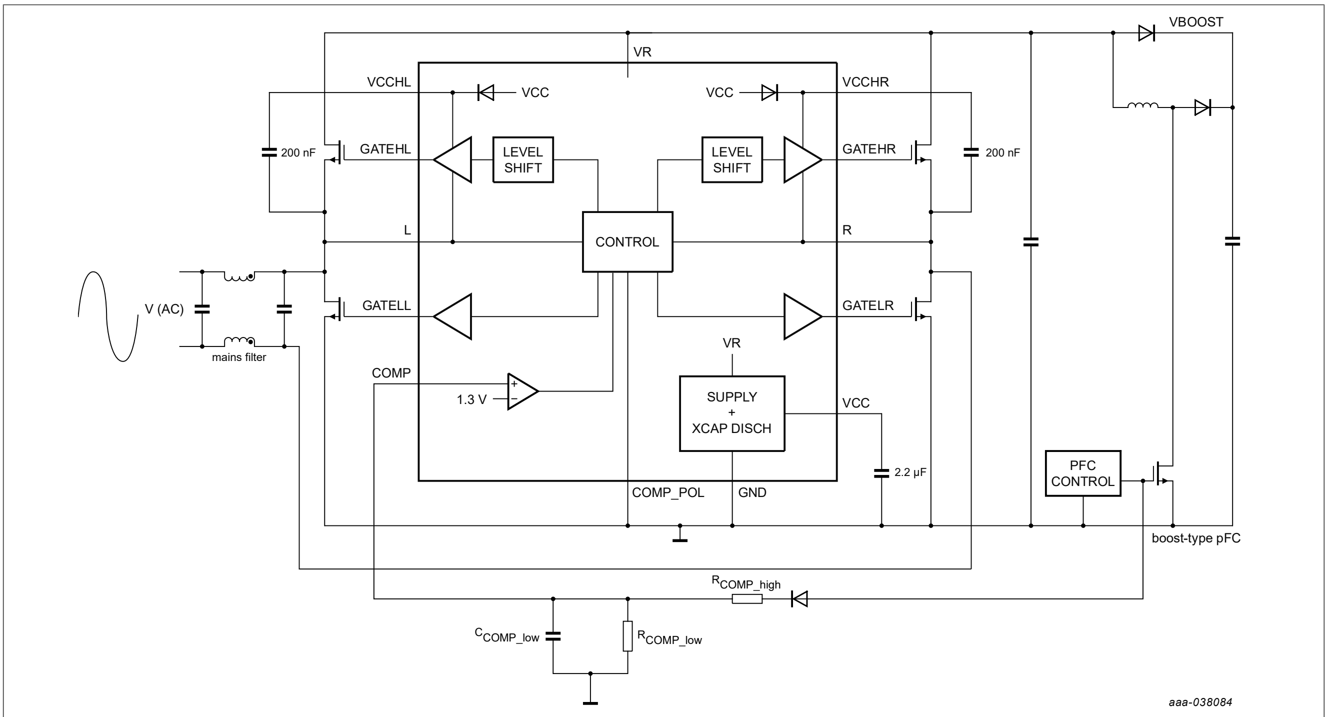


Figure 5. Application with mains filter, boost-type PFC, and low-power disable function via PFC gate signal

A microcontroller can also disable the TEA2209T. An application with a microcontroller is shown in Figure 6. Pin COMP_POL is connected to VCC. If pin COMP is high, the TEA2209T is disabled.

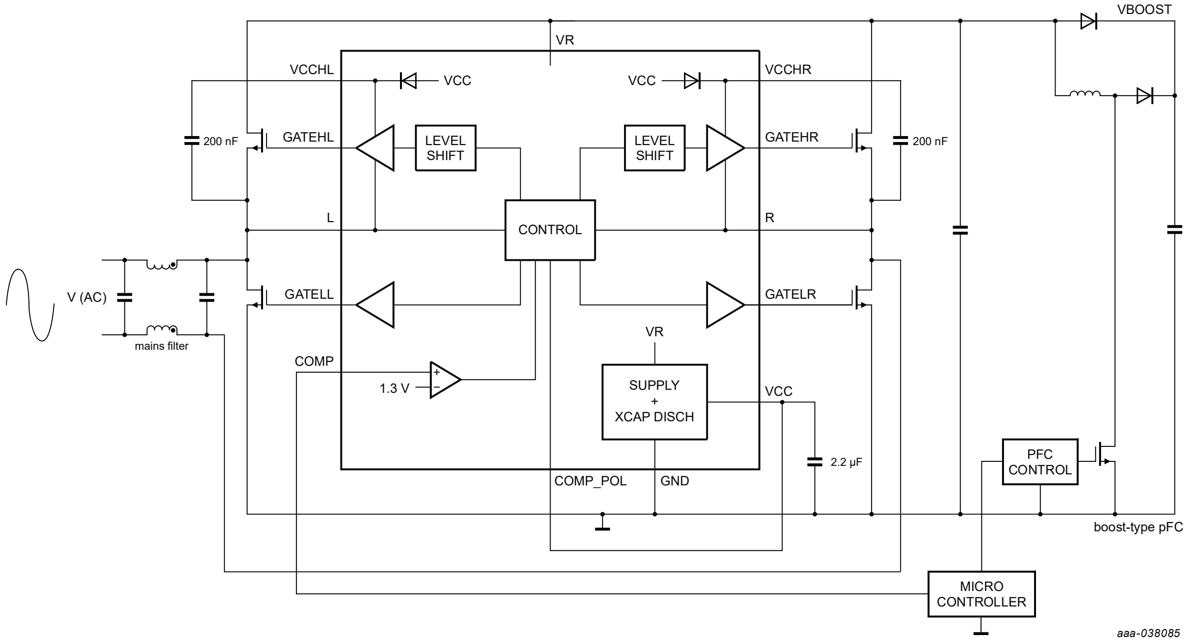
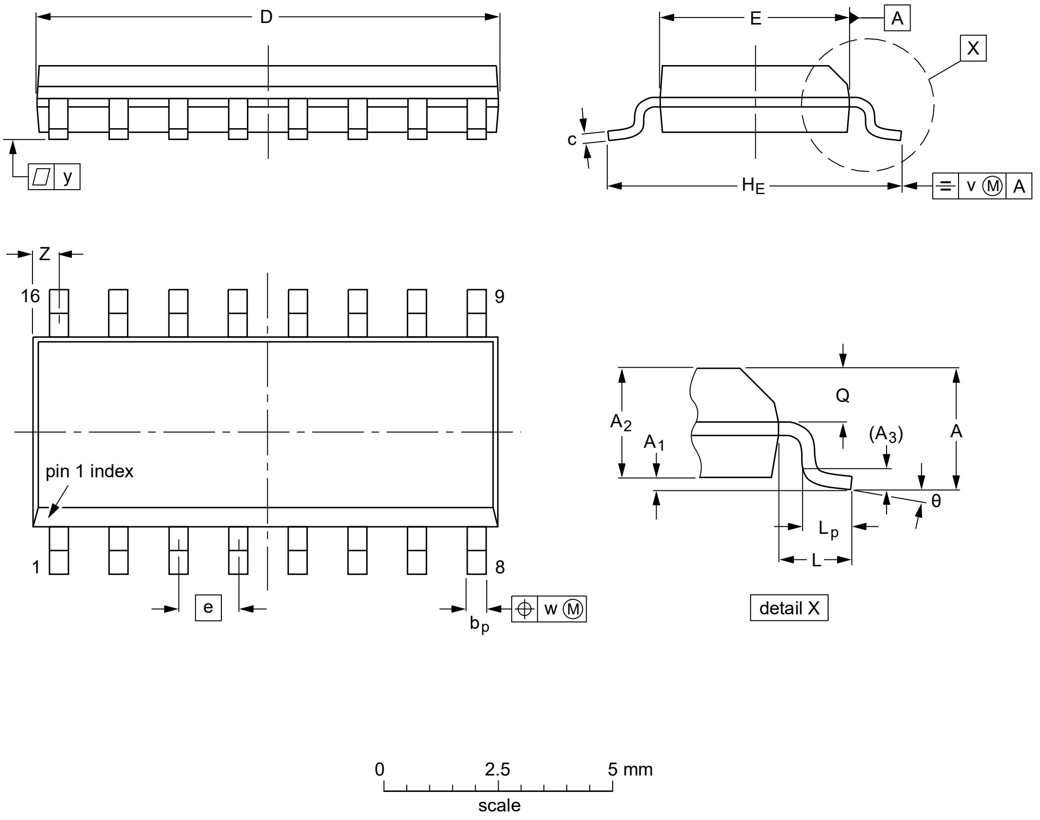


Figure 6. Application with mains filter, boost-type PFC, and low-power disable function via microcontroller

13 Package outline

Table 9.

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Figure 7. Package outline SOT109-1 (SO16)

14 Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	change device model
ESD	electrostatic discharge
HBM	human body model
MOSFET	metal–oxide–semiconductor field-effect transistor
MOV	metal-oxide varistor
PFC	power-factor controller
SMPS	switched-mode power supply
SOI	silicon-on insulator
THD	total harmonic distortion
UVLO	undervoltage lockout

15 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA2209T v.1.1	20210414	Product data sheet	-	TEA2209T v.1
Modifications:	• Section 11 "Characteristics" has been updated.			
TEA2209T v.1	20210324	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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