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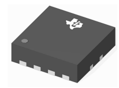


ADS7826
ADS7827
ADS7829

SLAS388 – JUNE 2003

10/8/12-BIT HIGH SPEED 2.7 V microPOWER™ SAMPLING ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **High Throughput at Low Supply Voltage ($2.7\ V\ V_{CC}$)**
  – ADS7829: 12-bit 125 KSPS
  – ADS7826: 10-bit 200 KSPS
  – ADS7827: 8-bit 250 KSPS
- **Very Wide Operating Supply VoltageL: 2.7 V to 5.25 V (as Low as 2.0 V With Reduced Performance)**
- **Rail-to-Rail, Pseudo Differential Input**
- **Wide Reference Voltage: 50 mV to V_{CC}**
- **Micropower Auto Power-Down:**
  – Less Than 60 µW at 75 kHz, 2.7 V V_{CC}
- **Low Power Down Current: 3 µA Max**
- **Ultra Small Chip Scale Package: 8-pin 3 x 3 PDSO (SON, Same Size as QFN)**
- **SPI™ Compatible Serial Interface**

APPLICATIONS

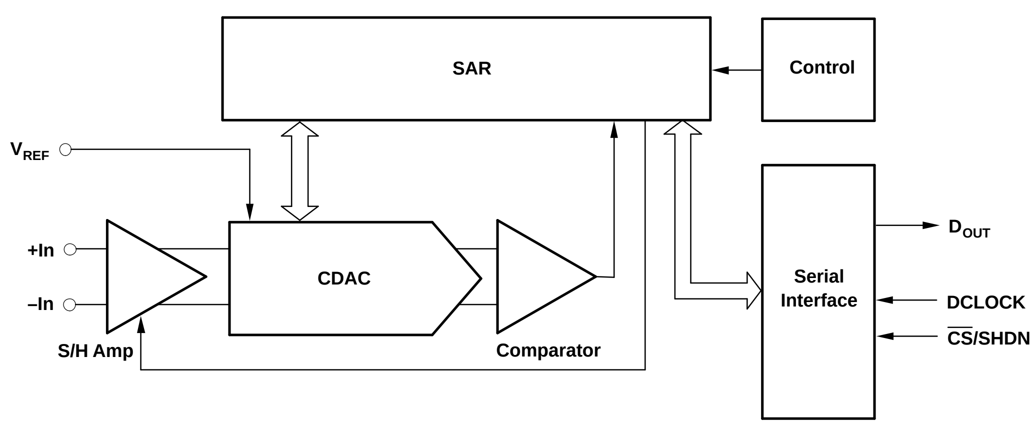
- **Battery Operated Systems**
- **Remote Data Acquisition**
- **Isolated Data Acquisition**
- **Simultaneous Sampling, Multichannel Systems**

DESCRIPTION

The ADS7826/27/29 is a family of 10/8/12-bit sampling analog-to-digital converters (A/D) with assured specifications at 2.7-V supply voltage. It requires very little power even when operating at the full sample rate. At lower conversion rates, the high speed of the device enables it to spend most of its time in the power down mode— the power dissipation is less than 60 µW at 7.5 kHz.

The ADS7826/27/29 also features operation from 2.0 V to 5 V, a synchronous serial interface, and a differential input. The reference voltage can be set to any level within the range of 50 mV to V_{CC}.

Ultra-low power and small package size make the ADS7826/27/29 family ideal for battery operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multichannel systems, and isolated data acquisition. The ADS7826/27/29 family is available in a 3 x 3 8-pin PDSO (SON, same size as QFN) package.



microPOWER is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)		PACKAGE (1)	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING (2)	ORDERING NUMBER	TRANSPORT MEDIA
	INTEGRAL	DIFFERENTIAL					
ADS7829I	±2	±2	SON-8	-40°C to 85°C	F29	ADS7829IDRBR	Tape and reel
ADS7829IB	±1.25	-1/1.25	SON-8	-40°C to 85°	F29	ADS7829IBDRBR	Tape and reel
ADS7826I	±1	±1	SON-8	-40°C to 85°C	F26	ADS7826IDRBR	Tape and reel
ADS7827I	±1	±1	SON-8	-40°C to 85°C	F27	ADS7827IDRBR	Tape and reel
ADS7829I	±2	±2	SON-8	-40°C to 85°C	F29	ADS7829IDRBT	Tape and reel
ADS7829IB	±1.25	-1/1.25	SON-8	-40°C to 85°C	F29	ADS7829IBDRBT	Tape and reel
ADS7826I	±1	±1	SON-8	-40°C to 85°C	F26	ADS7826IDRBT	Tape and reel
ADS7827I	±1	±1	SON-8	-40°C to 85°C	F27	ADS7827IDRBT	Tape and reel

(1) For detail drawing and dimension table, see end of this data sheet or package drawing file on web.
(2) Performance Grade information is marked on the reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

V_{CC}	6 V
Analog input	-0.3 V to (V_{CC} + 0.3 V)
Logic input	-0.3 V to 6 V
Case temperature	100°C
Junction temperature	150°C
Storage temperature	125°C
External reference voltage	5.5 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

At -40°C to 85°C, V_{CC} = 2.7 V, V_{ref} = 2.5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	ADS7829IB			ADS7829			ADS7826I			ADS7827I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT														
Full-scale input span	+In - (-In)	0		V_{ref}	0		V_{ref}	0		V_{ref}	0		V_{ref}	V
Absolute input range	+In	-0.2		V_{CC} +0.2	-0.2		V_{CC} +0.2	-0.2		V_{CC} +0.2	-0.2		V_{CC} +0.2	V
	-IN	-0.2		1.0	-0.2		1.0	-0.2		1.0	-0.2		1.0	V
Capacitance			25			25			25			25		pF
Leakage current			±1			±1			±1			±1		µA
SYSTEM PERFORMANCE														
Resolution			12			12			10			8		Bits
No missing codes		12			11			10			8			Bits
Integral linearity error		-1.25	±0.4	1.25	-2	±0.8	2	-1	±0.3	1	-1	±0.2	1	LSB (1)
Differential linearity error		-1	±0.4	1.25	-2	±0.8	2	-1	±0.3	1	-1	±0.2	1	LSB
Offset error		-3	±0.3	3	-3	±0.6	3	-2	±0.4	2	-1	±0.4	1	LSB
Gain error		-2	±0.3	2	-2	±0.6	2	-1	±0.3	1	-1	±0.2	1	LSB
Noise			33			33			33			33		µVrms
Power supply rejection			82			82			94			98		dB
SAMPLING DYNAMICS														
Conversion time				12			12			10			8	DCLOCK Cycles
Acquisition time			1.5			1.5			1.5			1.5		DCLOCK Cycles
f_{DCLOCK}			16 x fsample			16 x fsample			14 x fsample			12 x fsample		kHz
Throughput (sample rate) fsample	2.7 V ≤ V_{CC} ≤ 5.25 V (2)			125			125			200			250	kHz
	2.0 V ≤ V_{CC} < 2.7 V (3) (2)			75			75			85			100	kHz
DYNAMIC CHARACTERISTICS														
Total harmonic distortion			-82			-80			-78			-72		dB
SINAD	V_{IN} = 2.5 Vpp at 1 kHz		72			70			62			50		dB
Spurious free dynamic range (SFDR)	V_{IN} = 2.5 Vpp at 1 kHz		85			82			81			68		dB
REFERENCE INPUT														
Voltage range	2.7 V ≤V_{CC}≤3.6 V	0.05		V_{CC}-0.2	0.05		V_{CC}-0.2	0.05		V_{CC}-0.2	0.05		V_{CC}-0.2	V
Resistance	$\overline{CS}$ = GND, f_{SAMPLE} = 0 Hz		5			5			5			5		GΩ
	$\overline{CS}$ = V_{CC}		5			5			5			5		GΩ
Current drain	Full speed at V_{ref}/2		12	60		12	60		20	100		24	120	µA
	f_{SAMPLE} = 7.5 kHz		0.8			0.8			0.8			0.8		µA
	$\overline{CS}$ = V_{CC}		0.001	3		0.001	3		0.001	3		0.001	3	µA
DIGITAL INPUT/OUTPUT														
Logic family			CMOS			CMOS			CMOS			CMOS		
Logic levels														
V_{IH}	I_{IH} = +5 µA	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
V_{IL}	I_{IL} = +5 µA	-0.3		0.8	-0.3		0.8	-0.3		0.8	-0.3		0.8	V

(1) LSB means Least Significant Bit and is equal to $V_{ref} / 2^N$ where N is the resolution of ADC. For example, with V_{ref} equal to 2.5 V, one LSB is 0.61 mV for a 12 bit ADC (ADS7829).
(2) See the Typical Performance Curves for V_{CC} = 5 V and V_{ref} = 5 V.
(3) The maximum clock rate of the ADS7826/27/29 are less than 1.2 MHz at 2 V ≤V_{CC} <2.7 V. The recommended regerence voltage is between 1.25 V to 1.024 V.

SPECIFICATIONS (continued)

At -40°C to 85°C, V_{CC} = 2.7 V, V_{ref} = 2.5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	ADS7829IB			ADS7829			ADS7826I			ADS7827I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = -250 µA	2.2			2.1			2.1			2.1			V
V_{OL}	I_{OL} = 250 µA			0.4			0.4			0.4			0.4	V
Data format		Straight binary			Straight binary			Straight binary			Straight binary			
POWER SUPPLY REQUIREMENTS														
VCC	Operating range	2.7		3.6	2.7		3.6	2.7		3.6	2.7		3.6	V
	See (3) and (2)	2.0		2.7	2.0		2.7	2.0		2.7	2.0		2.7	V
	See (2)	3.6		5.25	3.6		5.25	3.6		5.25	3.6		5.25	V
Quiescent current	Full speed (4)		220	350		220	350		250	350		260	350	µA
	f_{SAMPLE} = 7.5 kHz (5),		20			20			20			20		µA
	f_{SAMPLE} = 7.5 kHz (6)		180			180			180			180		µA
Power down	$\overline{CS}$ = V_{CC}			3			3			3			3	µA
TEMPERATURE RANGE														
Specified performance		-40		85	-40		85	-40		85	-40		85	°C

(4) Full speed: 125 ksps for ADS7829, 200 ksps for ADS7826, and 250 ksps for ADS7827.
(5) f_{DCLOCK} = 1.2 MHz, $\overline{CS}$ = V_{CC} for 145 clock cycles out of every 160 for the ADS7829I and ADS7829IB.
(6) See the Power Dissipation section for more information regarding lower sample rates.

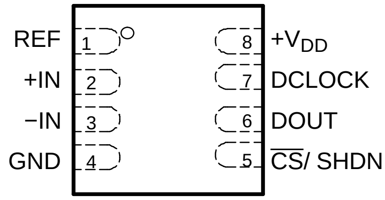
At -40°C to 85°C, V_{CC} = 5 V, V_{ref} = 5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	ADS7829IB			ADS7829			ADS7826I			ADS7827I			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE														
Resolution			12			12			10			8		Bits
No missing codes		12			11			10			8			Bits
Integral linearity error			±0.6			±0.8			±0.15			±0.1	1	LSB (7)
Differential linearity error			±0.5			±0.8			±0.15			±0.1	1	LSB
ANALOG INPUT														
Offset error			±2.6			±2.6			±1.2			±0.7		LSB
Gain error			±1.2			±1.2			±0.2			±0.1		LSB
REFERENCE INPUT														
Voltage range		0.05		V_{CC}	0.05		V_{CC}	0.05		V_{CC}	0.05		V_{CC}	V

(7) LSB means Least Significant Bit . With V_{ref} equal to 5 V, one LSB is 1.22 mV for a 12 bit ADC.

DEVICE INFORMATION

PIN DESCRIPTION
PDSO (SON−8) PACKAGE
(TOP VIEW)



Terminal Functions

PIN	NAME	DESCRIPTION
1	V_{ref}	Reference input
2	+In	Noninverting input
3	-In	Inverting input. Connect to ground or to remote ground sense point.
4	GND	Ground
5	$\overline{CS}$/SHDN	Chip select when LOW, shutdown mode when HIGH
6	DOUT	The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit, the data is valid for the next 12 edges.
7	DCLOCK	Data Clock synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	Power supply

TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{CC} = 2.7 V, V_{ref} = 25 V, (unless otherwise specified)

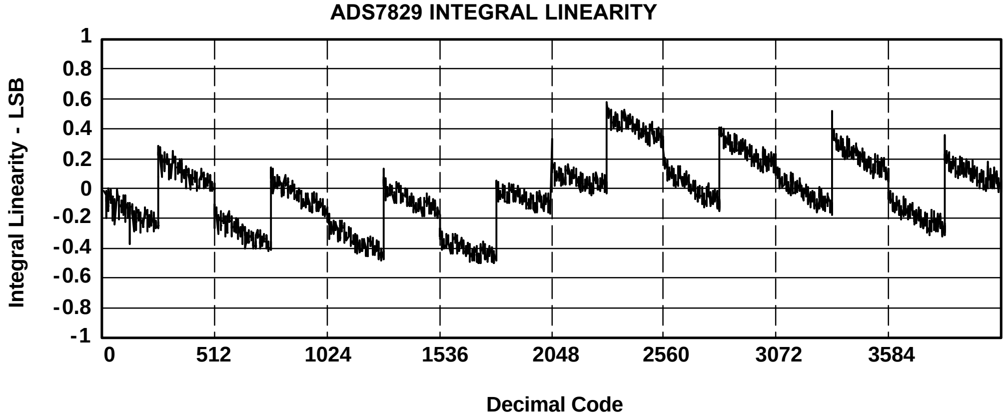


Figure 1

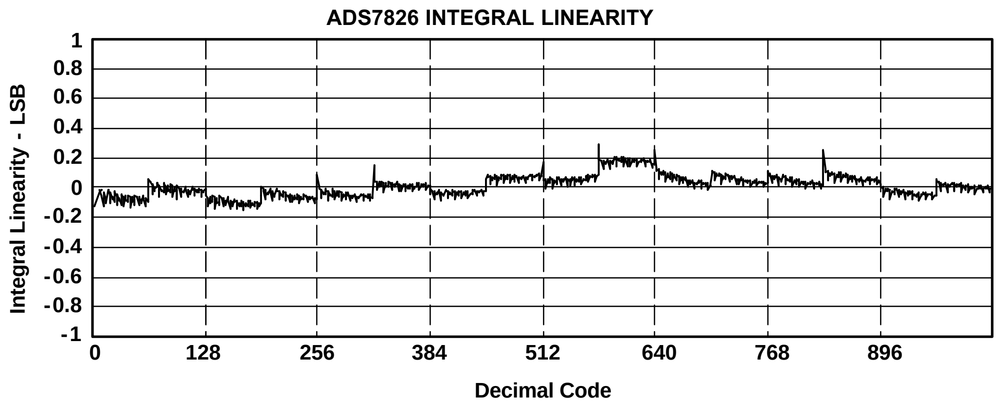


Figure 2

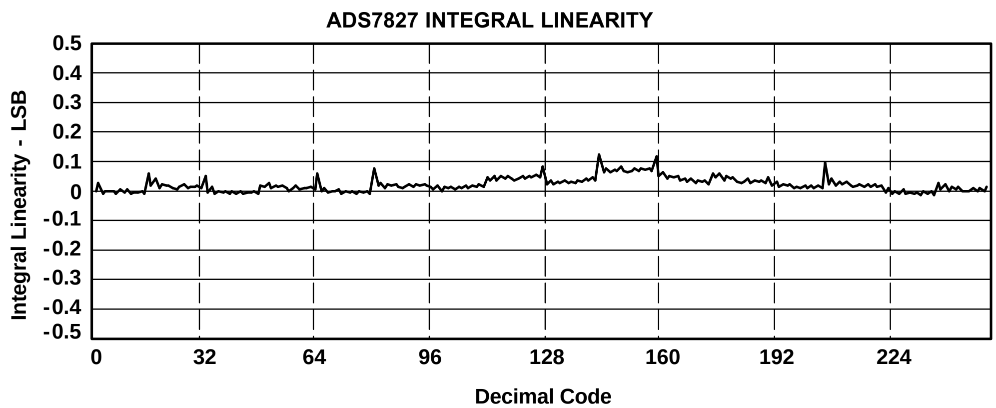


Figure 3

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CC} = 2.7 V, V_{ref} = 25 V, (unless otherwise specified)

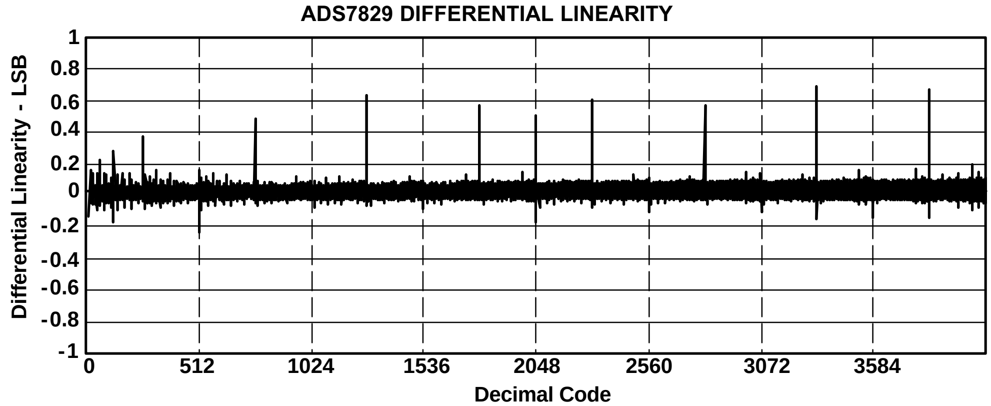


Figure 4

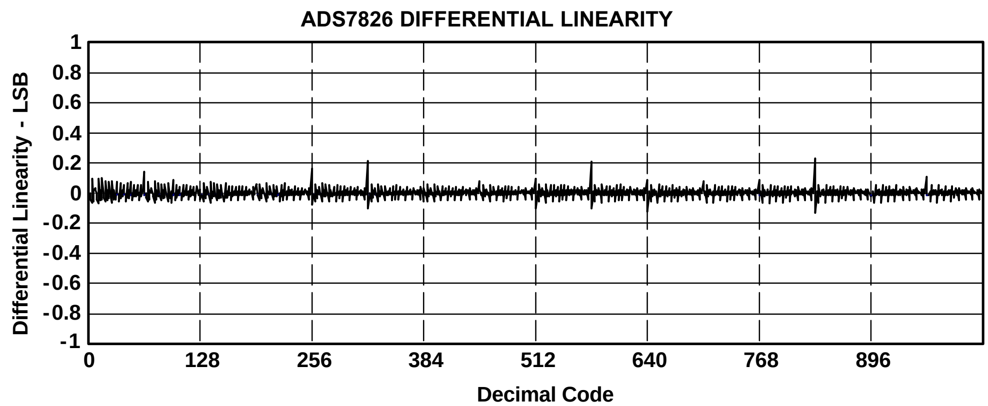


Figure 5

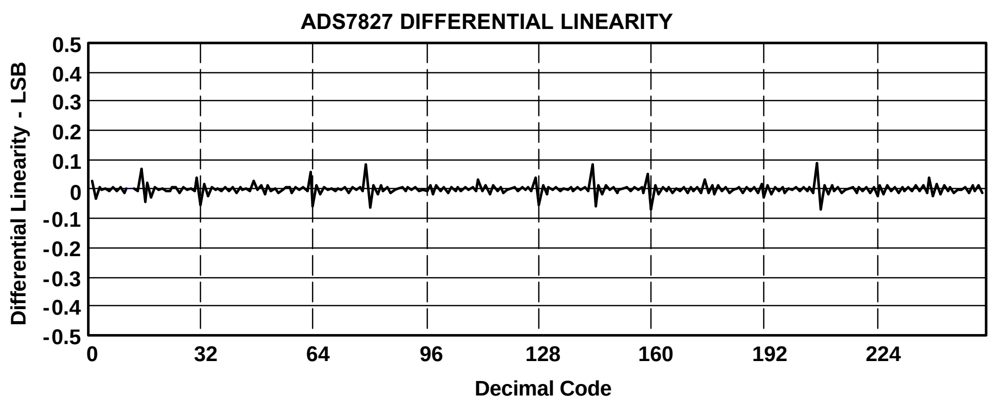


Figure 6

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CC} = 2.7 V, V_{ref} = 25 V, (unless otherwise specified)

CHANGE IN MINIMUM INTEGRAL LINEARITY vs FREE-AIR TEMPERATURE

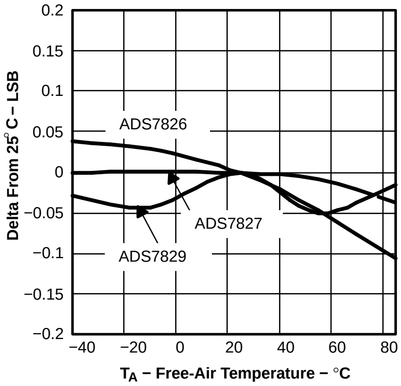


Figure 7.

CHANGE IN MAXIMUM INTEGRAL LINEARITY vs FREE-AIR TEMPERATURE

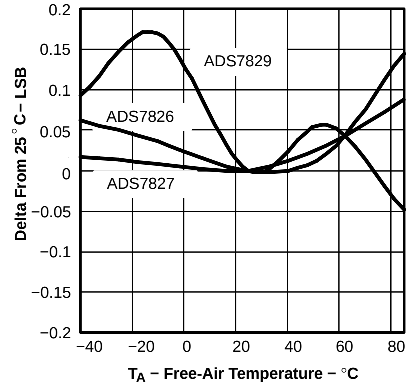


Figure 8.

CHANGE IN MINIMUM DIFFERENTIAL LINEARITY vs FREE-AIR TEMPERATURE

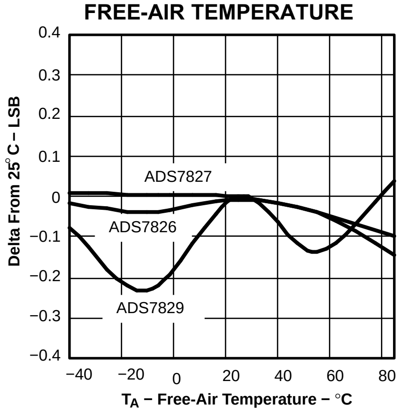


Figure 9.

CHANGE IN MAXIMUM DIFFERENTIAL LINEARITY vs FREE-AIR TEMPERATURE

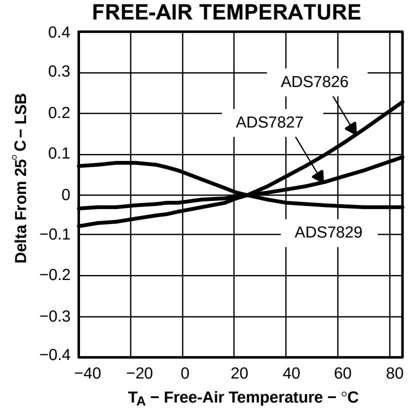


Figure 10.

CHANGE IN OFFSET ERROR vs FREE-AIR TEMPERATURE

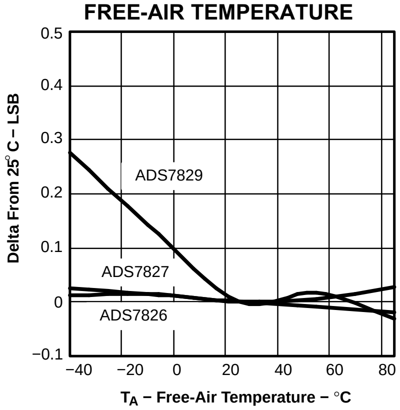


Figure 11.

CHANGE IN GAIN ERROR vs FREE-AIR TEMPERATURE

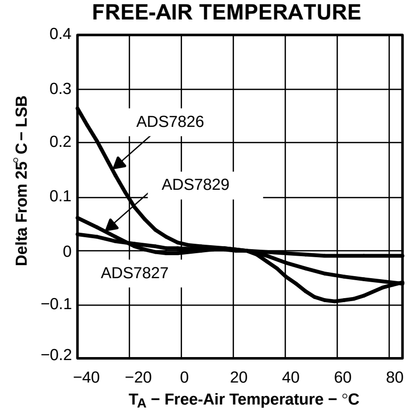


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CC} = 2.7 V, V_{ref} = 25 V, (unless otherwise specified)

CHANGE IN QUIESCENT CURRENT vs FREE-AIR TEMPERATURE

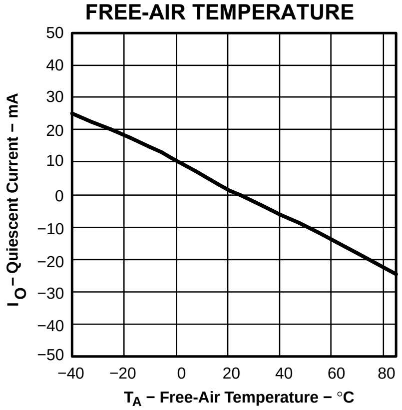


Figure 13.

CHANGE IN MAXIMUM INTEGRAL LINEARITY vs SUPPLY VOLTAGE

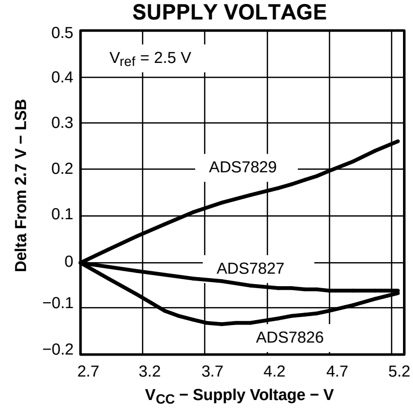


Figure 14.

CHANGE IN MINIMUM INTEGRAL LINEARITY vs SUPPLY VOLTAGE

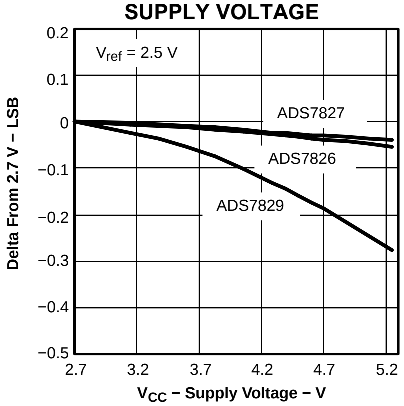


Figure 15.

CHANGE IN MAXIMUM DIFFERENTIAL LINEARITY vs SUPPLY VOLTAGE

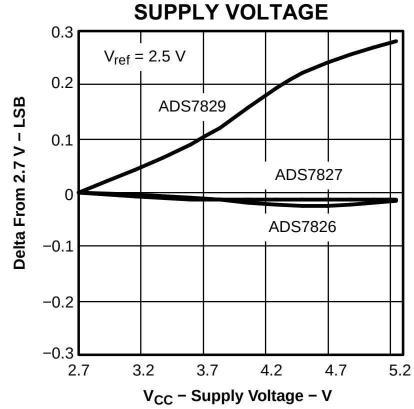


Figure 16.

CHANGE IN MINIMUM INTEGRAL LINEARITY vs SUPPLY VOLTAGE

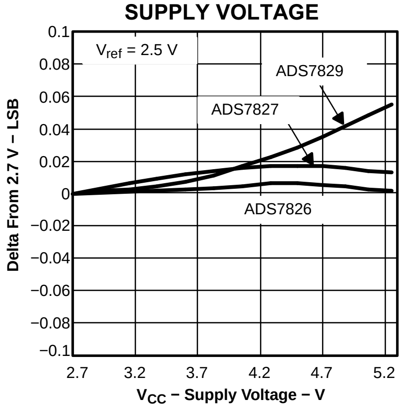


Figure 17.

CHANGE IN OFFSET ERROR vs SUPPLY VOLTAGE

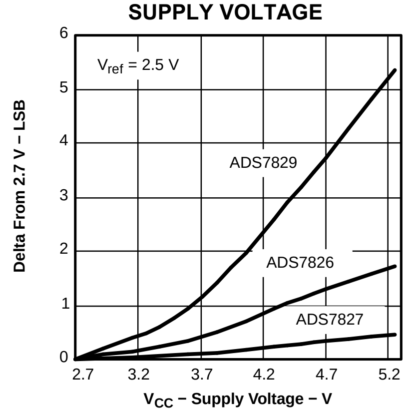


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{CC} = 2.7 V, V_{ref} = 25 V, (unless otherwise specified)

CHANGE IN GAIN vs SUPPLY VOLTAGE

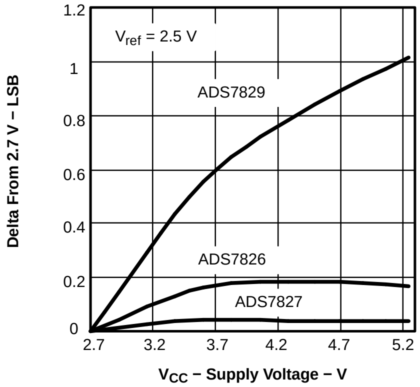


Figure 19.

CHANGE IN QUIESCENT CURRENT vs SUPPLY VOLTAGE

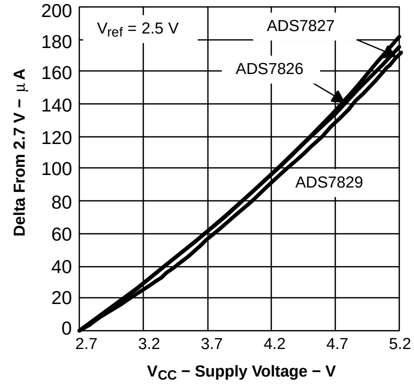


Figure 20.

REFERENCE CURRENT vs SAMPLE RATE

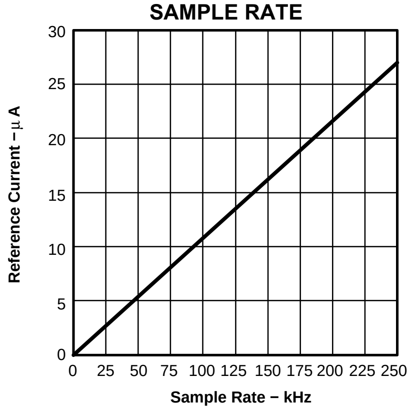


Figure 21.

ADS7829 CHANGE IN OFFSET ERROR vs REFERENCE VOLTAGE

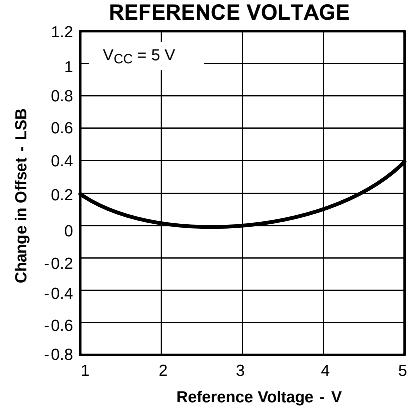


Figure 22.

ADS7829 CHANGE IN GAIN ERROR vs REFERENCE VOLTAGE

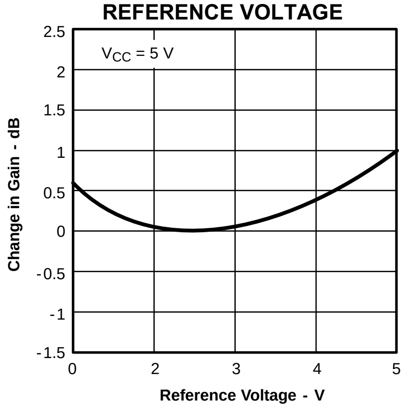


Figure 23.

ADS7829 PEAK-TO-PEAK NOISE vs REFERENCE VOLTAGE

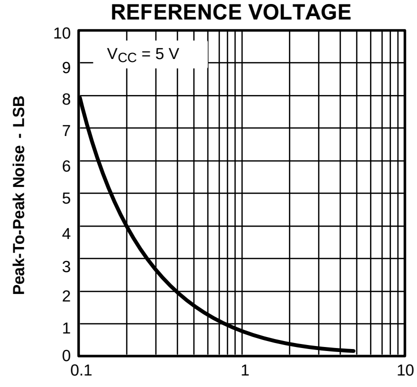


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25°C$, $V_{CC} = 2.7$ V, $V_{ref} = 25$ V, (unless otherwise specified)

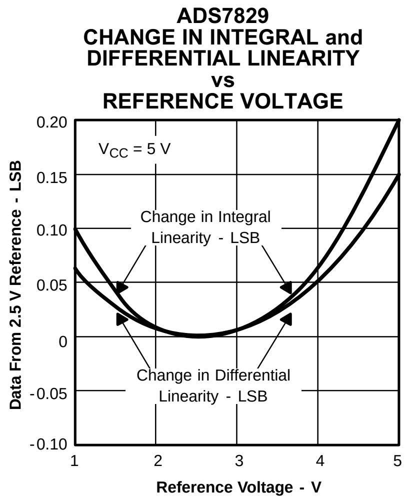


Figure 25.

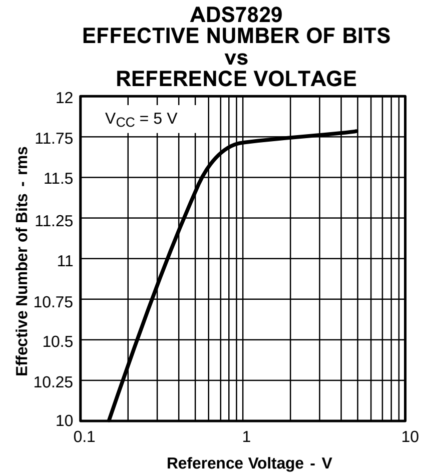


Figure 26.

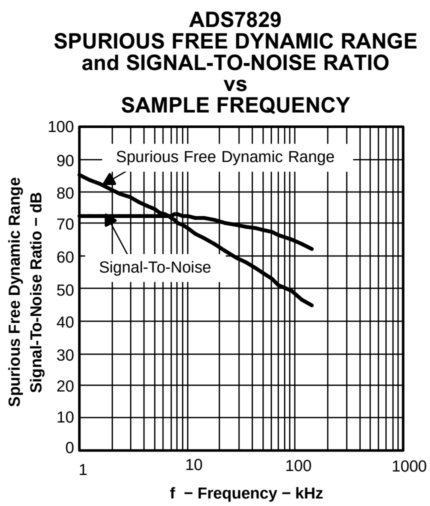


Figure 27.

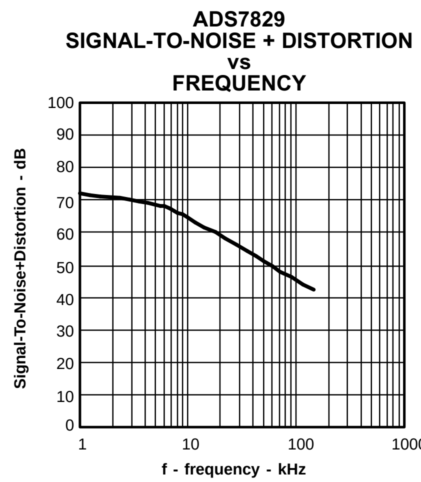


Figure 28.

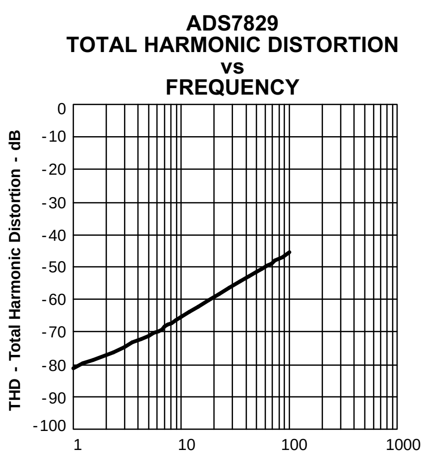


Figure 29.

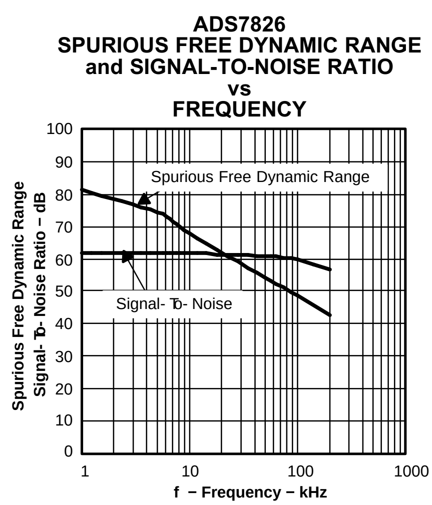


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At $T_A = 25°C$, $V_{CC} = 2.7$ V, $V_{ref} = 25$ V, (unless otherwise specified)

ADS7826
SIGNAL-TO-NOISE + DISTORTION
vs
FREQUENCY

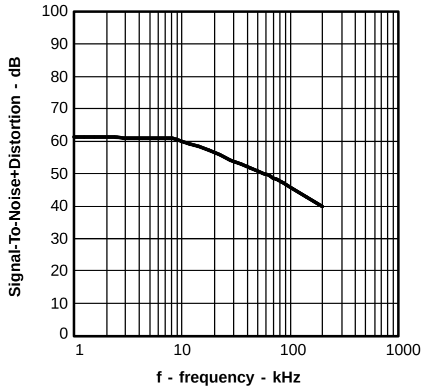


Figure 31.

ADS7826
TOTAL HARMONIC DISTORTION
vs
FREQUENCY

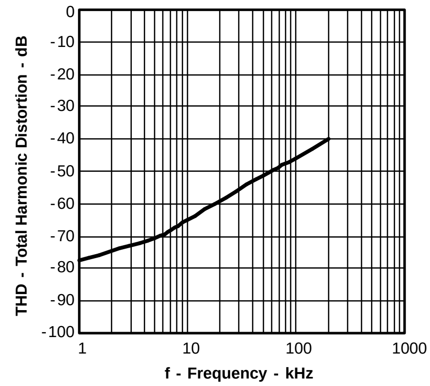


Figure 32.

ADS7827
SPURIOUS FREE DYNAMIC RANGE
and SIGNAL-TO-NOISE RATIO
vs
FREQUENCY

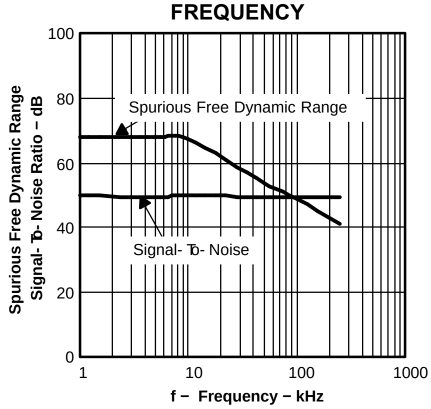


Figure 33.

ADS7827
SIGNAL-TO-NOISE + DISTORTION
vs
FREQUENCY

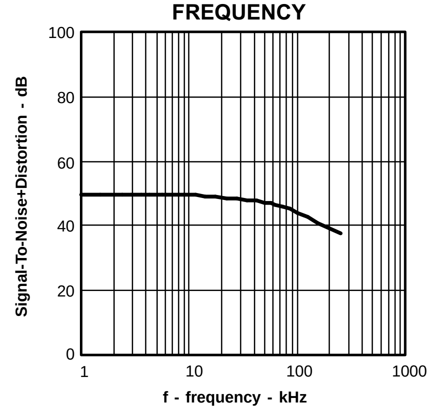


Figure 34.

ADS7827
TOTAL HARMONIC DISTORTION
vs
FREQUENCY

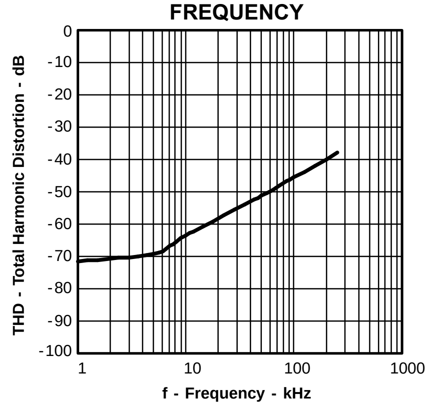


Figure 35.

THEORY OF OPERATION

The ADS7826/27/29 is a family of micropower classic successive approximation register (SAR) analog-to-digital (A/D) converters. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6 µm CMOS process. The architecture and process allow the ADS7826/27/29 family to acquire and convert an analog signal at up to 200K/250K/125K conversions per second respectively while consuming very little power.

The ADS7826/27/29 family requires an external reference, an external clock, and a single power source (V_{CC}). The external reference can be any voltage between 50 mV and V_{CC}. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS7826/27/29 family.

The minimum external clock input to DCLOCK can be as low as 10 kHz. The maximum external clock frequency is 2 MHz for ADS7829, 2.8 MHz for ADS7826 and 3 MHz for ADS7827 respectively. The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 400 ns (V_{CC} = 2.7 V or greater). The minimum DCLOCK frequency is set by the leakage on the capacitors internal to the ADS7826/27/29 family.

The analog input is provided to two input pins: +In and -In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay.

ANALOG INPUT

The +In and -In input pins allow for a differential input signal. Unlike some converters of this type, the -In input is not re-sampled later in the conversion cycle. When the converter goes into the hold mode, the voltage difference between +In and -In is captured on the internal capacitor array.

The range of the -In input is limited to -0.2 V to 1 V. Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the -In input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power down mode. Essentially, the current into the ADS7826/27/29 family charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (25 pF) to a 10/8/12-bit settling level within 1.5 DCLOCK cycles. When the converter goes into the hold mode or while it is in the power down mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the -In input should not drop below GND - 200 mV or exceed GND + 1 V. The +In input should always remain within the range of GND - 200 mV to V_{CC} + 200 mV. Outside of these ranges, the converter's linearity may not meet specifications.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7826/27/29 family operates with a reference in the range of 50 mV to V_{CC}. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 2^N (where N is 12 for ADS7829, 10 for ADS7826, and 8 for ADS7827). This means that any offset or gain error inherent in the A/D converter appears to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter also appears to increase with lower LSB size. With a 2.5 V reference, the internal noise of the converter typically contributes only 0.32 LSB peak-to-peak of potential error to the output code. When the external reference is 50 mV, the potential error contribution from the internal noise is 50 times larger —16 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical performance curves *Effective Number of Bits vs Reference Voltage* and *Peak-to-Peak Noise vs Reference Voltage* (only curves for ADS7829 are shown). Note that the effective number of bits (ENOB) figure is calculated based on the converter's signal-to-(noise + distortion) ratio with a 1 kHz, 0 dB input signal. SINAD is related to ENOB as follows:

SINAD = 6.02 × ENOB + 1.76

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter is more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

DIGITAL INTERFACE

Signal Levels

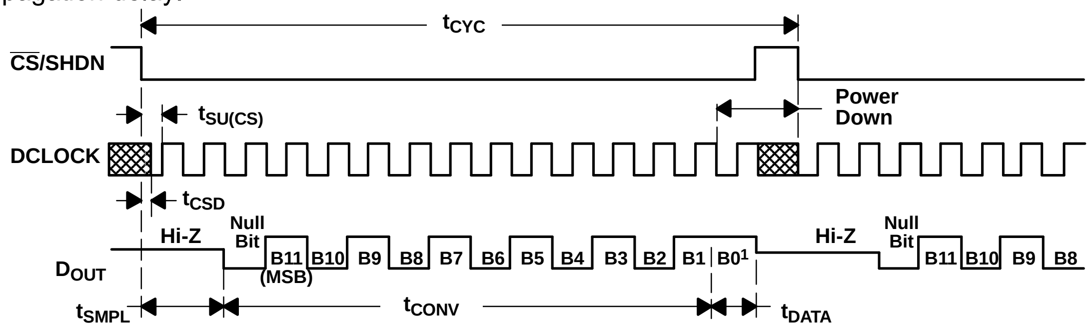
The digital inputs of the ADS7826/27/29 family can accommodate logic levels up to 6 V regardless of the value of V_{CC}. Thus, the ADS7826/27/29 family can be powered at 3 V and still accept inputs from logic powered at 5 V.

The CMOS digital output (D_{OUT}) swings 0 V to V_{CC}. If V_{CC} is 3 V and this output is connected to a 5-V CMOS logic input, then that IC may require more supply current than normal and may have a slightly longer propagation delay.

Serial Interface

The ADS7826/27/29 family communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface. Timings for ADS7829 are shown in Figure 36 and Table 1. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

The timings for ADS7826 and ADS7827 serial interface are shown in Figure 37 and Table 1. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, athe system can use the fallng edge of DCLOCK to capture each bit.



After completing the data transfer, if further clocks are applied with $\overline{CS}$ LOW, the A/D outputs LSB-First data then followed with zeroes indefinitely.

Figure 36. ADS7829 Timing

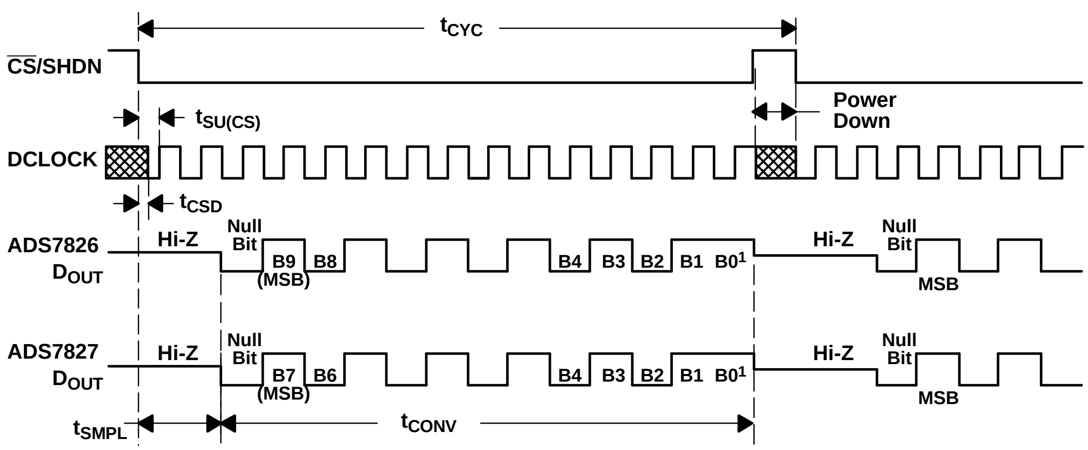


Figure 37. ADS7826 and ADS7827 Timing

Table 1. Timing Specifications (V_{CC} = 2.7 V and Above -40°C to 85°C

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNIT
t_{SAMPLE}	Analog input sample time		1.5		2.0	DCLOCK Cycles
t_{CONV}	Conversion time	ADS7829I or ADS7829IB		12		DCLOCK Cycles
		ADS7826I		11		
		ADS7827I		9		
t_{CYC}	Cycle time	ADS7829I or ADS7829IB	16			DCLOCK Cycles
		ADS7826	14			
		ADS7827	12			
t_{CSD}	$\overline{CS}$ falling to DCLOCK LOW				0	ns
$t_{SU(CS)}$	$\overline{CS}$ falling to DCLOCK rising		30			ns
$t_{h(DO)}$	DCLOCK falling to current D_{OUT} not valid		15			ns
$t_{d(DO)}$	DCLOCK falling to next D_{OUT} valid			130	200	ns
t_{dis}	$\overline{CS}$ rising to D_{OUT} 3-state			40	80	ns
t_{en}	DCLOCK falling to D_{OUT} enabled			75	175	ns
t_f	D_{OUT} fall time			90	200	ns
t_r	D_{OUT} rise time			110	220	ns

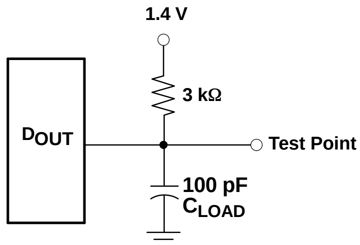
A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 1.5 to 2.0 clock periods of the conversion cycle are used to sample the input signal. After the second falling DCLOCK edge, D_{OUT} is enabled and outputs a LOW value for one clock period. For the next N (N is 12 for ADS7829, 10 for ADS7826, and 8 for ADS7827) DCLOCK periods, D_{OUT} outputs the conversion result, most significant bit first. After the least significant bit has been sent, D_{OUT} goes to 3-state after the rising edge of $\overline{CS}$. A new conversion is initiated only when $\overline{CS}$ has been taken high and returned low again.

DATA FORMAT

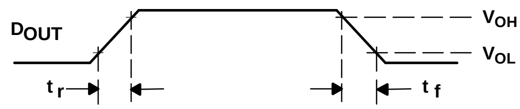
The output data from the ADS7826/27/29 family is in straight binary format. ADS7829 out is shown in Table 2, as an example. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise. For ADS7826 the last two LSB's are don't cares, while for ADS7827 the last four LSB's are don't cares.

Table 2. Ideal Input Voltages and Output Codes (ADS7829 Shown as an Example)

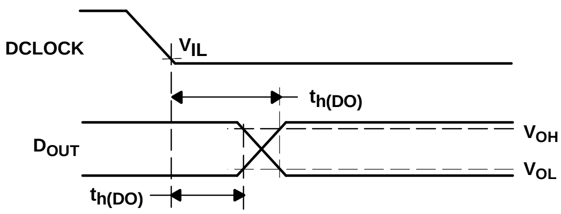
DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
FULL SCALE RANGE	V_{ref}		
LEAST SIGNIFICANT BIT (LSB)	$V_{ref}/4096$	BINARY CODE	HEX CODE
Full scale	V_{ref} - 1 LSB	1111 1111 1111	FFF
Midscale	$V_{ref}/2$	1000 0000 0000	800
Midscale - 1 LSB	$V_{ref}/2$ - 1 LSB	0111 1111 1111	7FF
Zero	0 V	0000 0000 0000	000



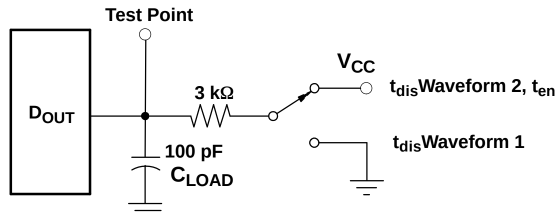
Load Circuit for t_{dDO}, t_r, and t_f



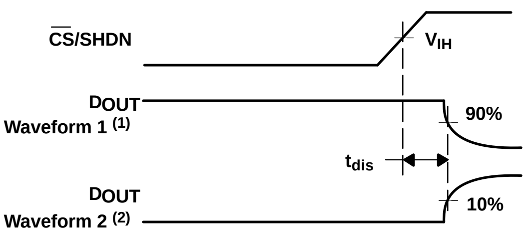
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



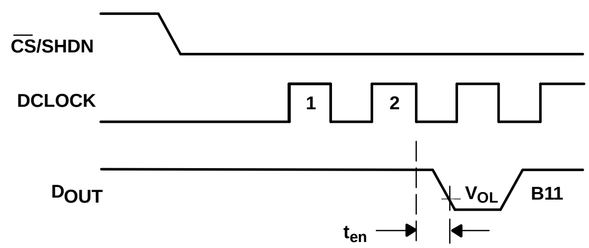
Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



Voltage Waveforms for t_{en}

(1) Waveform 1 is for an output with internal conditions such that the output is HIGH unless disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is LOW unless disabled by the output control.

Figure 38. Timing Diagrams and Test Circuits for the Parameters in Table 1.

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allows the ADS7826/27/29 family to convert at the full sample rate while requiring very little power. But, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS7826/27/29 family scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that satisfies the requirements of the system.

In addition, the ADS7826/27/29 family is in power down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH. Ideally, each conversion occurs as quickly as possible, preferably, at DCLOCK rate.

This way, the converter spends the longest possible time in the power down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components) but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power-down mode is entered.

The current consumption of the ADS7826/27/29 family versus sample rate. For this graph, the converter is clocked at maximum DCLOCK rate regardless of the sample rate —$\overline{CS}$ is HIGH for the remaining sample period. Figure 4 also shows current consumption versus sample rate. However, in this case, the minimum DCLOCK cylce time is used—$\overline{CS}$ is HIGH for one DCLOCK cycle.

There is an important distinction between the power down mode that is entered after a conversion is complete and the full power-down mode which is enabled when $\overline{CS}$ is HIGH. While both shutdown the analog section, the digital section is completely shutdown only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption is not as low as when $\overline{CS}$ is HIGH.

Power dissipation can also be reduced by lowering the power supply voltage and the reference voltage. The ADS7826/27/29 family operates over a V_{CC} range of 2.0 V to 5.25 V. However, at voltages below 2.7 V, the converter does not run at the maximum sample rate. See the typical performance curves for more information regarding power supply voltage and maximum sample rate.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7826/27/29 family circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high. At a 125-kHz to 250-kHz conversion rate, the ADS7826/27/29 family makes a bit decision every 800 ns to 400 ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled, for example the ADS7829, to a 12-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n *windows* in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter’s DCLOCK signal—as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS7826/27/29 family should be clean and well bypassed. A 0.1-μF ceramic bypass capacitor should be placed as close to the ADS7826/27/29 family package as possible. In addition, a 1-μ to 10-μF capacitor and a 5-Ω or 10-Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1-μF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op-amp, be careful that the op-amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS7826/27/29 family draws very little current from the reference on average, there are still instantaneous current demands placed on the external reference circuitry.

Also, keep in mind that the ADS7826/27/29 family offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply appears directly in the digital results. While high frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50 Hz or 60 Hz), can be difficult to remove.

The GND pin on the ADS7826/27/29 family must be placed on a clean ground point. In many cases, this is the *analog* ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power supply connection point. The ideal layout includes an analog ground plane for the converter and associated analog circuitry.

APPLICATION CIRCUITS

Figure 39 and Figure 40 show some typical application circuits the ADS7826/27/29 family. Figure 39 uses an ADS7826/27/29 and a multiplexer to provide for a flexible data acquisition circuit. A resistor string provides for various voltages at the multiplexer input. The selected voltage is buffered and driven into V_{ref}. As shown in Figure 39, the input range of the ADS7826/27/29 family programmable to 100 mV, 200 mV, 300 mV, or 400 mV. The 100-mV range would be useful for sensors such as thermocouple shown.

Figure 39 shows a basic data acquisition system. The ADS7826/27/29 family input range is 0 V to V_{CC}, as the reference input is connected directly to the power supply. The 5-Ω resistor and 1-μF to 10-μF capacitor filters the microcontroller *noise* on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of the noise.

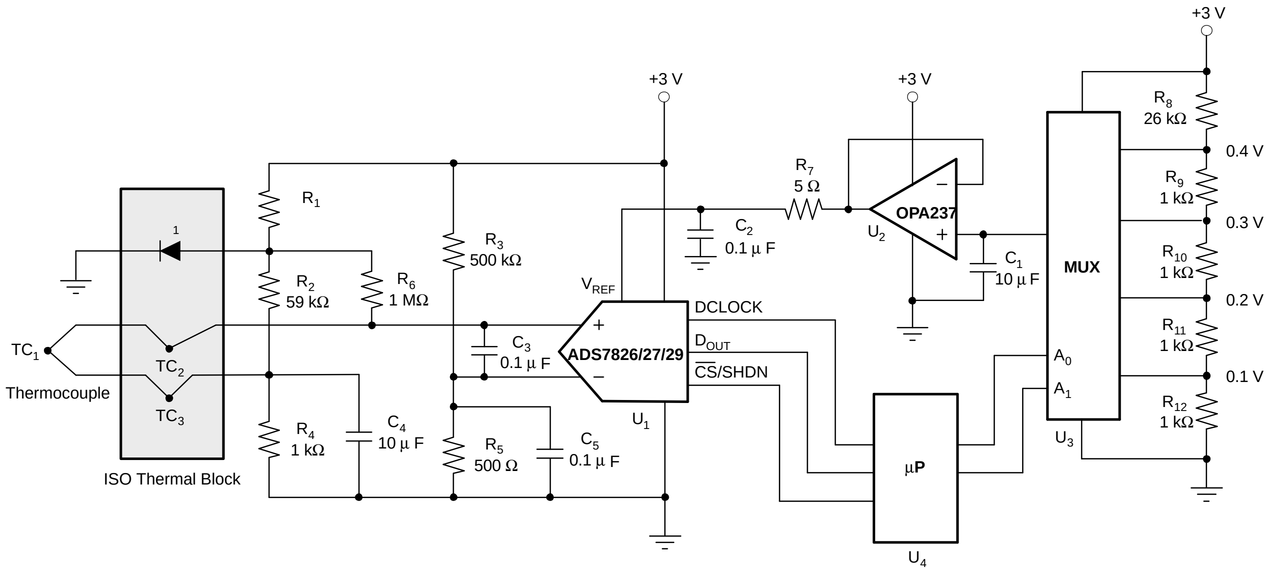


Figure 39. Thermocouple Application Using a MUX to Scale the Input Range of the ADS7826/27/29 family

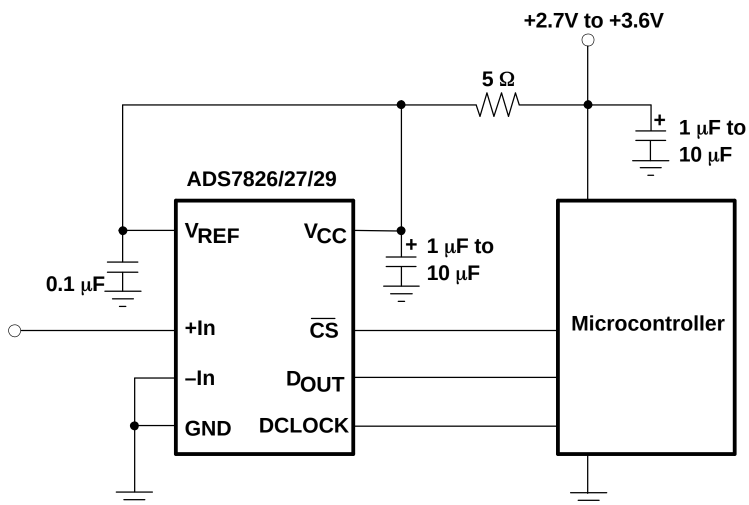


Figure 40. Basic Data Acquisition System

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7826IDRBR	ACTIVE	SON	DRB	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F26	Samples
ADS7826IDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F26	Samples
ADS7827IDRBR	ACTIVE	SON	DRB	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F27	Samples
ADS7827IDRBRG4	ACTIVE	SON	DRB	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F27	Samples
ADS7827IDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F27	Samples
ADS7827IDRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	F27	Samples
ADS7829IBDRBR	ACTIVE	SON	DRB	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	F29	Samples
ADS7829IBDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	F29	Samples
ADS7829IBDRBTG4	ACTIVE	SON	DRB	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	F29	Samples
ADS7829IDRBR	ACTIVE	SON	DRB	8	2500	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	F29	Samples
ADS7829IDRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	F29	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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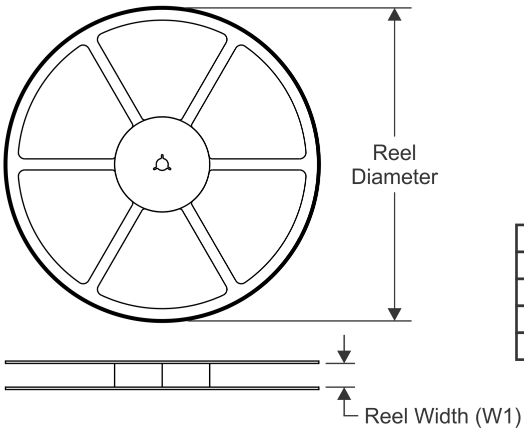
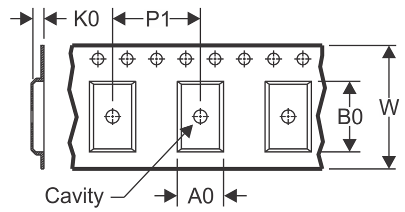
TAPE AND REEL INFORMATION

REEL DIMENSIONS

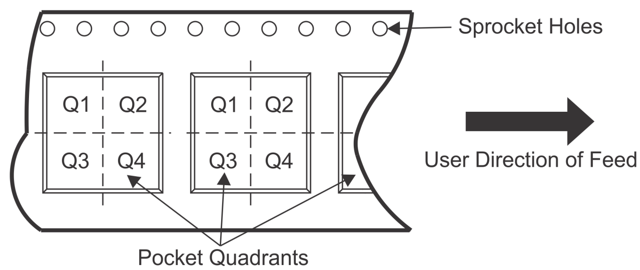


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

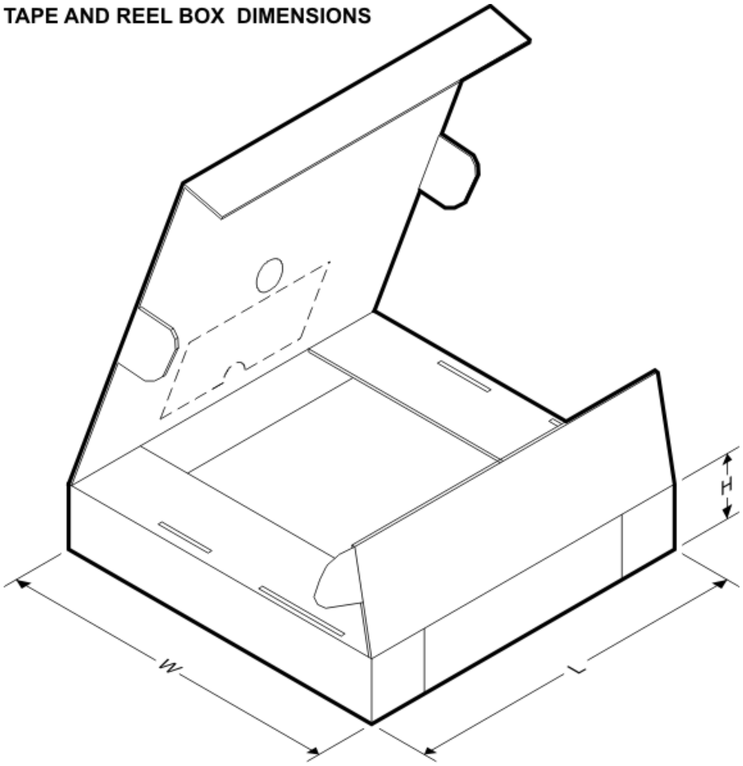
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7826IDRBR	SON	DRB	8	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7826IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7827IDRBR	SON	DRB	8	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7827IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7829IBDRBR	SON	DRB	8	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7829IBDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7829IDRBR	SON	DRB	8	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS7829IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

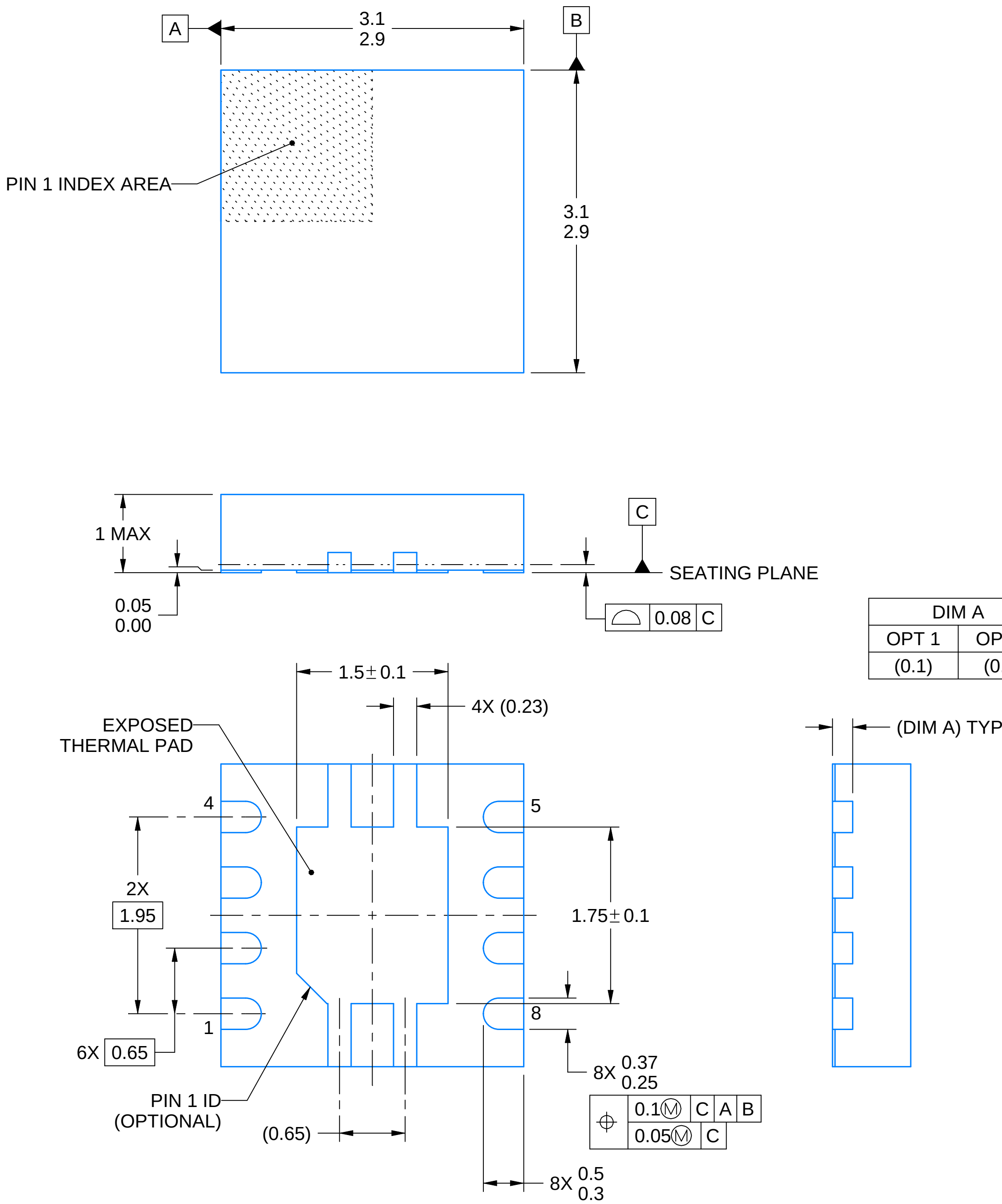
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7826IDRBR	SON	DRB	8	2500	367.0	367.0	35.0
ADS7826IDRBT	SON	DRB	8	250	210.0	185.0	35.0
ADS7827IDRBR	SON	DRB	8	2500	367.0	367.0	35.0
ADS7827IDRBT	SON	DRB	8	250	210.0	185.0	35.0
ADS7829IBDRBR	SON	DRB	8	2500	367.0	367.0	35.0
ADS7829IBDRBT	SON	DRB	8	250	210.0	185.0	35.0
ADS7829IDRBR	SON	DRB	8	2500	367.0	367.0	35.0
ADS7829IDRBT	SON	DRB	8	250	210.0	185.0	35.0

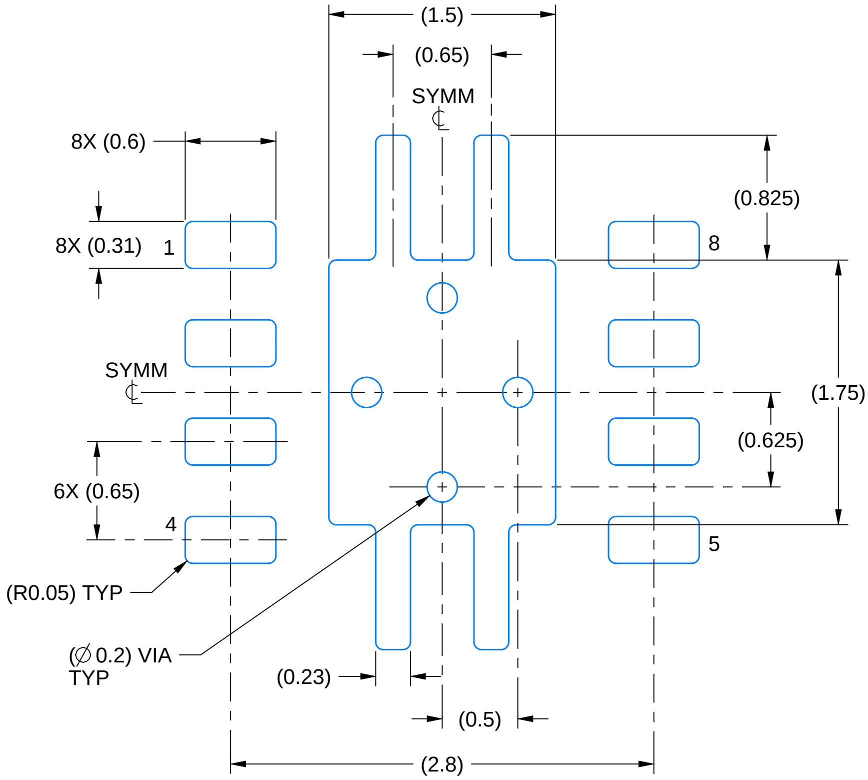
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



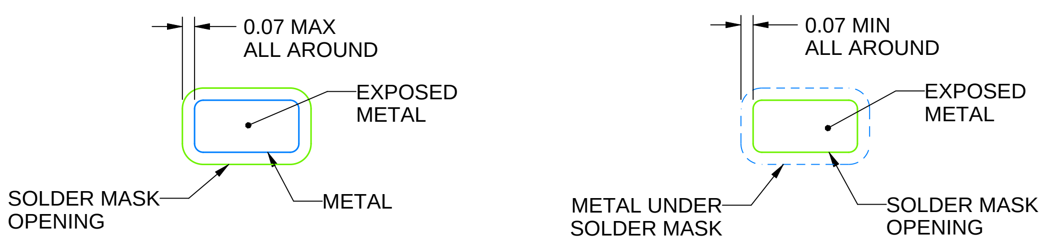
DIM A	
OPT 1	OPT 2
(0.1)	(0.2)

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

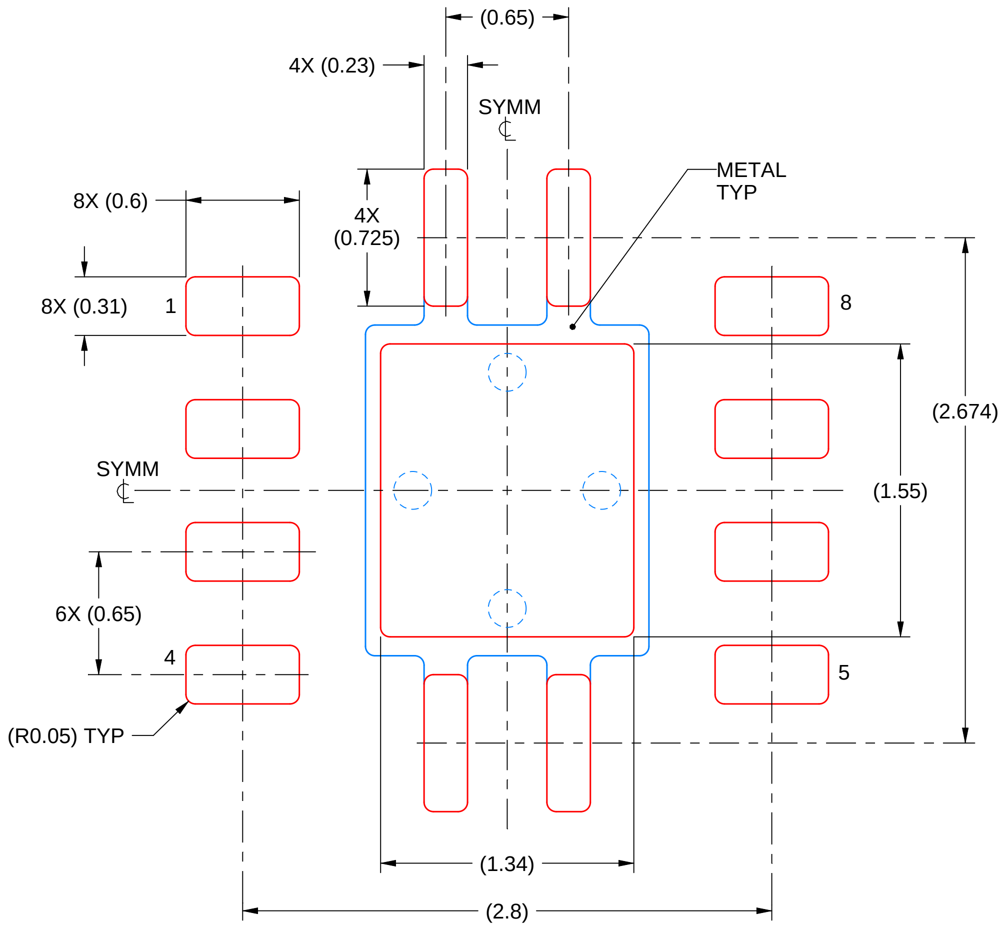
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265