AMC6821-Q1 Intelligent Temperature Monitor and PWM Fan Controller

1 Features

- Qualified for automotive applications:
  - Junction temperature: –40°C to +150°C, T_J
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Remote temperature sensor: ±3°C accuracy, 0.250°C resolution
- Local temperature sensor: ±3°C accuracy, 0.250°C resolution
- PWM controller
- PWM frequency: 10 Hz to 40 kHz
- Duty cycle: 0% to 100%, 8 bits
- Automatic fan speed control loops
- SMBus interface
- Power: 2.7 V to 5.5 V
- Package (green): SSOP-16 (4mm × 5mm)
- RoHS-compliant
- Latch-up exceeds 100 mA per JESD78B - class I

2 Applications

- ADAS domain controller
- Drive assist ECU
- Digital cockpit processing unit
- Surround view system ECU

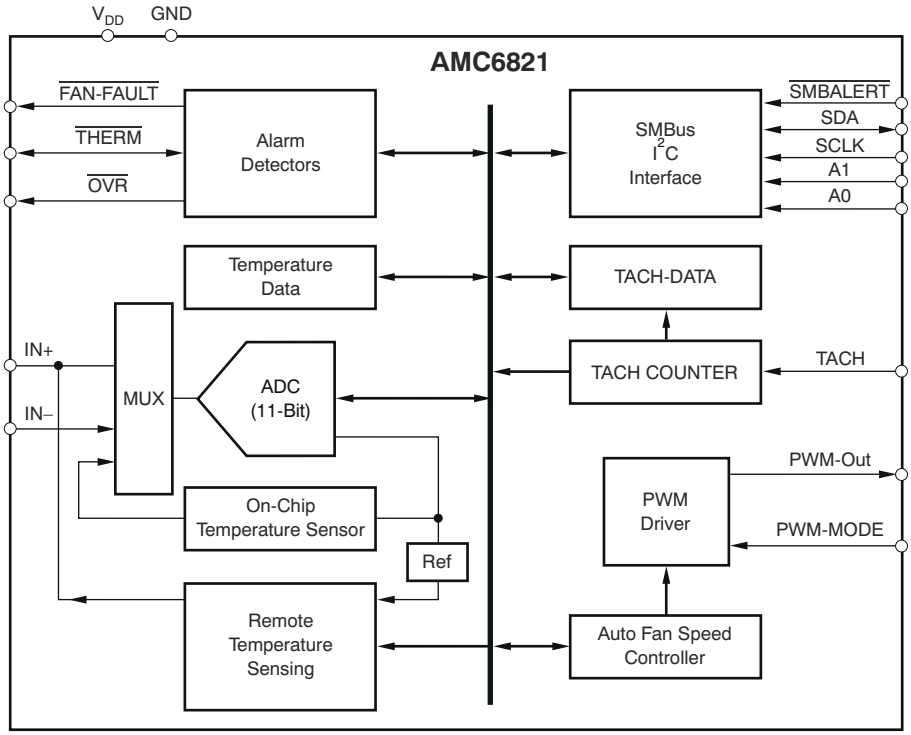
3 Description

The AMC6821-Q1 is an intelligent temperature monitor and pulse-width modulation (PWM) fan controller. It is designed for noise-sensitive or power-sensitive applications that require active system cooling. Using either a low-frequency or a high-frequency PWM signal, this device can simultaneously drive a fan, monitor remote sensor diode temperatures, and measure and control the fan speed so that it operates with minimal acoustic noise at the lowest possible speed.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC6821-Q1	SSOP (16)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2009) to Revision A (January 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *Applications* section, the *ESD Ratings* table, *Thermal Information* table, and the *Application and Implementation* section	1
• Added Functional Safety information to the *Features* section	1
• Deleted *Ordering Information* table. Content moved to the *Mechanical, Packaging, and Orderable Information* section	1
• Added the I/O column to the *Pin Functions* table	3

5 Description (continued)

The AMC6821-Q1 has three fan control modes: Auto Temperature-Fan mode, Software-RPM mode, and Software-DCY mode. Each mode controls the fan speed by changing the duty cycle of a PWM output. Auto Temperature-Fan mode is an intelligent, closed-loop control that optimizes fan speed according to user-defined parameters. This mode allows the AMC6821-Q1 to run as a stand-alone device without CPU intervention; the fan can continue to be controlled (based on temperature measurements) even if the CPU or system locks up. Software-RPM mode is a second closed-loop control. In this mode, the AMC6821-Q1 adjusts the PWM output to maintain a consistent fan speed at a user-specified target value; that is, the device functions as a fan speed regulator. Software-RPM mode can also be used to allow the AMC6821-Q1 to operate as a stand-alone device. The third mode, Software-DCY, is open-loop. In Software-DCY mode, the PWM duty cycle is set directly by the value written to the device.

The AMC6821-Q1 has a programmable $\overline{\text{SMBALERT}}$ output to indicate error conditions and a dedicated $\overline{\text{FAN-FAULT}}$ output to indicate fan failure. The $\overline{\text{THERM}}$ pin is a fail-safe output for over-temperature conditions that can be used to throttle a CPU clock. Additionally, the $\overline{\text{OVR}}$ pin indicates the over-temperature limit as well. All of the alarm thresholds are set through the device registers. The AMC6821-Q1 is available in a SSOP-16 package.

6 Pin Configuration and Functions

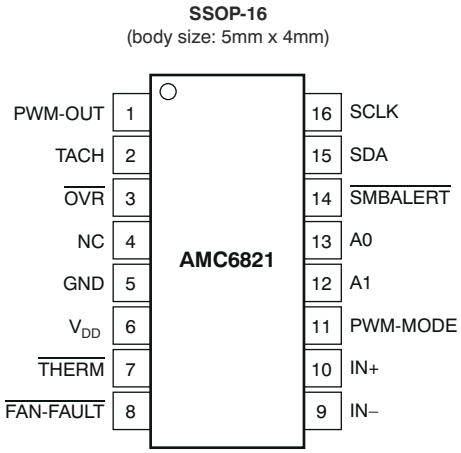


Figure 6-1. DBQ Package 16-Pin SSOP Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
PWM-OUT	1	O	Digital output, open-drain. PWM output to control fan speed.
TACH	2	I	Digital input. Fan tachometer input to measure the fan speed.
$\overline{\text{OVR}}$	3	O	Digital output, open-drain, active low. Goes low when temperature reaches the critical shutdown threshold or remote temperature sensor failed. (See the *Interrupt* section for details.)
NC	4	-	Not connected. Reserved for manufacturer's testing.
GND	5	_	System ground
V_{DD}	6	I	Power supply, 3 V to 5 V
$\overline{\text{THERM}}$	7	I/O	Digital input/output (open-drain). As an output, an active low output indicates the temperature over the THERM temperature limit. As an input, the pin provides an external fan control. When the pin is pulled low by external signal, the THERM-IN bit is set, and the fan is set to full-speed.
$\overline{\text{FAN-FAULT}}$	8	O	Digital open-drain output. Goes low when a fan failure is detected.
IN–	9	I	Negative analog differential input. Connected to cathode of external temperature-sensing diode.
IN+	10	I	Positive analog differential input. Connected to anode of external temperature-sensing diode Pentium-IV™ substrate transistor or general-purpose 2N3904 type transistor.
PWM-MODE	11	I	PWM mode selection. When tied low (GND), the high PWM frequency range (1 kHz to 40 kHz) is selected. When tied to V_{DD} or floated, the low PWM frequency range (10 Hz to 94 Hz) is selected. Checked only on power-up or reset.
A1	12	I	Device slave address selection pin (see the *SMB Interface* section for details). Checked only on power-up or reset.
A0	13	I	Device slave address selection pin (see the *SMB Interface* section for details). Checked only on power-up or reset.
$\overline{\text{SMBALERT}}$	14	O	Digital output, open-drain, $\overline{\text{SMBALERT}}$, active low. Requires a pullup resistor (2.2 kΩ typical).
SDA	15	I/O	Bidirectional digital I/O pin, SMBus data, open-drain. Requires a pullup resistor (2.2 kΩ typical).
SCLK	16	I	Digital input, SMBus clock. Requires a pullup resistor (2.2 kΩ typical).

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{DD} to GND	–0.3	6.5	V
Digital input voltage to GND	–0.3	6.5	V
Input current		10	mA
Select pins A0, A1, PWM-MODE to GND	–0.3	V_{DD} + 0.3	V
Analog input voltage to GND	–0.3	V_{DD} + 0.3	V
Operating temperature	–40	125	°C
Junction temperature (T_J Max)		150	°C
Storage temperature	–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating V_{DD}	2.7	5	5.5	V
Specified V_{DD}	3		5	V
Operating temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		AMC6821-Q1 DBQ (SSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_A = –40°C to 100°C and V_{DD} = 3 V or 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT						
	Local sensor accuracy	T_A = 0°C to 90°C		±0.5	±3	°C
		T_A = –25°C to 100°C		±1	±4	°C
	Remote sensor accuracy(1)	T_R = 50°C to 100°C		±0.5	±3	°C
		T_R = –40°C to 125°C		±1	±4	°C
	Sensor resolution	Both channels		0.125		°C
	Conversion time	Two channels		62.5		ms
PWM CONTROLLER						
	PWM frequency range (programmable)(2)		10		40k	Hz
	PWM frequency accuracy	T_A = 25°C to 100°C	–6%		7%	
	Duty cycle(2)	Programmable	0%		100%	
	Duty cycle resolution	8-bit		0.39		%/bit
FAN RPM-TO-DIGITAL CONVERTER						
	Accuracy	T_A = 25°C to 100°C	–6%		7%	
	Full-scale count(2)				65535	
	Nominal input RPM(2)		100		23000	RPM
	Internal clock frequency for RPM measurement			100		kHz
DIGITAL INPUT/OUTPUT						
V_{OL}	Open-drain output low voltage	Sink current 6 mA, V_{DD} = 3 V	0		0.4	V
I_{OH}	Open-drain high-level output leakage current			0.1	1	µA
V_{IH}	Input high voltage		2.1			V
V_{IL}	Input low voltage				0.8	V
I_{IH}	Input high current		–1			µA
I_{IL}	Input low current				1	µA
	Input capacitance			5		pF
POWER SUPPLY						
	Current	V_{DD} = 5		1.1	2	mA
	Power dissipation			5		mW

(1) The remote temperature sensor is optimized for the Pentium M™ thermal diode with diode ideality n = 1.0022 and T_A = 0°C to 100°C.
(2) Not production tested. Specified by design.

7.6 Timing Requirements

At V_{DD} = 3 V or +5 V, and T_A = –40°C to +125°C, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	Clock frequency			100	kHz
t_{BUF}	Bus free time	4.7			µs
$t_{SU:STA}$	Start setup time	4.7			µs
$t_{HD:STA}$	Start hold time	4			µs
$t_{SU:STO}$	Stop condition setup time	4			µs
t_{LOW}	SCLK low time	4.7			µs
t_{HIGH}	SCLK high time	4			µs
t_R	SCLK, SDA rise time			1000	ns

At V_{DD} = 3 V or +5 V, and T_A = –40°C to +125°C, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
t_F	SCLK, SDA fall time			300	ns
$t_{SU:DAT}$	Data setup time	350			ns
$t_{HD:DAT}$	Data hold time	350			ns
t_{POR}	Time from software reset command or power-on to normal operation. During this period, I2C™ communication is not recognized.			1.5	ms

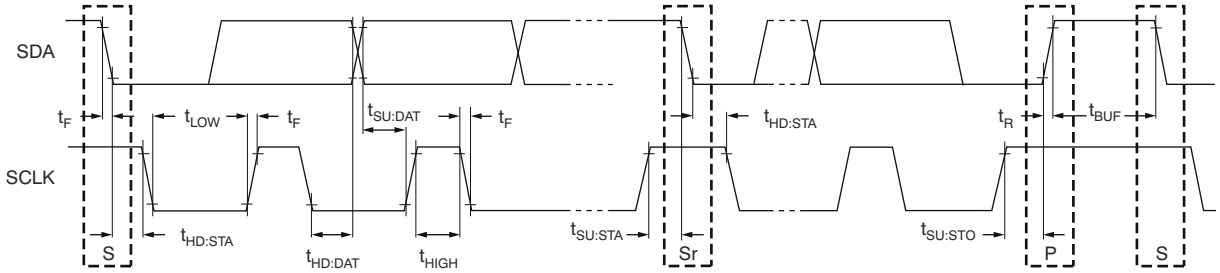


Figure 7-1. Timing Specification

7.7 Typical Characteristics

T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

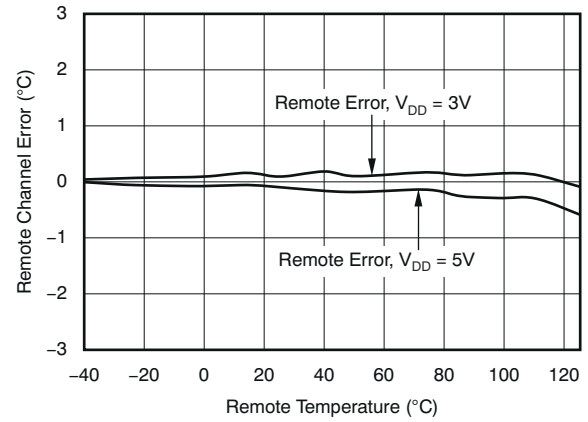


Figure 7-2. Remote Channel Error vs Remote Temperature

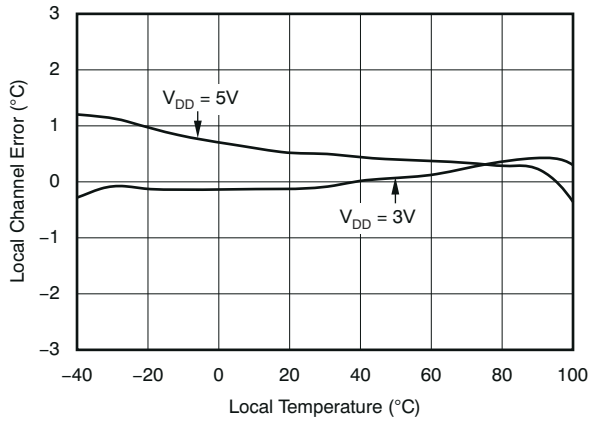


Figure 7-3. Local Channel Error From Calibrated Bath

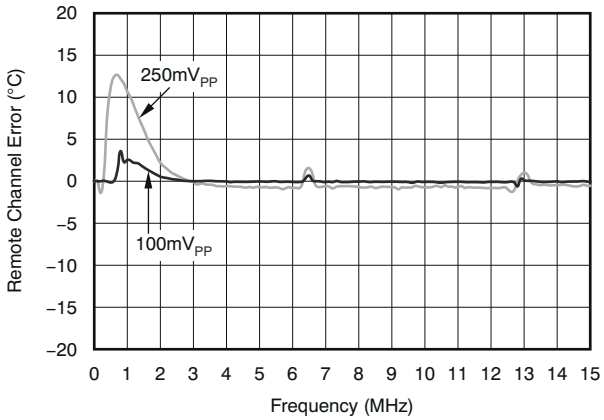


Figure 7-4. Temperature Error vs Power-Supply Noise Frequency

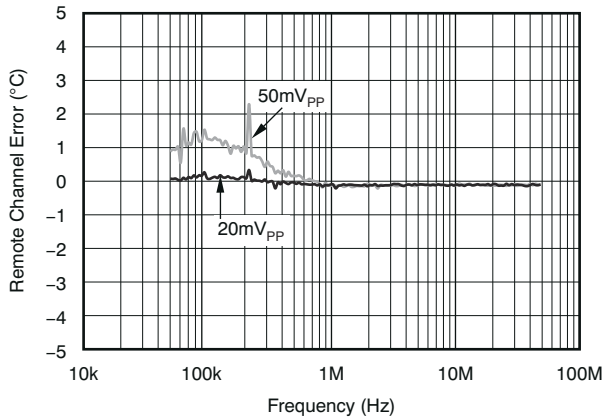


Figure 7-5. Temperature Error vs Common-Mode Noise Frequency

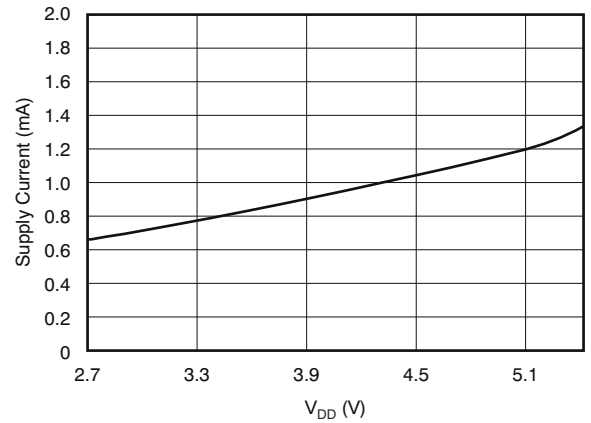


Figure 7-6. Supply Current vs V_{DD}

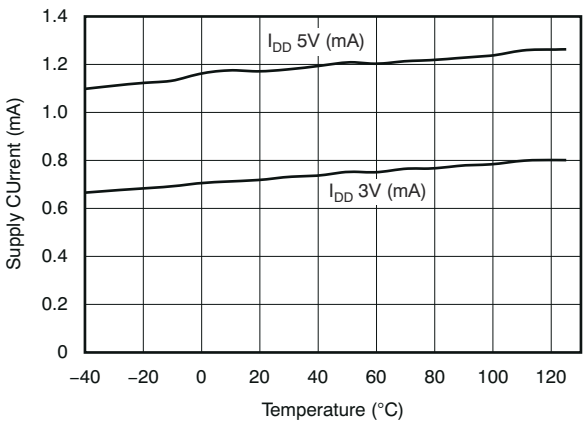


Figure 7-7. Supply Current vs Temperature

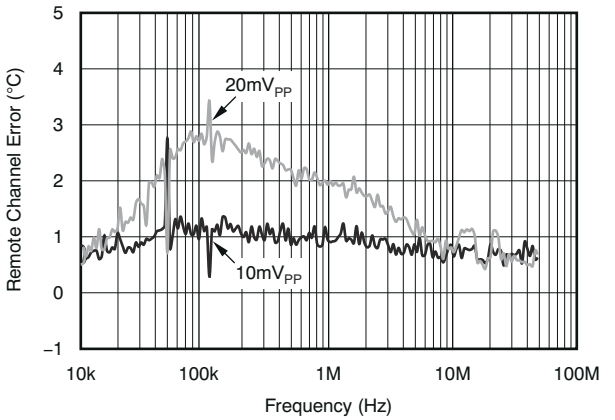


Figure 7-8. Temperature Error vs Differential Mode Noise Frequency

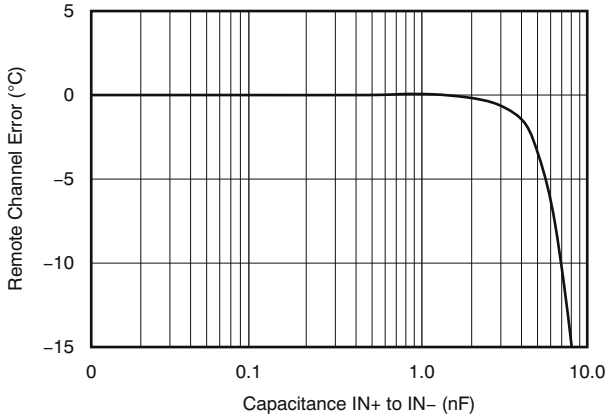


Figure 7-9. Temperature Error vs Capacitance Between In+ and In–

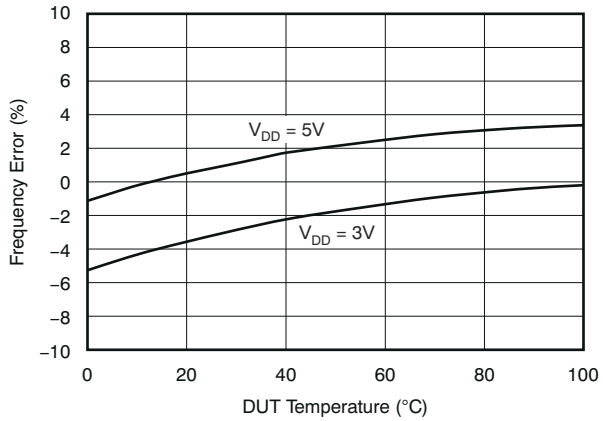
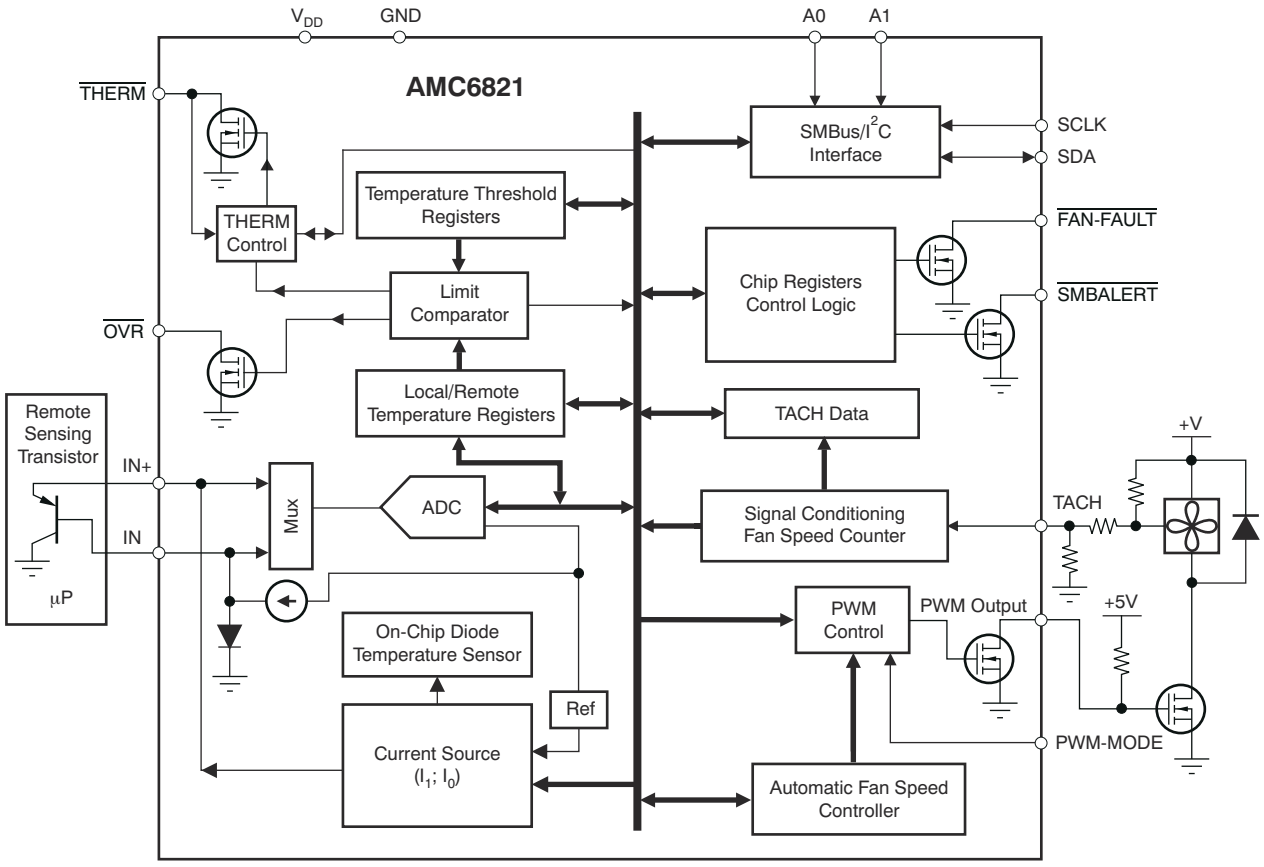


Figure 7-10. PWM Frequency Error vs Temperature

8 Detailed Description

8.1 Functional Block Diagram



8.2 Feature Description

8.2.1 ADC Converter

Figure 8-1 shows the 11-bit, on-chip analog-to-digital converter (ADC) of the AMC6821-Q1. This ADC converts the analog input into digital format. The analog input is passed through front-end signal conditioning circuitry to remove the noise. The resulting signal is then converted by the ADC. To further reduce the effects of noise, digital filtering is performed by averaging the results of 32 measurement cycles. After digital filtering, the newest result is stored in the temperature data register (low byte and high byte) in two's complement format. The ADC stops when the START bit of Configuration Register 1 is cleared ('0') and runs when START = 1.

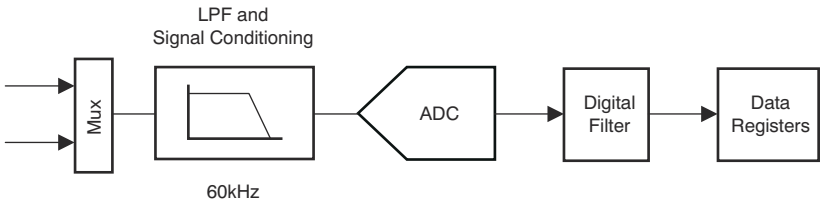


Figure 8-1. On-Chip Analog-to-Digital Converter

8.2.2 Temperature Sensor

The AMC6821-Q1 has an integrated temperature sensor (shown in Figure 8-2) to measure the ambient temperature, and one remote diode sensor (such as a Pentium thermal diode) input to measure external (CPU) temperature. The measurement relies on the characteristics of a semiconductor junction operation at a fixed current level. The forward voltage of the diode (V_{BE}) depends on the current through it and the ambient

temperature. The change in V_{BE} when the diode is operated at two different currents, I_1 and I_2, is shown in Equation 1:

$$\Delta V_{BE} = \frac{KT}{q} \times \ln(N) \quad (1)$$

where

- k is Boltzmann's constant,
- q is the charge of the carrier,
- T is the absolute temperature in degrees Kelvin, and
- N is the ratio of the two currents.

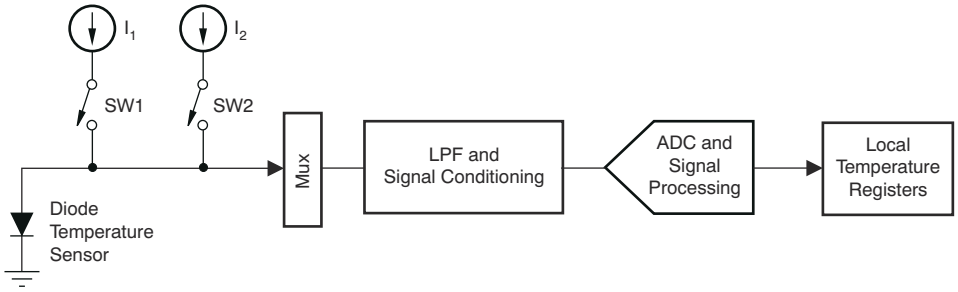


Figure 8-2. Integrated Local Temperature Sensor

The remote sensing transistor can be a substrate transistor built within the microprocessor (as in a Pentium-IV), or a discrete small-signal type transistor. This architecture is shown in Figure 8-3. The internal bias diode biases the IN– terminal above ground to prevent the ground noise from interfering with the measurement. An external capacitor (up to 1000pF) may be placed between IN+ and IN– to further reduce the noise from interfering.

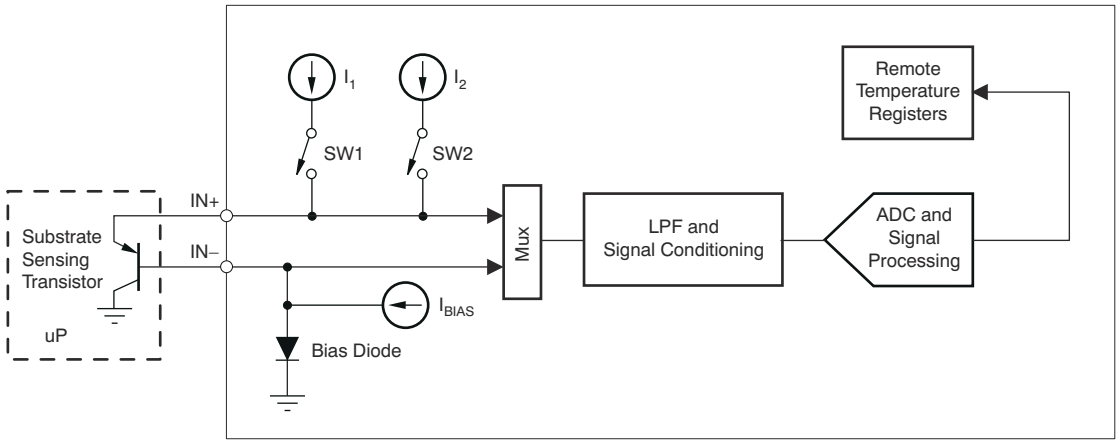


Figure 8-3. Remote Temperature Sensor

The analog sensing signal is pre-processed by a low-pass filter and signal conditioning circuitry, then digitized by the ADC. The resulting digital signal is further processed by the digital filter and processing unit. The final result is stored in the local temperature data register and remote temperature data register, respectively. The eight MSBs are stored in the corresponding Temp-DATA-HByte register, and the three LSBs are stored in the Temp-DATA-LByte register. Refer to the *Temperature Data Registers* section for details.

The format of the final result is in two's complement; see Table 8-1. It should be noted that the device measures the temperature from –40°C to +125°C, although the code represents temperature from –128°C to +127°C.

8.2.2.1 Series Resistance Cancellation

Parasitic resistance (seen in series with the remote diode) to the IN+ and IN– inputs to the AMC6821-Q1 is caused by a variety of factors, including printed circuit board (PCB) trace resistance and trace length. This series resistance appears as a temperature offset in the remote sensor temperature measurement, and causes more than 0.45°C error per ohm. The AMC6821-Q1 is implemented with a TI-patented technology to automatically cancel out the effect of this series resistance, giving a more accurate result without the need for user characterization of this resistance. With this technology, the AMC6821-Q1 is able to reduce the effects of series resistance to typically less than 0.0025°C per ohm.

8.2.2.2 Reading Temperature Data

It is important to note that temperature can be read by an 8-bit value (with 1°C of resolution) from the Temp-DATA-HByte register, or as an 11-bit value (with 0.125°C of resolution) from the Temp-DATA-LByte and Temp-DATA-HByte registers. If only 1°C of resolution is required, the temperature readings can be read back at any time and in no particular order. If reading the 11-bit measurement is required, the process involves a two-register read for each measurement. To get an 11-bit result of the remote sensor, the controller must read the Temp-DATA-LByte register (0x06) first, and then the Remote-Temp-DATA-HByte register (0x0B) to complete the reading. However, to get bit 11 of the local sensor only, or to get both local and remote sensors, the controller must read Temp-DATA-LByte first, Local-Temp-DATA-HByte (0x0A) second, and Remote-Temp-DATA-HByte third. This method causes all associated temperature data registers to be frozen until the Remote-Temp-DATA-HByte register has been read. This process also prevents the high byte data from being updated while the three LSBs are being read, and vice-versa.

Table 8-1. Temperature Data Format

TEMPERATURE (°C)	BINARY DIGITAL CODE (11 BITS)
+127	01111111000
+125	01111101000
+100	01100100000
+75	01001011000
+50	00110010000
+25	00011001000
+10	00001010000
+1	00000001000
0	00000000000
–1	11111111000
–25	11100111000
–50	11001110000
–75	10110101000
–100	10011100000
–125	10000011000
–128	10000000000

8.2.2.3 Temperature Out-of-Range Detection

The AMC6821-Q1 has the following temperature limitation detections:

1. **High and Low Temperature Limit:** The value of the High-Temp-Limit and Low-Temp-Limit registers specify the remote or local temperature ranges of normal operation. When the local or remote temperatures are equal to or above the value of the corresponding High-Temp-Limit register, the LTH or RTH bits in the status register are set ('1'). Likewise, when the local or remote temperatures are less than or equal to the corresponding Low-Temp-Limit register, the LTL or RTL bits in the status register are set ('1').

   When the local temperature is out-of-range (LTH = 1 or LTL = 1), the local temperature out-of-range event occurs. The LTO bit in the status register is set ('1'), and the LTO interrupt is generated via the $\overline{\text{SMBALERT}}$ pin if it is enabled (the LTOIE bit of Configuration Register 2 is set). Similarly, when the remote temperature is out-of range (RTH = 1 or RTL = 1), the remote temperature out-of-range event occurs. The RTO bit in the status register is set ('1'), and the RTO interrupt is generated via the $\overline{\text{SMBALERT}}$ pin if it is enabled (that is, the RTOIE bit of Configuration Register 2 is set).
2. **Critical Limit:** Critical temperature limit is the highest allowed of remote or local temperature. When the temperature is greater than or equal to the corresponding critical temperature, the LTCT or RTCT bit of the status register is set ('1'), the output of the $\overline{\text{OVR}}$ pin goes low, and a non-maskable interrupt is generated through the $\overline{\text{SMBALERT}}$ pin (low).
3. **Passive Cooling Temperature (PSV) Limit:** This limit defines the passive cooling threshold. In the auto remote-temperature-fan control mode, the system enters a passive cooling condition when the remote temperature is equal to or below this limit, and the fan stops. In the maximum fast speed calculated control mode, the fan stops and the system enters a passive cooling condition when both the remote and local temperatures are equal to or below this limit. In passive cooling, the LPSV bit of Status Register 2 (0x03) is set ('1'), and a PSV interrupt is generated on the $\overline{\text{SMBALERT}}$ pin if enabled (PSVIE = 1). Note that reading the Status Register clears the LPSV bit. After reading, if the active control temperature remains equal to or below the PSV temperature, this bit reasserts on next monitoring cycle.

4. **THERM Limit:** This limit is an additional *fail-safe* threshold. When the local or remote temperature is equal to or above this limit, the corresponding L-THERM or R-THERM bit is set ('1'), and the $\overline{\text{THERM}}$ pin is asserted low, which can be used to throttle the CPU clock. Furthermore, the THERM interrupt is generated on the $\overline{\text{SMBALERT}}$ pin if enabled (THERMOVIE = 1). Reading Status Register 1 clears the R-THERM and L-THERM bits. Once cleared, these bits are not reasserted until the temperature falls 5°C below the THERM limit, even if the THERM condition persists. If the THERM-FAN-EN bit of Configuration Register 3 is set ('1'), L-THERM = 1 or R-THERM = 1 forces the fan to run at full speed. When THERM-FAN-EN = 0, the status of the L-THERM and R-THERM bits do not affect the fan speed directly. Note that the THERM limit can be lower or higher than other temperature limits. For example, if the THERM limit is lower than the PSV temperature limit, then the CPU clock can be throttled while the cooling fan is off.

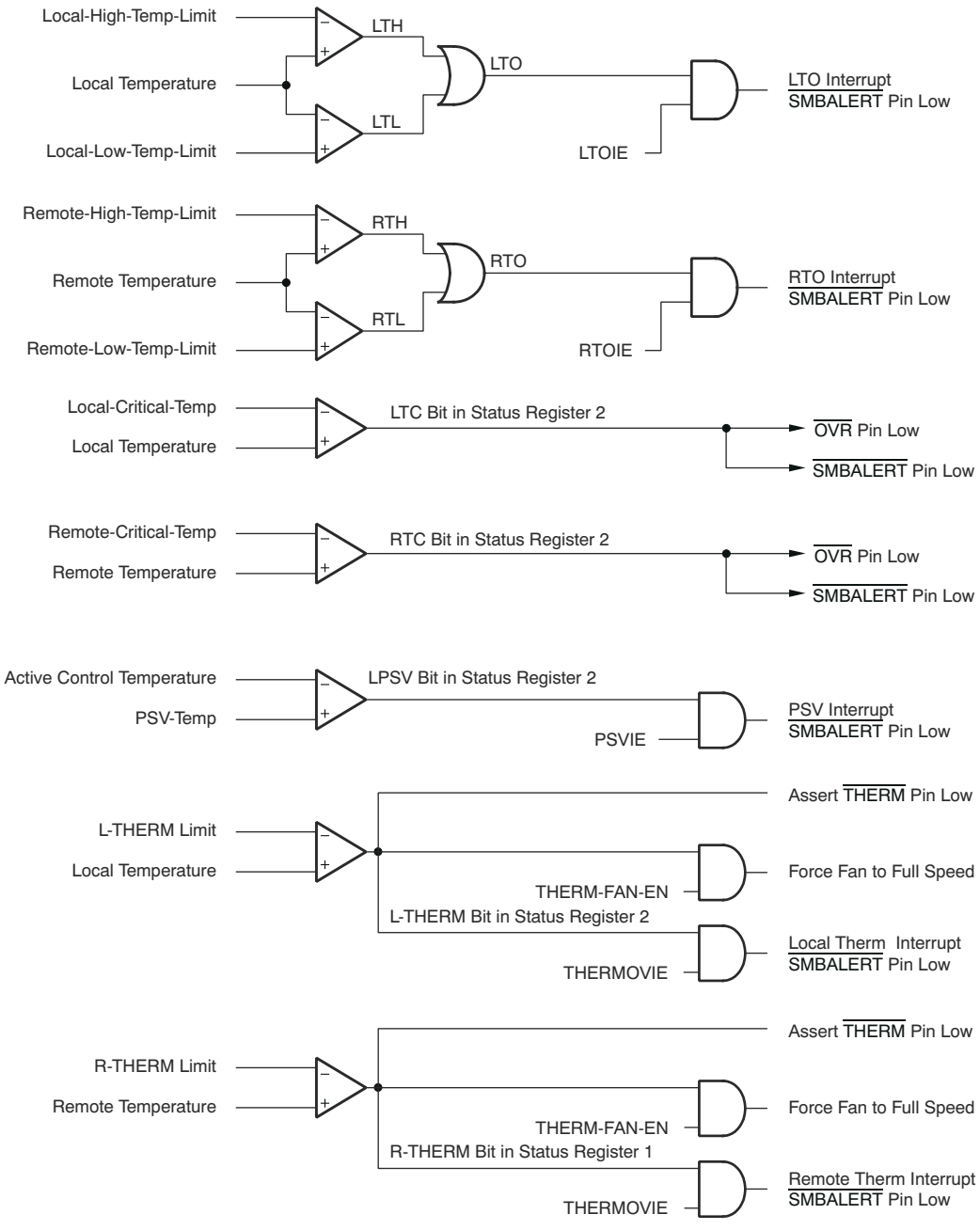


Figure 8-4. Temperature Out-of-Range Detection

8.2.2.4 Remote Temperature Sensor Failure Detection

The remote temperature sensor failure detection determines whether the remote sensor diode has an open-circuit condition, a short-circuit to ground, or a short-circuit (IN+) to (IN–) condition. This fault detection is based on the analog input voltage and is not checked until the first monitoring cycle is completed after power-on.

Reading the fault sensor returns a value of –128°C (0x80). Since the power-on default value of the temperature data registers is 0x80 (–128°C), a reading of 0x80 from the temperature data register immediately after power-on does not indicate a diode fault condition. The remote temperature sensor failure is only checked after the first monitoring cycle has been completed after power-on or reset.

When a remote sensor failure occurs, the remote sensor failure bit (RTF in the Status Register) is set to '1', the $\overline{\text{OVR}}$ pin is forced low, and if the interrupt is enabled (RTFIE = 1), the RTF interrupt is generated through the $\overline{\text{SMBALERT}}$ pin. Once this interrupt is generated, the RTF bit remains '1' and the $\overline{\text{OVR}}$ pin stays low until a power-on reset or software reset is issued, whether or not the failure condition persists.

8.2.3 PWM Output

The PWM-Out pin is an open-drain output. When PWM-EN of Configuration Register 2 is cleared ('0'), the PWM-Out pin is disabled and goes into a high-impedance status. When PWM-EN is set ('1'), the PWM-Out pin is enabled to drive the fan. When enabled, the status of the PWM-Out pin is determined by the PWM duty cycle and phase bits (PWMINV of Configuration Register 1). When PWMINV = 0 (default), the PWM-Out pin goes low for 100% duty cycle (suitable for driving the fan using a PMOS FET). Setting PWMINV to '1' makes the PWM-Out pin go high (with an external pull-up resistor) for a 100% duty cycle. This setting is used to drive an NMOS-power FET.

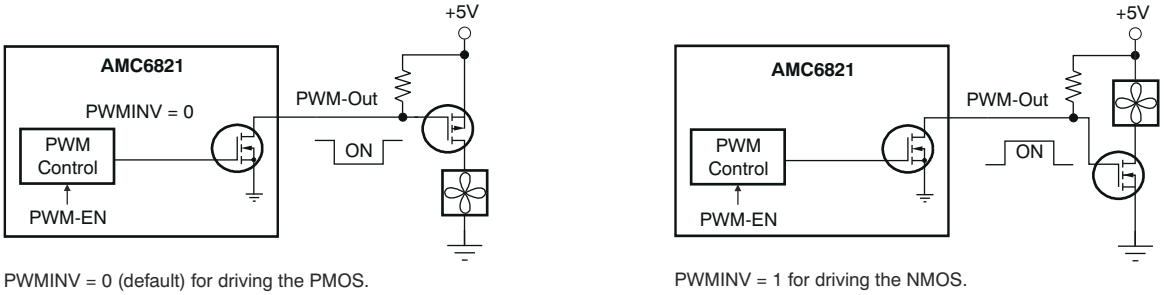


Figure 8-5. PWM Output

8.2.4 PWM Waveform Setting

PWM frequency and duty cycle are programmable. The value of the DCY Register defines the duty cycle: it has 8-bit resolution, 1LSB corresponding to 1/255 (0.392%). Writing 0x00 sets the duty cycle to 0%; writing 0xFF sets the duty cycle to 100%.

PWM frequency has two ranges: the high range is from 1kHz to 40kHz, and the low range is from 10Hz to 94Hz. The PWM-MODE pin status determines which range is selected. When the PWM-MODE pin is tied to ground, the high range is selected. Otherwise, the low range is selected. Bits [PWM2:PWM0] in the Fan Characteristics Register define the frequency; see Table 8-2. The resolution of the PWM waveform period is 0.312µs, corresponding to a 3.2MHz clock. The default value after power-on is 30Hz when the low range is selected, or 25kHz when the high range is selected.

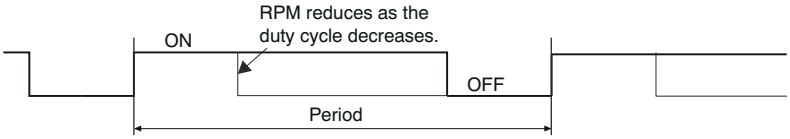


Figure 8-6. PWM Waveform (PWMinv = 1)

Table 8-2. PWM Frequency

PWM2	PWM1	PWM0	PWM FREQUENCY
When the PWM-MODE Pin is Floating or Tied to V_{DD}			
0	0	0	10Hz
0	0	1	15Hz
0	1	0	23Hz
0	1	1	30Hz (default)
1	0	0	38Hz
1	0	1	47Hz
1	1	0	62Hz
1	1	1	94Hz
When the PWM-MODE Pin is Tied to GND			
0	0	0	1kHz
0	0	1	10kHz
0	1	0	20kHz
0	1	1	25kHz (default)
1	0	0	30kHz
1	0	1	40kHz
1	1	0	40kHz
1	1	1	40kHz

8.2.5 Fan Speed Measurement

The AMC6821-Q1 monitors the fan speed (RPM) via the TACH pin, as illustrated in Figure 8-7. The TACH-EN bit of Configuration Register 2 (bit 2, 0x01) enables the fan speed measurement. When TACH-EN is cleared ('0'), the measurement is disabled. The measurement is enabled when the TACH-EN bit is set to '1'. This section describes the device behavior when TACH-EN is set ('1').

The on-chip fan-speed counter does not count the fan tach output pulses directly because of the low RPM of the fan. Instead, the period of the fan revolution is measured by gating an on-chip clock (100kHz). The result is stored in the TACH-DATA Register that contains two bytes (16 bits total). RPM monitoring is disabled when the START bit of Configuration Register 1 or the TACH-EN bit of Configuration Register 2 is cleared ('0'), and is enabled when START = 1 and TACH-EN = 1.

If the TACH-MODE bit is cleared, RPM monitoring stops and the TACH-DATA register is not updated when the duty cycle is less than 7% for the software duty cycle mode and auto-temperature-fan control modes. In software-RPM mode, RPM monitoring is always performed and updated after each monitoring. If the TACH mode = '1' the RPM monitoring is always performed, and the TACH data are always updated after each monitoring.

8.2.5.1 Tach-Data Register

Two fan tach pulse periods (PSPR = 0) or four tach pulse periods (PSPR = 1) are measured and the result is stored in the TACH-DATA Register, as shown in Figure 8-7. Counting stops if the counter is over-range; the measurement cycle repeats until monitoring is disabled, and the fan speed (RPM) can be calculated as shown in Equation 2:

$$RPM = \frac{(100{,}000 \times 60)}{(\text{Value of TACH-DATA Register})} \quad (2)$$

8.2.5.1.1 Reading the Tach Data Register

To read the fan speed, both TACH-DATA-LByte and TACH-DATA-HByte must be read. TACH-DATA-LByte must be read first. This reading causes TACH-DATA-HByte to be frozen until both the high and low byte registers have been read from, preventing TACH reading errors.

8.2.5.1.2 RPM Measurement Rate

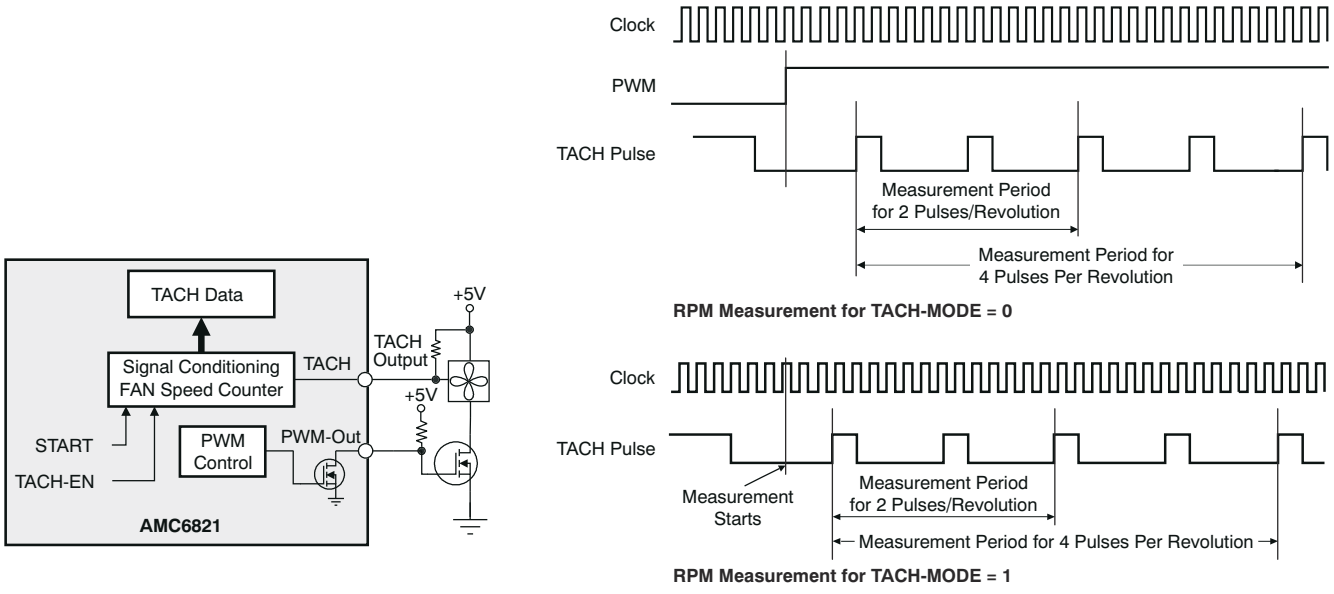
The TACH-FAST bit of Configuration Register 4 determines the rate. When TACH-FAST = 1, the TACH-DATA Register is updated every 250ms (fast monitoring). When TACH-FAST = 0 (default), the reading is updated every second (standard monitoring period).

8.2.5.1.3 Select Number of Pulses/Revolution

The speed sensor of most common fans provides two or four TACH pulses per revolution. The PSPR bit of Configuration Register 4 specifies how many pulses per revolution are generated. PSPR = 1 indicates four pulses/revolution and PSPR = 0 (default) indicates two pulses/revolution.

8.2.5.1.4 Tach Mode Selection

The TACH-MODE bit of Configuration Register 2 specifies the TACH pulse output mode of the fan. Some fans (such as three- and two-wire) are powered directly by the PWM, and must be *PWM-On* to provide a TACH pulse output. When the PWM-Out pin switches these fans ON/OFF directly, the PWM-Out must be kept ON to power the fan during the measurement. In this case, the TACH-MODE bit of Configuration Register 2 must be cleared ('0'). When TACH-MODE = 0, the PWM-Out pin is kept ON during the critical tach edges of the measurement period. Clearing the TACH mode ('0') also enables the internal correction circuitry to correct the error caused by the extra duty cycle applied in the measurement period. The power-on default value of the PWM mode is '0'.



a) Block Diagram of Fan Speed Monitoring

b) Measuring the Period of TACH Pulses to Determine the Fan Speed

Figure 8-7. Fan Speed Measurement

Some fans (such as the JMC® four-wire fan) are powered directly by dc power, instead of being powered by the PWM. In this case, the TACH mode must be set to '1'. When TACH-MODE = 1, the PWM-Out pin is not forced ON; instead, the status is controlled completely by the DCY register, just as in normal operation. Setting TACH-MODE to '1' also disables the internal correction circuit because no extra duty cycle is applied. Setting the TACH mode to '1' allows TACH reading continuously, regardless of the status of the PWM-Out pin.

The selection of the TACH mode affects the RPM monitoring and control. When the TACH-MODE bit is equal to '1', the duty cycle of the PWM-Out pin is always determined by the calculated value; the TACH data are always updated at every RPM monitoring. However, when the TACH-MODE bit is equal to '0', in the Software-RPM Control mode the PWM-Out pin is forced to 30% if the calculated duty cycle is less than 30%; in other modes, the PWM-Out pin is forced to 0% and the TACH data are not updated if the calculated duty cycle is less than 7%.

8.2.5.1.5 Fan RPM Out-of-Range Detection

The larger value of the TACH data corresponds to a slower speed. When the TACH data are larger than the TACH-Low-Limit, the fan runs at a speed below the predefined minimum RPM, and the FANS bit in Status Register 1 is set to '1'. Note that no FANS (fan-slow) detections are made during spin-up. The FANS bit is cleared ('0') only after reading this register and reasserted ('1') in the next monitoring if a fan-slow is detected. After spin-up, FANS is set ('1') even if the TACH data are less than the TACH-Low-Limit until the register is read.

When the TACH data are less than the TACH-High-Limit, the fan runs at a speed above the predefined maximum RPM, and the RPM-ALARM bit in Status Register 1 is set ('1'). Note that the RPM-ALARM bit is cleared when reading the register. Once cleared, this bit is not reasserted in the next monitoring cycle even if the condition persists. This bit may be reasserted only if the RPM drops below the allowed maximum speed.

When FANS = 1 or RPM-ALARM = 1, there is a fan-out-of-range interrupt and FAN-ORN is generated if the FANIE bit in Configuration Register 1 is set ('1'). This interrupt makes the $\overline{\text{SMBALERT}}$ pin go low.

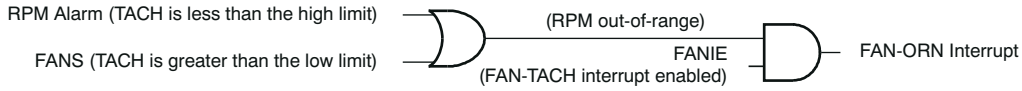
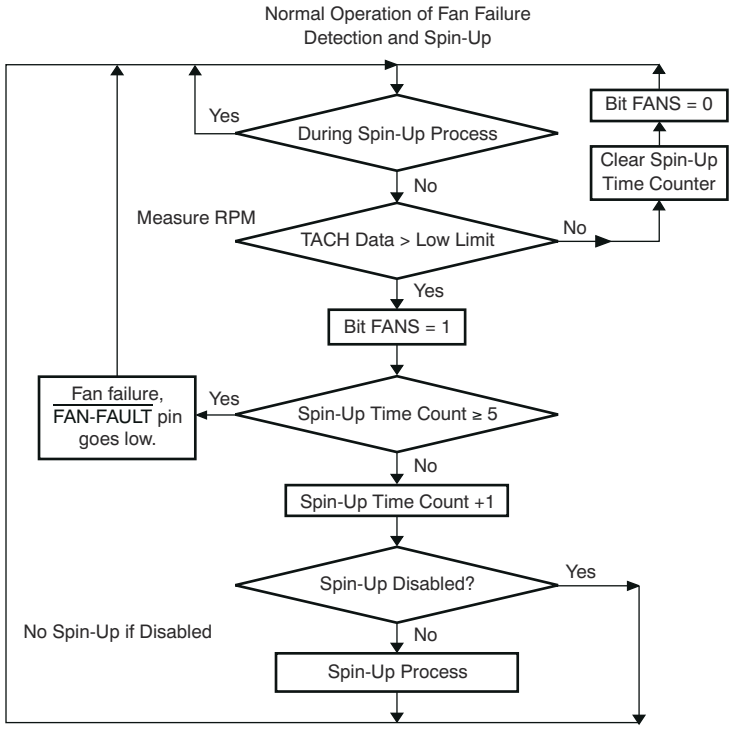


Figure 8-8. RPM Out-of-Range Detection

8.2.6 Fan Failure Detection

When the TACH data are larger than the TACH low limit, the fan runs at a speed below the predefined minimum RPM. When this condition occurs, a spin-up process is applied to start the fan again when spin-up is enabled. Bits [STIME2:STIME0] of the Fan Characteristics Register define this time period. Figure 8-9 shows the function of the fan failure detection. Refer to the Fan Spin-Up section.

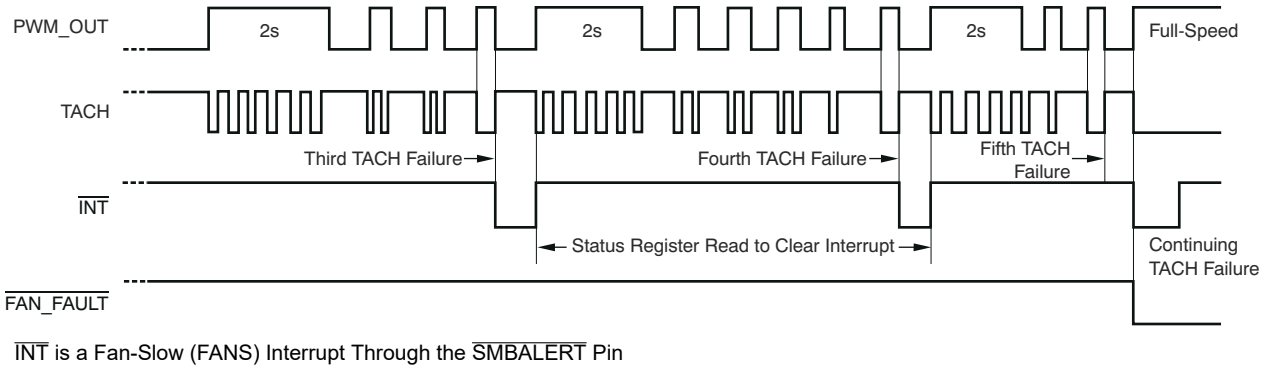
The fan speed is measured immediately after spin-up; the TACH-FAST bit of Configuration Register 4 determines the monitoring rate. If the fan does not return to a normal range after five consecutive spin-ups, a FAN-FAILURE occurs; the $\overline{\text{FAN-FAULT}}$ pin goes low when it is enabled (the FAN-FAULT-EN bit of Configuration Register 1 is set), and the spin-up process continues. If the fan returns to a normal speed range before the fifth spin-up, the $\overline{\text{FAN-FAULT}}$ pin does not go low even though the FANS bit is still set to '1'. No FANS (fan-slow) detections are performed during spin-up. After the FAN-FAULT pin goes low, spin-up is performed indefinitely until the RPM reading returns to within normal range or the spin-up is disabled.



Measure the RPM continuously once every 0.25s (TACH-FAST bit = 1) or 1s (TACH-FAST = 0), even after a fan failure. However, there are no FANS detections during spin-up.
The $\overline{\text{FAN-FAULT}}$ pin is negated if the fan returns to a normal RPM range.

Figure 8-9. Fan Failure Detection and Spin-Up

The $\overline{\text{SMBALERT}}$ pin continues to generate interrupts after the assertion of the $\overline{\text{FAN-FAULT}}$ pin because the tach measurement continues even after a fan failure. Should the fan recover from the failure condition, the $\overline{\text{FAN-FAULT}}$ pin signal is negated and the fan returns to normal operating speed. Figure 8-10 shows the operation of a FANS interrupt.



$\overline{\text{INT}}$ is a Fan-Slow (FANS) Interrupt Through the $\overline{\text{SMBALERT}}$ Pin

Figure 8-10. Operation of the $\overline{\text{FAN-FAULT}}$ Pin With a Spin-Up Time = 2 Seconds

8.2.7 $\overline{\text{FAN-FAULT}}$ Pin

The $\overline{\text{FAN-FAULT}}$ pin is an open-drain output pin (see Figure 8-11). When the FAN-FAULT-EN bit of Configuration Register 1 is cleared ('0'), this pin is disabled and is always in a high-impedance status. When FAN-FAULT-EN = 1, the pin is enabled and the status indicates a fan-failure. The pin asserts low when a fan failure occurs. $\overline{\text{FAN-FAULT}}$ is negated when the fan returns to normal speed.

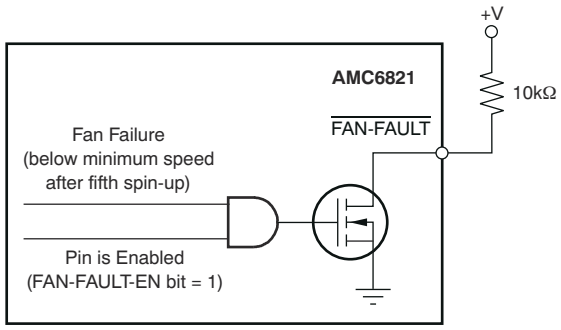


Figure 8-11. $\overline{\text{FAN-FAULT}}$ Pin

8.2.8 Fan Control

8.2.8.1 $\overline{\textit{THERM}}$ Pin and External Hardware Control

Figure 8-12 shows the $\overline{\text{THERM}}$ pin is a bidirectional I/O.

8.2.8.1.1 $\overline{\text{THERM}}$ Pin as an Output

As an open-drain output, the $\overline{\text{THERM}}$ pin is the indicator of temperature over the THERM limit. When the remote temperature exceeds the Remote-THERM-Limit, or when the local temperature is greater than the Local-THERM-Limit, the $\overline{\text{THERM}}$ pin goes low and remains low until the measured temperature falls 5°C below the exceeded THERM limit.

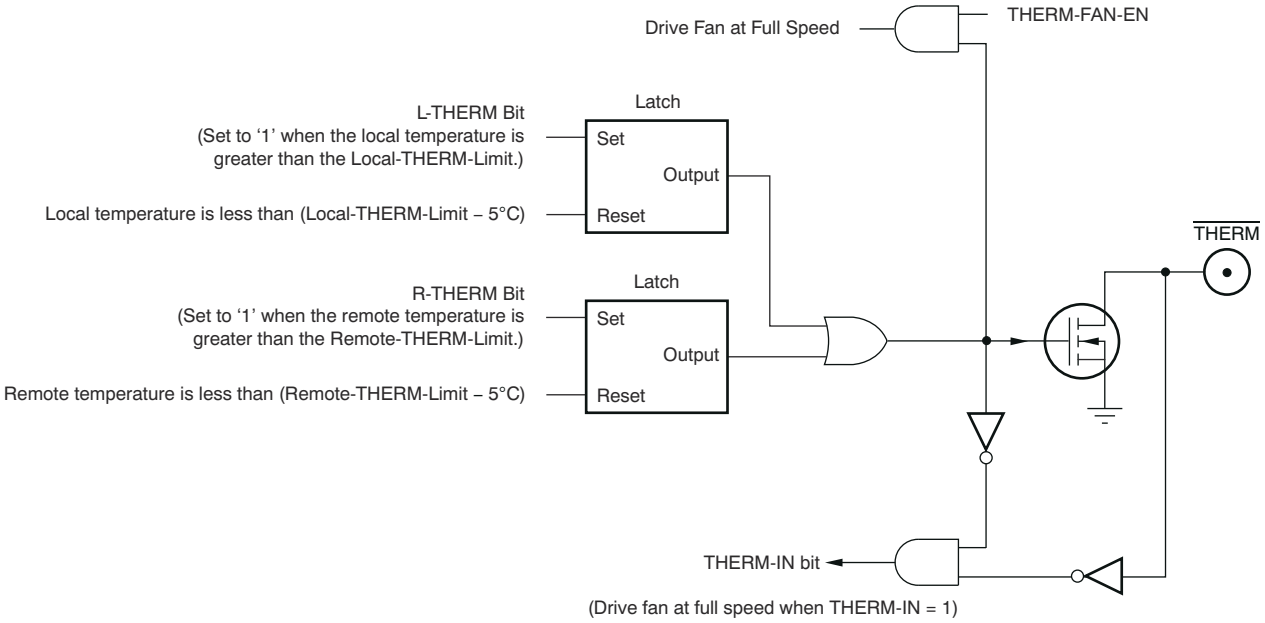


Figure 8-12. Structure of the THERM Pin

When the THERM limit is exceeded, the corresponding status flag bit (R-THERM or L-THERM of Status Register 1 or Status Register 2) is set to '1', and the THERM interrupt through the SMBALERT pin is generated if it is enabled (THERMOVIE of bit Configuration Register 1 is set to '1'). This interrupt forces the SMBALERT pin low. Note that the THERM pin is always forced to low when R-THERM = 1 or L-THERM = 1, no matter what the status of THERMOVIE is. Reading the status registers clears the flag bit (R-THERM and L-THERM). Clearing the flag bit makes the SMBALERT pin go back to high, but does not negate the THERM pin. It remains low until the temperature falls 5°C below the exceeded THERM limit. After this bit is cleared, the active flag bit (R-THERM for remote temperature or L-THERM for local temperature) and the THERM interrupt are not re-armed until the temperature falls 5°C below the exceeded THERM limit. Figure 8-13 shows this procedure.

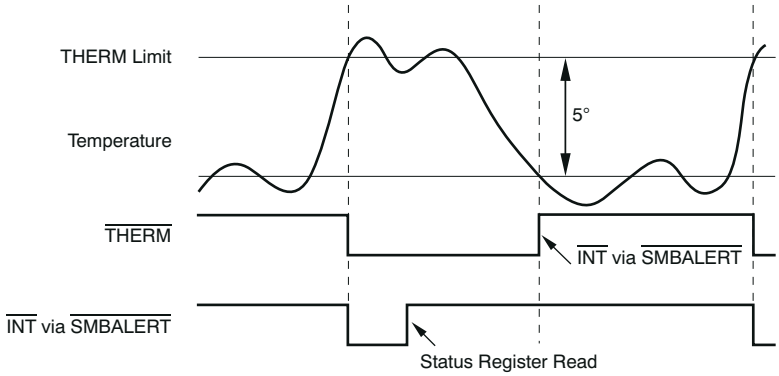


Figure 8-13. Operation of the Therm Interrupt and the THERM Pin

When working as an output, the status of the THERM pin affects the RPM fan. If the THERM-FAN-EN bit is set ('1'), the fan goes to full-speed (that is, the duty cycle is 100%) when the THERM pin goes low. However, when THERM-FAN-EN = 0, the status of the THERM pin does not affect the fan speed.

8.2.8.1.2 THERM Pin as an Input

When this pin works as input, it is the input of the external hardware control signal; the THERM-IN bit of Status Register 2 reflects the input. When the THERM pin is pulled low as an input, THERM-IN is set ('1') and the fan is driven at full speed (that is, the duty cycle is 100%), no matter what THERM-FAN-EN is. The THERM-FAN-EN bit has no effect when the THERM pin works as an input.

8.2.8.2 Fan Spin-Up

The PWM duty cycle controls the cooling fan speed. To spin up a fan from a stopped state or under-speed status, the spin-up process is applied to overcome the fan inertia. During the first third of spin-up, the duty cycle of the PWM gradually increases from 33.3% to 100%, and then maintains at 100% through the rest of the process. At the end of the spin-up process, the duty cycle is adjusted to 33.3%. After starting, the fan speed is controlled normally. Figure 8-14 shows the spin-up process. The bits [STIME2:STIME0] (bits 2:0 of 0x20) define the spin-up time, from 0.2 seconds to 8 seconds, as shown in Table 8-3. Fan speed is monitored immediately after the spin-up process.

Spin-up is disabled by setting the FSPD bit of the Fan Characteristics Register to '1'. If disabled, the spin-up process is not applied when the fan stops or an RPM is detected below the minimum speed. The TACH low limit register defines the minimum speed. After power-on or reset, the FSPD bit is cleared and the spin-up is always performed, regardless of the state of the FANS bit (bit 1 of 0x02).

Note that no FANS (fan-slow) detections are performed during spin-up. This bit is cleared ('0') only after reading it, and reasserts '1' in the next monitoring if a fan-slow condition is detected. After spin-up, FANS is set ('1') even if the TACH data are less than the TACH low limit until the flag is read.

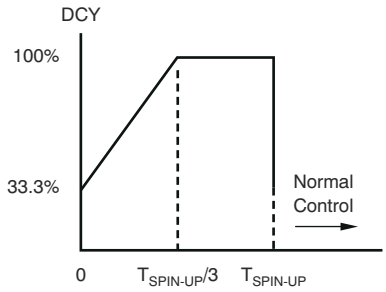


Figure 8-14. Spin-Up Process

Table 8-3. Spin-Up Time

STIME2	STIME1	STIME0	SPIN-UP TIME (SECONDS)
0	0	0	0.2
0	0	1	0.4
0	1	0	0.6
0	1	1	0.8
1	0	0	1
1	0	1	2 (default)
1	1	0	4
1	1	1	8

8.2.8.3 Normal Fan Speed Control

The fan speed is controlled by four different modes:

- software DCY control;
- software RPM control,
- auto remote temperature fan control;
- maximum fast-speed calculated control.

The Auto Temperature-Fan Control mode consists of auto remote temperature-fan control and maximum fast-speed calculated control. It is an intelligent closed-loop control. In this mode, the fan speed is controlled either by the remote temperature (Auto-Remote Temperature-Fan Control) or by maximum speed calculated for internal and remote temperature. This control mode optimizes fan speed for a given temperature to intelligently manage the system thermals/acoustics. The user writes the proper registers to define the linear feedback control algorithm parameters. After programming, the AMC6821-Q1 runs stand-alone, even without the intervention of the micro-controller. It ensures that if the controller or system locks up, the fan can still be controlled based on temperature measurements, and the fan speed adjusted to correct any changes in system temperature. Software-RPM works as a fan speed regulator to maintain the speed at a programmable target value. It is a closed-loop mode and can run stand-alone as well. The Software-DCY mode is an open-loop mode; the PWM output duty cycle changes to the target value immediately after the user writes the desired duty cycle to the device registers.

Bits FDRC1 and FDRC0 in Configuration Register 1 determine the operation mode.

8.2.8.3.1 Software DCY Control Mode

When the bits [FDRC1:FDRC0] = [00], the fan works in the software DCY control mode. The host writes the desired duty cycle value corresponding to the required RPM into the DCY register. The duty cycle changes to the new value immediately after the writing. In this mode, if the TACH measurement is enabled (bit 2 of 0x01 = 1) and the TACH-MODE bit (bit 1 of 0x01) is cleared ('0'), the duty cycle from the PWM-OUT pin is forced to 0% when the value in the DCY register is less than 7%. However, if the TACH measurement is disabled (bit 2 of 0x01 is cleared) or the TACH mode is set ('1'), the DCY register always keeps the programmed value written by the host and is not forced to '0' even when the programmed value is less than 7%.

8.2.8.3.2 Software-RPM Control Mode (Fan Speed Regulator)

This mode works as a fan speed regulator that maintains the speed at a programmable target value. It works only when the TACH measurement is enabled (bit 2 of 0x02 = 1). When the bits [FDRC1:FDRC0] = [01], the fan works in the software RPM control mode, as shown in Figure 8-15. The host writes the proper value into the TACH Setting Register to set the target fan speed. The actual fan speed is monitored by an on-chip fan speed counter, and the result is stored in the TACH-DATA Register (refer to the Fan Speed Measurement section for more details). The actual speed is compared with the setting value. If there is a difference, the duty cycle is adjusted.

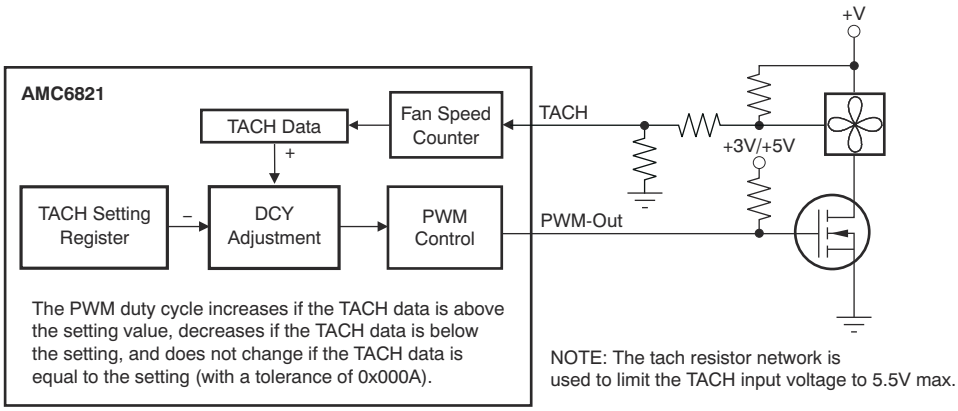


Figure 8-15. Software RPM Control

The monitoring and adjustment is made once every second, or once every 250ms, as determined by the TACH-FAST bit of Configuration Register 4 (bit 5, 0x04). Bits [STEP1:STEP0] of the DCY-RAMP Register define the allowed amount of each adjustment. When the difference between the values of the TACH-DATA and TACH Setting Registers are equal to or less than 0x000A, the adjustment finishes. 0x000A corresponds to about 1.8% tolerance for 10,000RPMs, or 0.9% for 5000RPMs. This measurement architecture is illustrated in Figure 8-16.

In practice, the selected target speed must be not too low to operate the fan. When the TACH-MODE bit (bit 1 of 0x02) is cleared ('0'), the duty cycle of PWM-Out is forced to 30% when the calculated desired value of duty cycle is less than 30%. Therefore, the TACH setting must be not greater than the value corresponding to the RPM for 30% duty cycle. When TACH mode = '1', the TACH setting must not be greater than the value corresponding to the allowed minimum RPM at which the fan runs properly.

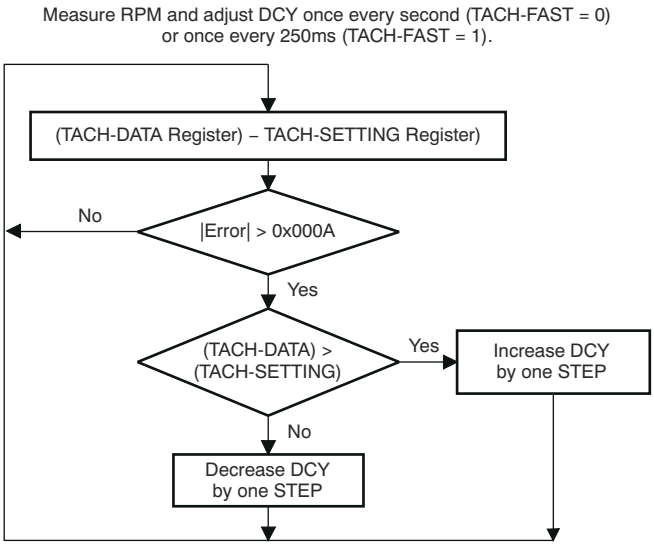


Figure 8-16. RPM Fan DCY Loop

8.2.8.3.3 Auto Temperature Fan Mode

The Auto Temperature-Fan mode is a closed-loop control that optimizes fan speed for a given temperature to intelligently manage the system thermals/acoustics. It runs stand-alone even without the intervention of a controller. The AMC6821-Q1 has two auto temperature fan control modes. When the bits [FDRC1:FDRC0] = [10] (default), the fan is in the Auto Remote Temperature-Fan Speed control mode. The temperature reading from the remote temperature sensor is the active control temperature that controls the PWM duty cycle. When the bits [FDRC1:FDRC0] = [11], the fan is in the maximum fast-speed calculated control mode. The local temperature and the remote temperature have independently-programmed control loops with different parameters. In the maximum fast-speed calculated control mode, the required fan speed is calculated for the remote and local channels, respectively. Whichever control loop calculates the fastest speed based on the measured temperature drives the fan. After the monitor starts, the PWM duty cycle is determined by the actual control temperature. When the temperature is above the low temperature and below the high temperature, the internal control loop automatically adjusts the duty cycle to a proper value according to the measured temperature. When the temperature rises, the duty cycle increases to a higher value; when the temperature drops, the duty cycle reduces. This architecture makes the fan always run at an optimal speed. This adjustment is based on the control-loop parameters defined in the Local TEMP-FAN Control Register, Remote TEMP-FAN Control Register, and the DCY-RAMP Register. Changing the parameters changes the desired value of the duty cycle and the fan speed.

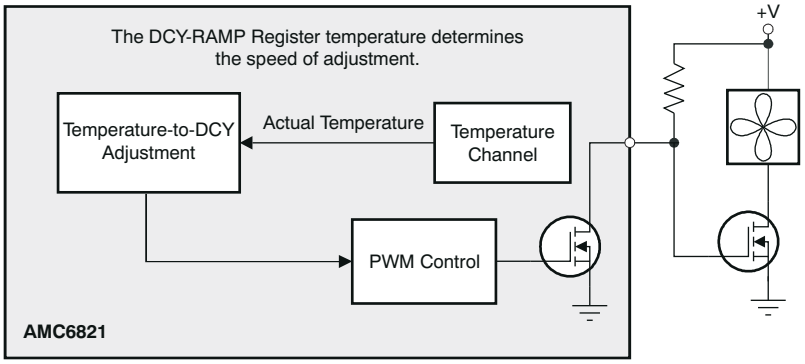


Figure 8-17. Auto Fan Temperature Loop

The bits [R-TEMP4:R-TEMP0] of the Remote TEMP-FAN Control Register and the bits [L-TEMP4:L-TEMP0] of the Local TEMP-FAN Control Register are the low temperature bits that define the low temperature of the control loops. Bits [SPL2:SPL0] of these registers are the slope bits that define the increment of the duty cycle when the temperature increases 1°C. The bits [RATE2:RATE0] of the DCY-RAMP Register (bits [4:1], 0x23) specify the updating rate of the duty cycle in the temp-fan control mode, and the bits [STEP1:STEP0] define how much the duty cycle is adjusted by each updating. The target duty cycle for temperature T1 and the HIGH-TEMP (high temperature) can be calculated by Equation 3:

$$\text{Target DCY at T1} = \text{DCY-LOW-TEMP} + (\text{T1} - \text{LOW-TEMP}) \times \text{SLOPE};$$

$$\text{HIGH-TEMP} = (\text{LOW-TEMP}) + \frac{(100 - \text{DCY-LOW-TEMP})}{\text{SLOPE}} \quad (3)$$

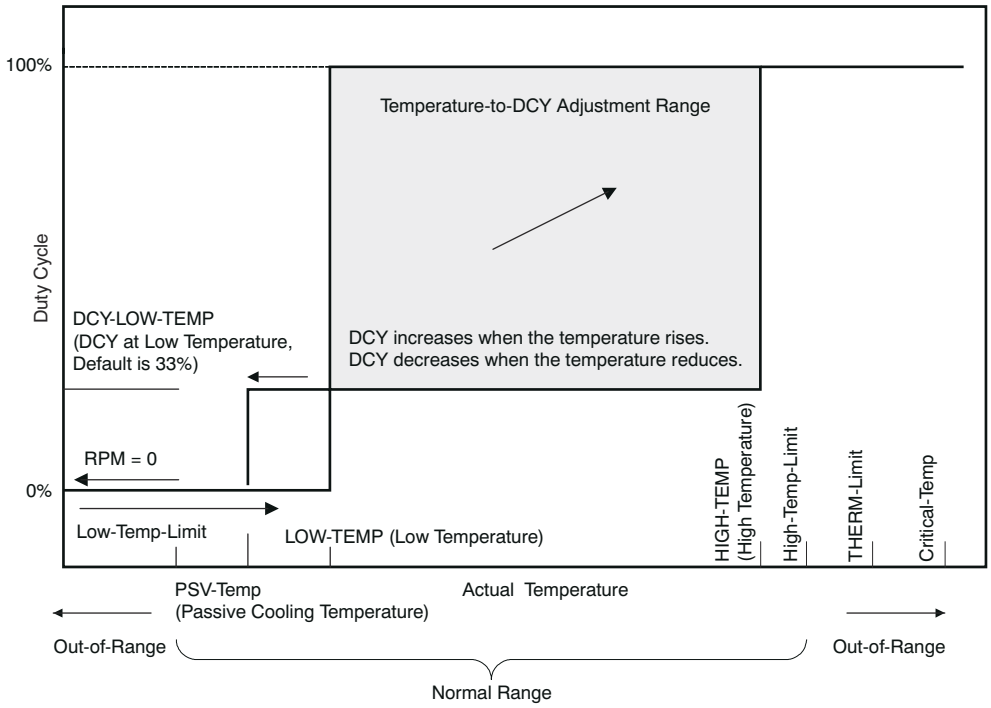


Figure 8-18. Active Control Temperature—PWM Duty Cycle

When the active control temperature is equal to or below the corresponding low temperature, the duty cycle is equal to the value of the DCY-LOW-TEMP Register and the fan runs at a predefined minimum speed. When the control temperature is equal to or higher than the corresponding high temperature, the PWM duty cycle is set to 100% and the fan runs at full speed. When the active control temperature is equal to or below the corresponding

value of the PSV-Temp Register (the predefined passive cooling temperature), the fan stops and the PWM duty cycle is set to 0.

When the actual duty cycle is different from the desired value, the duty cycle is adjusted automatically. When the RAMPE bit of the DCY-RAMP Register is cleared ('0'), the duty cycle changes to the desired value immediately after being calculated. When the RAMPE bit is '1', the duty cycle changes to the new value gradually.

The DCY-RAMP Register specifies how quickly the duty cycle changes. The duty cycle can be checked every 0.0625 second to every eight seconds, depending on the bits [RATE2:RATE0] bits. It changes 1/255(0.392%) to 4/255 (1.57%) each time, depending on the bits [STEP1:STEP0] bits. When the difference between the actual value and the target value is equal to or less than the adjustment threshold (as defined by the bits [THRE1:THRE0] bits), the adjustment finishes. See the DCY-RAMP Register for details. When the TACH monitoring is enabled (TACH-EN bit, bit 2 of 0x02, is set to '1') and the TACH-MODE bit (bit 1 of 0x02) is cleared ('0'), the duty cycle is forced to 0% when the calculated value is less than 7%. If the TACH monitoring is disabled (TACH-EN = 0) or the TACH-MODE bit is set ('1'), the duty cycle is always set to the calculated value even if the value is less than 7%.

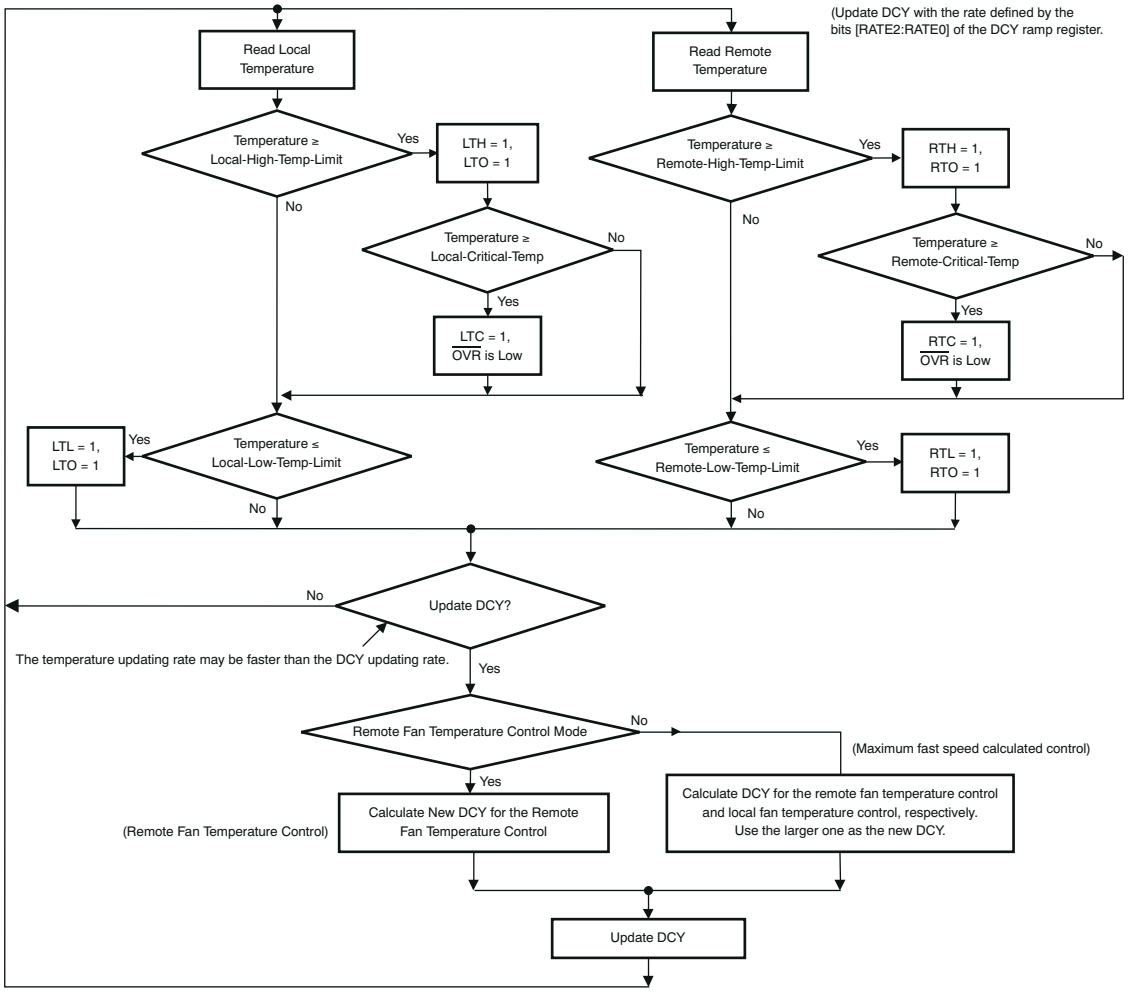


Figure 8-19. Temperature Monitoring Flow Chart

8.2.9 Interrupt

The AMC6821-Q1 provides two interrupt output pins, $\overline{\text{OVR}}$ and $\overline{\text{SMBALERT}}$.

8.2.9.1 $\overline{\text{OVR}}$ Pin

$\overline{\text{OVR}}$ is an open-drain output pin that works as an over-critical temperature limit (shutdown threshold) indicator and remote sensor failure indicator. Figure 8-20 shows the architecture. Setting the OVREN bit of Configuration Register 4 to '1' enables this pin; clearing OVREN ('0') disables it. When disabled, the $\overline{\text{OVR}}$ pin is in a high-impedance status. When enabled, the status is controlled by the over-critical temperature flag and remote sensor failure flag bits of the Status Registers.

When the temperature is over the critical limit (shutdown threshold), the corresponding over-critical limit flag of the Status Register (RTC for the remote channel and LTC for the local channel) is set ('1'). This flag is cleared ('0') when reading the Status Registers. Once cleared, this bit is not reasserted until the temperature falls 5°C below the exceeded critical limit, even if the over-critical limit condition persists. When the temperature is equal to or above the critical temperature limit, the $\overline{\text{OVR}}$ pin is asserted (active low) to indicate this critical condition. As the over-critical temperature limit indicator, the $\overline{\text{OVR}}$ pin remains low once asserted until the measured temperature falls 5°C below the exceeded critical limit.

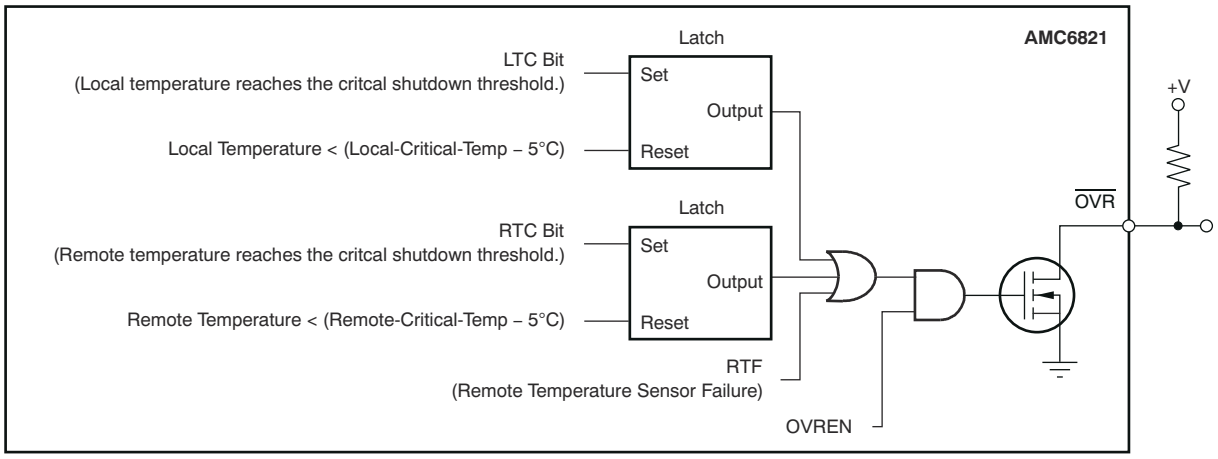


Figure 8-20. $\overline{\text{OVR}}$ Pin

When a remote temperature sensor failure condition is detected (either short-circuit or open-circuit), the remote temperature sensor failure bit (RTF) in Status Register 1 (bit 5, 0x02) is set ('1') and the $\overline{\text{OVR}}$ pin is forced low no matter what the status of RTFIE is. This value indicates a remote sensor failure condition. Once this condition occurs, the RTF bit remains '1' and the $\overline{\text{OVR}}$ pin stays low until a power-on reset or software reset is issued, regardless if the failure condition continues thereafter. RTF = 1 also generates an RTF interrupt through the $\overline{\text{SMBALERT}}$ pin when RTFIE = 1.

8.2.9.2 $\overline{\text{SMBALERT}}$ Pin

The $\overline{\text{SMBALERT}}$ pin is a standard interrupt output defined by SMBus specification revision 2.0. This pin is an open-drain output pin and is illustrated in Figure 8-23.

8.2.9.3 SMBALERT Interrupt Behavior

When an out-of-limit event occurs, the proper flag bits in the status registers are set ('1'), and the corresponding interrupts are generated, if enabled. When an interrupt is generated, the $\overline{\text{SMBALERT}}$ pin asserts low. The host can poll the device status registers to get the information, or give a response to the SMBALERT interrupt signal. It is important to note how the SMBALERT output and status bits behave when writing interrupt-handler software. Figure 8-21 shows how the SMBALERT output and status bits behave.

Once a limit is exceeded, the corresponding status bit is set to '1'. The status bit remains set until the error condition subsides and the status register gets read. The status bits are referred to as being *sticky* because they remain set until read by software. This design ensures that out-of-limit events cannot be missed if the software is polling the device periodically. The SMBALERT output remains low for the entire duration that the reading is out of limits and remains low until the status register has been read. This architecture has implications on how software handles the interrupt.

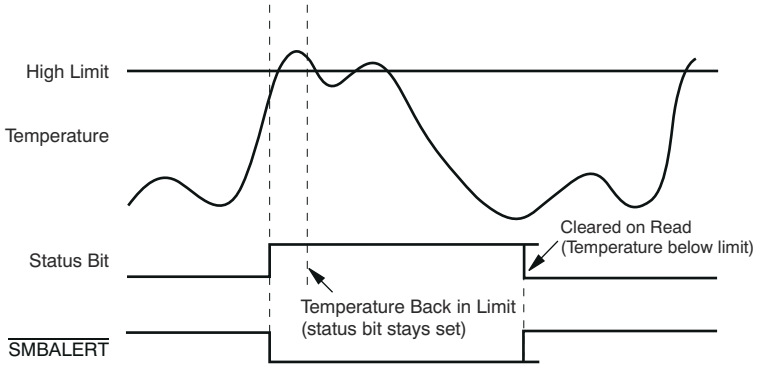


Figure 8-21. $\overline{\text{SMBALERT}}$ Pin and Status Bits Behavior

8.2.9.4 Handling SMBALERT Interrupts

To prevent the system from being tied up while servicing interrupts, it is recommend to handle the SMBALERT interrupt in this manner:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Disable the interrupt source by clearing the appropriate enable bit in the configuration registers.
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt source bit has cleared, reset the corresponding interrupt enable bit to '1'. This reset makes the SMBALERT output and status bits behave as shown in Figure 8-22.

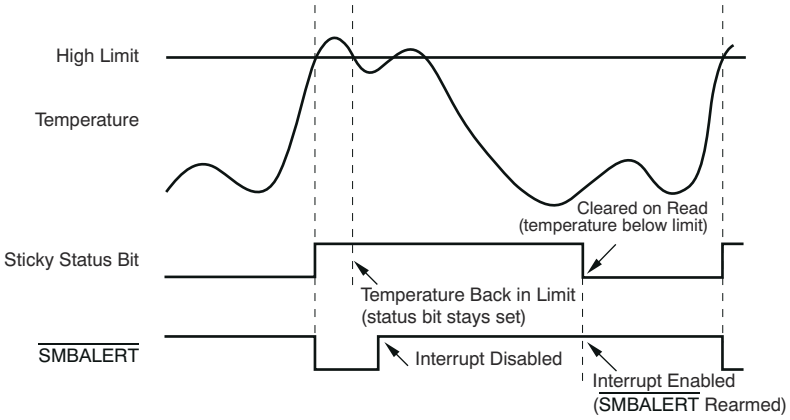


Figure 8-22. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$

Individual interrupts can be masked by clearing the corresponding interrupt enable bit in the configuration registers to prevent SMBALERT interrupts. Note that masking an interrupt source only prevents the $\overline{\text{SMBALERT}}$ pin output from being asserted; the appropriate status bit gets set as normal.

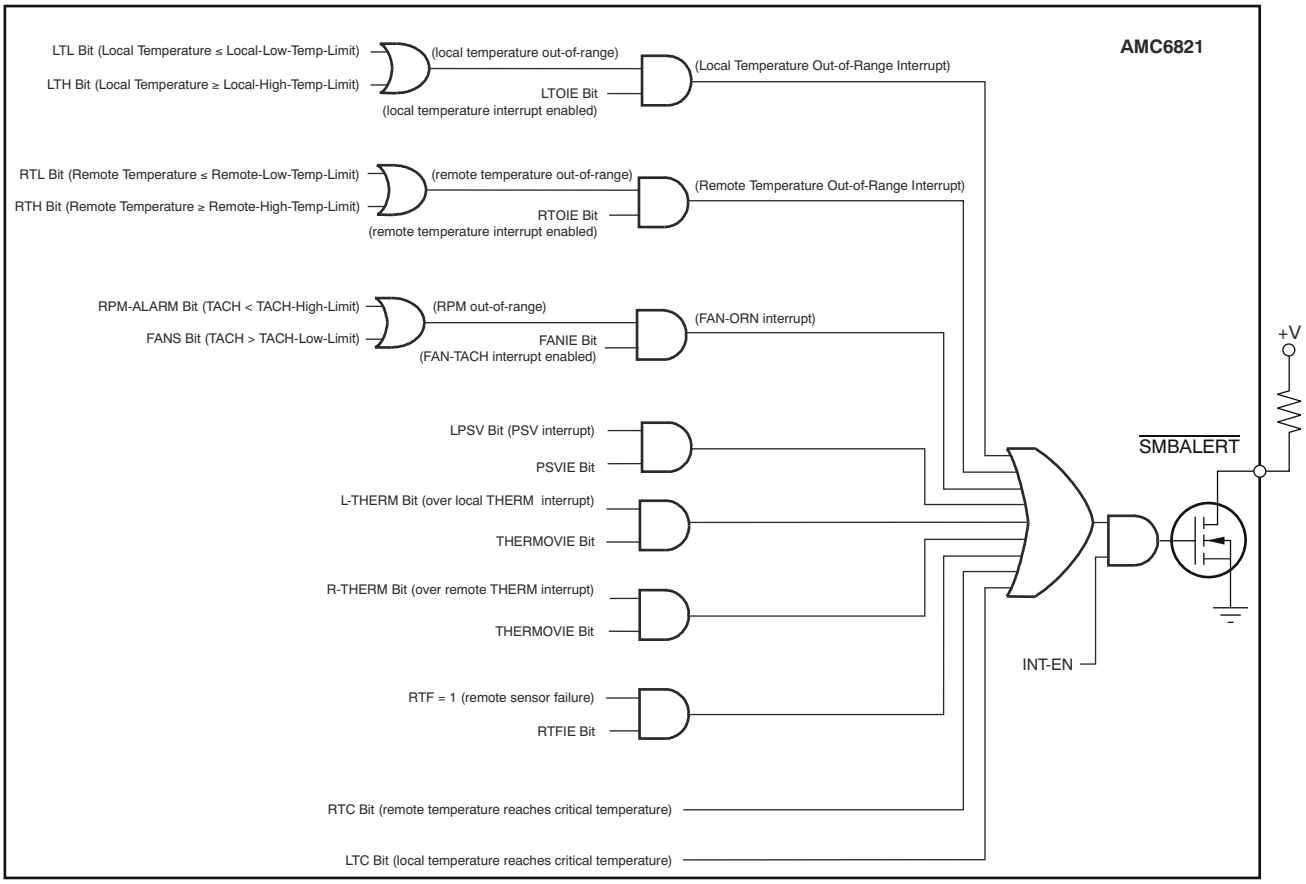


Figure 8-23. $\overline{\text{SMBALERT}}$

8.3 Device Functional Modes

8.4 Programming

8.4.1 SMBus Interface

The AMC6821-Q1 communicates through the serial system management bus (SMBus). The AMC6821-Q1 is connected to this bus as a slave device, under the control of a bus master. The AMC6821-Q1 has a 7-bit serial bus address that is programmable by properly connecting the address pins A0 and A1. Table 8-4 shows the selection of the AMC6821-Q1 slave address. The address selection pins should be either tied directly to V_{DD} or GND. For the NC condition, they should be unconnected with minimum trace capacitance. Note that the address is checked only on a reset or power-up condition.

Table 8-4. AMC6821-Q1 Address Select(1)

A0	A1	ADDRESS
GND	GND	0011000
NC	GND	0011010
V_{DD}	GND	0011001
GND	NC	0101100
NC	NC	0101110
V_{DD}	NC	0101101
GND	V_{DD}	1001100

Table 8-4. AMC6821-Q1 Address Select(1) (continued)

A0	A1	ADDRESS
NC	V_{DD}	1001110
V_{DD}	V_{DD}	1001101

(1) NC = No connection.

8.4.1.1 Communication Protocols

The AMC6821-Q1 employs four standard SMBus protocols: the send byte, receive byte, write byte, and read byte. All other operations result in undefined results. Repeated start is not allowed during the read bit.

Table 8-5. Send Byte

S	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	P
	7-bit AMC6821-Q1 slave address			8-bit register address		

S = start condition; P = stop condition; shaded = slave to master; unshaded = master to slave; WR = write (bit value of 0).

Table 8-6. Receive Byte

S	SLAVE ADDRESS	RD	ACK	DATA	NACK	P
	7-bit AMC6821-Q1 slave address			8-bit data from the register selected previously		

S = start condition; P = stop condition; shaded = slave to master; unshaded = master to slave; RD = read (bit value of 1); NACK = not acknowledged.

Table 8-7. Write Byte

S	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7-bit AMC6821-Q1 slave address			8-bit register address		8-bit data written to register		

S = start condition; P = stop condition; shaded = slave to master; unshaded = master to slave; WR = write (bit value of 0).

Table 8-8. Write Multiple Bytes

S	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	DATA	ACK
	7-bit AMC6821-Q1 slave address			8-bit register address of first register to be written		First 8-bit data written first register		Second 8-bit data written second register	

DATA	ACK	...	DATA	ACK	P
Third 8-bit data written third register			Last 8-bit data		

S = start condition; P = stop condition; shaded = slave to master; unshaded = master to slave; WR = write (bit value of 0).

The first register is the one to which the first data byte is written. The next register is the second register. If the bus master continues to transfer data into the AMC6821-Q1 after writing the last location, all data are ignored until the operation stops.

Table 8-9. Read Byte

S	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	Sr	SLAVE ADDRESS	RD	ACK	DATA	NACK	P
	7-bit AMC6821-Q1 slave address			8-bit register address			7-bit AMC6821-Q1 slave address			8-bit data from register		

S = start condition; P = stop condition; shaded = slave to master; unshaded = master to slave; WR = write (bit value of 0); RD = read (bit value of 1); NACK = not acknowledged; Sr = repeated start condition.

Table 8-10. Read Multiple Bytes

S	SLAVE ADDRESS	WR	ACK	COMMAND	ACK	Sr	SLAVE ADDRESS	RD	ACK	DATA	ACK
	7-bit AMC6821-Q1 slave address			Address of first register to be read			7-bit AMC6821-Q1 slave address			8-bit data from first register	

DATA	ACK	...	DATA	NACK	P
8-bit data from second register			Last 8-bit data		

S = start condition; P = stop condition; shaded = slave to master; unshaded = master to slave; WR = write (bit value of 0); RD = read (bit value of 1); NACK = not acknowledged; Sr = repeated start condition.

The first register is the one from which the first data byte is transmitted. The next register is the second register. If the bus master continues clocking data out after reading the last location (0x3F), the value *0x00* is sent out until the operation stops.

The AMC6821-Q1 is entirely controlled by the registers. All registers are 8-bit. The AMC6821-Q1 has an address pointer register; the value of the address pointer register determines the register to be written to or read from. To write data to the device register or read data from it, the address pointer register must be set properly. Data can then be written into or read from that register. The command issued by the bus master always contains the initial value of the address pointer register. The command is constructed as shown in Table 8-11.

Table 8-11. Command Format(1)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

(1) ADDR[5:0] is the address of the register that is accessed first. The register address is stored in the address pointer register.

In the send byte operation, the bus master writes the address of a specified device register into the address pointer register.

In the receive byte operation, the bus master reads the data back from the device register addressed by the address point register.

In the write byte operation, the bus master sets the address pointer register to the address of a specified device register, then writes 8-bit data into it. In the read byte operation, the SMBus master sets the address pointer register to the address of a specified device register first, then reads 8-bit data back from it.

In the write multiple bytes operation, the address pointer of the AMC6821-Q1 increments by '1' after the data are written, until it reaches the last register address (0x3F). If the host continues to transfer data into the AMC6821-Q1 after writing the last location, all data are ignored until the operation stops. When reading multiple bytes, the address pointer of the AMC6821-Q1 increments by '1' after transmitting the data until it reaches the last register address (0x3F). If the host continues clocking data out after reading the last location, the value *0x00* is sent out until the operation stops.

8.4.2 SMBus Alert Response Address (ARA)

The alert response address is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices issue simultaneous interrupts. The $\overline{\text{SMBALERT}}$ pin is an open-drain interrupt output pin. When the AMC6821-Q1 issues an interrupt request, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The bus master sends an alert response address or ARA (ARA = 0001100), and initiates a read operation (see Table 8-12).
3. The AMC6821-Q1 responds to the ARA by sending its slave address back. The 7-bit device slave address is placed in the seven most significant bits of the byte; the last bit is '0'.
4. The master receives the AMC6821-Q1 slave address and starts the interrupt service.
5. If more than one device pulls the SMBus low, the highest priority (lowest slave address) device wins the communication right via standard arbitration during the slave address transfer (refer to the SMBus specification version 2.0 for details).
6. To service the interrupt request of the AMC6821, the master must read the status register. Most interrupt source bits in the status registers are cleared after reading the status register, and are reasserted if the

error condition still exists on the next monitoring cycle. The $\overline{\text{SMBALERT}}$ only clears if the interrupt has been resolved.

Table 8-12. ARA Operation

S	ALERT RESPONSE ADDRESS	RD	ACK	DATA	NACK	P
	0001100			7-bit MSB: slave address of AMC6821-Q1 LSB = 0		

S = start condition; P = stop condition; shaded = slave to master; unshaded = master to slave; RD = read (bit value of 1); NACK = not acknowledged.

8.4.3 Power-On Reset and Start Operation

After power-on, all registers are set to the power-on default values. The device does not perform any monitoring functions until the START bit of Configuration Register 1 is set ('1'). No detections are executed until the first monitoring cycle is completed, and all measurement data registers (such as remote and local temp-data registers and the TACH data register) are updated with the new measured value. No interrupt signals are generated until the first cycle of monitoring and detection is completed. This process avoids any false alarms caused by the power-on default setting.

After power-on, the fan spin-up process is performed. At the end of spin-up, the duty cycle of the PWM driver is adjusted to 33%. (Refer to the Fan Spin-Up section for details). Device status after software reset is similar to power-on reset.

8.5 Register Map

All registers are 8-bit. Table 8-13 shows the memory map. Locations that are marked *Reserved* read back 0x0000 if they are read by the host. Writing to these locations has no effect.

Table 8-13. Memory Map

ADDR	NAME	R/W	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IDENTIFICATION REGISTERS											
0x3D	Device ID Register	R	0x21	0	0	1	0	0	0	0	1
				Device identification number. Always read '0x21'.							
0x3E	Company ID Register	R	0x49	0	1	0	0	1	0	0	1
				Company identification number.							
CONFIGURATION REGISTERS											
0x00	Configuration Register 1	R/W	0xD4	THERMOVIE	FDRC1	FDRC0	FAN-Fault-EN	PWMINV	FANIE	INT-EN	START
				THERM INT Enable	Fan Control Mode		$\overline{\text{FAN-Fault}}$ Pin EN	PWM Invert	RPM Int EN	Global Int EN	Start Monitor
0x01	Configuration Register 2	R/W	0x3D	RST	PSVIE	RTOIE	LTOIE	RTFIE	TACH-EN	TACH-MODE	PWM-EN
				Reset	LPSV Int EN	RT Int EN	LT Int EN	Remote Failure Int EN	TACH EN	TACH Mode	PWM-Out EN
0x3F	Configuration Register 3	R/W	0x82	THERM-FAN-EN	0	0	0	0	0	1	0
				THERM-Fan Control				Part Revision Number			
0x04	Configuration Register 4	R/W	0x08	For Future Use	PSPR	TACH-FAST	OVREN	1	0	0	0
				Must be rewritten to '1'.	Pulse Number	TACH Reading Fast	$\overline{\text{OVR}}$ Pin EN	Reserved			
0x02	Status Register 1	R	0x00	LTL	LTH	RTF	R-THERM	RTL	RTH	FANS	RPM-ALARM
				LT Low	LT High	RT Failure	RT Over Therm	RT Low	RT High	Fan Slow	Fan Fast
0x03	Status Register 2	R	0x00	THERM-IN	L-THERM	LPSV	LTC	RTC	0	0	0
				Therm Input	LT Over Therm	LT Below Therm	LT Over Critical	RT Over Critical	Reserved		
TEMPERATURE MONITORING											
0x06	Temp-DATA-LByte	R	0x00	LT2	LT1	LT0	0	0	RT2	RT1	RT0
				3 LSBs of Local Reading			Reserved		3 LSBs of Remote Reading		
0x0A	Local-Temp-DATA-HByte	R	0x80	LT10 (MSB)	LT9	LT8	LT7	LT6	LT5	LT4	LT3
				The 8 MSBs of newest reading of local temperature sensor. Default = –128°C.							
0x0B	Remote-Temp-DATA-HByte	R	0x80	RT10 (MSB)	RT9	RT8	RT7	RT6	RT5	RT4	RT3
				The 8 MSBs of newest reading of remote temperature sensor. Default = –128°C.							
0x14	Local-High-Temp-Limit	R/W	0x3C	LT-H10	LT-H9	LT-H8	LT-H7	LT-H6	LT-H5	LT-H4	LT-H3
				8 MSBs of upper-bound threshold of out-of-range detection of Local-Temp. 3 LSBs are '0'. Default = +60°C.							
0x15	Local-Low-Temp-Limit	R/W	0x00	LT-L10	LT-L9	LT-L8	LT-L7	LT-L6	LT-L5	LT-L4	LT-L3
				8 MSBs of lower-bound threshold of the out-of-range detection of Local-Temp. 3 LSBs are '0'. Default = 0°C.							
0x16	Local-THERM-Limit	R/W	0x46	LT-T10	LT-T9	LT-T8	LT-T7	LT-T6	LT-T5	LT-T4	LT-T3
				8 MSBs of local THERM temperature limit. 3 LSBs are '0'. When local temperature is equal to or above this limit, L-THERM is detected. Default = +70°C.							
0x18	Remote-High-Temp-Limit	R/W	0x50	RT-H10	RT-H9	RT-H8	RT-H7	RT-H6	RT-H5	RT-H4	RT-H3
				The 8 MSBs of the upper-bound threshold of the out-of-range detection of Remote-Temp. 3 LSBs are '0'. Default = +80°C.							
0x19	Remote-Low-Temp-Limit	R/W	0x00	RT-L10	RT-L9	RT-L8	RT-L7	RT-L6	RT-L5	RT-L4	RT-L3
				The 8 MSBs of the lower-bound threshold of the out-of-range detection of Remote-Temp. 3 LSBs are '0'. Default = 0°C.							
0x1A	Remote-THERM-Limit	R/W	0x64	RT-T10	RT-T9	RT-T8	RT-T7	RT-T6	RT-T5	RT-T4	RT-T3
				8 MSBs of Remote THERM temperature limit. 3 LSBs are '0'. When remote temperature is equal to or above this limit, R-THERM is detected. Default = +100°C.							
0x1B	Local-Critical-Temp	R/W	0x50	LT-C10	LT-C9	LT-C8	LT-C7	LT-C6	LT-C5	LT-C4	LT-C3
				The 8 MSBs of Local Critical temperature shutdown threshold. 3 LSBs are '0'. When the Local-Temp is equal to or above this limit, the LTC interrupt occurs and $\overline{\text{OVR}}$ goes low. Default = +80°C.							

Table 8-13. Memory Map (continued)

ADDR	NAME	R/W	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TEMPERATURE MONITORING (continued)											
0x1C	PSV-Temp	R/W	0x00	0	0	PSV8	PSV7	PSV6	PSV5	PSV4	PSV3
				Passive Cooling Temperature threshold. 3 LSBs and two MSBs are '0'. For details, refer to the passive cooling temperature limit in the Temperature Out-of-Range Detection section. Default = 0°C.							
0x1D	Remote-Critical-Temp	R/W	0x69	RT-C10	RT-C9	RT-C8	RT-C7	RT-C6	RT-C5	RT-C4	RT-C3
				The 8 MSBs of Remote Critical temperature shutdown threshold. 3 LSBs are '0'. When the Remote-Temp is equal to or above this limit, an RCRT interrupt occurs and $\overline{OVR}$ goes low. Default = +105°C.							
PWM CONTROLLER											
0x20	FAN-Characteristics	R/W	0x1D	FSPD	0	PWM2	PWM1	PWM0	STIME2	STIME1	STIME0
				Spin Dis		PWM Frequency Setting			Spin-Up Time Setting		
0x21	DCY-Low-Temp	R/W	0x55	L-DCY7	L-DCY6	L-DCY5	L-DCY4	L-DCY3	L-DCY2	L-DCY1	L-DCY0
				The duty cycle of PWM when the temperature is equal to or below Low-Temp in Auto Temp-Fan Control mode. Default = 0x55, 33.2%.							
0x22	DCY (Duty Cycle)	R/W	0x55	DCY7 (MSB)	DCY6	DCY5	DCY4	DCY3	DCY2	DCY1	DCY0
				Actual Duty cycle of PWM output. The duty cycle changes immediately after new data are written into this register. 8-bit, 0.39%/bit, range 0%-100%. Default = 33%. In read operation, the returned data are the actual DCY value driving the PWM-Out pin with two exceptions. Refer to the DCY Register section. In write operation, the data written are the actual DCY value driving the PWM-Out pin in Software-DCY control mode. In all other control modes, the data are not used to drive the PWM. Instead, they are stored in a temporary register, and used to control the PWM immediately after the control mode is changed to software-DCY control.							
0x23	DCY-RAMP	R/W	0x52	RAMPE	STEP1	STEP0	RATE2	RATE1	RATE0	THRE1	THRE0
				Ramp Enable	DCY Adjustment Step in Auto Fan Control		DCY Update Rate in Auto Temp-Fan Control			Adjustment Threshold in Auto Temp-Fan Control	
0x24	Local Temp-Fan Control(1)	R/W	0x41	L-TEMP4	L-TEMP3	L-TEMP2	L-TEMP1	L-TEMP0	L-SLP2	L-SLP1	L-SLP0
				Low-Temp in Auto Local Temp-Fan control.					Slope in Auto Local Temp-Fan control.		
0x25	Remote Temp-Fan Control	R/W	0x61	R-TEMP4	R-TEMP3	R-TEMP2	R-TEMP1	R-TEMP0	R-SLP2	R-SLP1	R-SLP0
				Low-Temp in Auto Remote Temp-Fan control.					Slope in Auto Remote Temp-Fan control.		
TACH (RPM) MEASUREMENT											
0x08	TACH-DATA-LByte	R	0x00	TACH-DATA7	TACH-DATA6	TACH-DATA5	TACH-DATA4	TACH-DATA3	TACH-DATA2	TACH-DATA1	TACH-DATA0
				Low byte of TACH measurement.							
0x09	TACH-DATA-HByte	R	0x00	TACH-DATA15	TACH-DATA14	TACH-DATA13	TACH-DATA12	TACH-DATA11	TACH-DATA10	TACH-DATA9	TACH-DATA8
				High byte of TACH measurement.							
0x10	TACH-Low-Limit-LByte	R/W	0xFF	TACH-Low-Limit7	TACH-Low-Limit6	TACH-Low-Limit5	TACH-Low-Limit4	TACH-Low-Limit3	TACH-Low-Limit2	TACH-Low-Limit1	TACH-Low-Limit0
				Low byte of TACH count limit corresponding to minimum allowed RPM. Since the TACH circuit counts between TACH pulses, a slow fan results in a larger measured value. When the measured value is larger than TACH-Low-Limit, the fan runs below the allowed minimum speed limit.							
0x11	TACH-Low-Limit-HByte	R/W	0xFF	TACH-Low-Limit15	TACH-Low-Limit14	TACH-Low-Limit13	TACH-Low-Limit12	TACH-Low-Limit11	TACH-Low-Limit10	TACH-Low-Limit9	TACH-Low-Limit8
				High byte of TACH Limit corresponding to minimum allowed RPM.							
0x12	TACH-High-Limit-LByte	R/W	0x00	TACH-High-Limit7	TACH-High-Limit6	TACH-High-Limit5	TACH-High-Limit4	TACH-High-Limit3	TACH-High-Limit2	TACH-High-Limit1	TACH-High-Limit0
				Low byte of TACH count Limit corresponding to maximum allowed RPM. Since the TACH circuit counts between TACH pulses, a fast fan results in a small measured value. When the measurement is less than this limit, the fan runs above the allowed maximum speed limit.							
0x13	TACH-High-Limit-HByte	R/W	0x00	TACH-High-Limit15	TACH-High-Limit14	TACH-High-Limit13	TACH-High-Limit12	TACH-High-Limit11	TACH-High-Limit10	TACH-High-Limit9	TACH-High-Limit8
				High byte of TACH limit corresponding to maximum allowed RPM.							
0x1E	TACH-SETTING-LByte	R/W	0xFF	TACH-SETTING7	TACH-SETTING6	TACH-SETTING5	TACH-SETTING4	TACH-SETTING3	TACH-SETTING2	TACH-SETTING1	TACH-SETTING0
				Low byte of TACH value corresponding to the predetermined target fan speed. TACH-SETTING must be not greater than the value corresponding to the RPM for 30% duty cycle when the TACH-MODE bit is cleared ('0').							
0x1F	TACH-SETTING-HByte	R/W	0xFF	TACH-SETTING15	TACH-SETTING14	TACH-SETTING13	TACH-SETTING12	TACH-SETTING11	TACH-SETTING10	TACH-SETTING9	TACH-SETTING8
				High byte of TACH value corresponding to the predetermined fan speed. TACH-SETTING must be not greater than the value corresponding to the RPM for 30% duty cycle when the TACH-MODE bit is cleared ('0').							
0x3A	Reserved	R	0x00	Always read '0'.							
0x3B	Reserved	R	0x00	Always read '0'.							

(1) Used to calculate the target PWM duty cycle for local temperature in maximum fast-speed calculated control.

8.5.1 Register Description

In this section, all interrupts are the interrupt signal through the $\overline{\text{SMBALERT}}$ pin, unless otherwise noted.

8.5.1.1 Device Configuration Registers

Table 8-14. Configuration Register 1 (Address 0x00, Value After Power-On Reset = 0xD4)

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	THERMOVIE	R/W	1	THERM interrupt enable. When this bit is set, the THERM interrupt is enabled. L-THERM = 1 or R-THERM = 1 causes an interrupt. When this bit is cleared ('0'), the THERM interrupt is disabled. When disabled, L-THERM = 1 or R-THERM = 1 does not assert the $\overline{\text{SMBALERT}}$ pin, but forces the $\overline{\text{THERM}}$ pin low. Power-on default = 1.
6	FDRC1	R/W	1	Fan driver control bit 1. Power-on default = 1. Refer to Table 8-15.
5	FDRC0	R/W	0	Fan driver control bit 0. Power-on default = 0. Refer to Table 8-15.
4	FAN-Fault-EN	R/W	1	Setting this pin to '1' enables the $\overline{\text{FAN-FAULT}}$ pin. Clearing this pin ('0') disables the $\overline{\text{FAN-FAULT}}$ pin (always in Hi-Z). Power-on default = 1.
3	PWMINV	R/W	0	PWM invert bit. When PWMINV = 0 (default), the PWM-Out pin goes low for 100% duty cycle (suitable for driving the fan using a PMOS device). Setting PWMINV to '1' makes the PWM-Out pin go high (with an external pull-up resistor) for 100% duty cycle (suitable for driving the fan using a NMOS device). Power-on default = 0.
2	FANIE	R/W	1	Fan RPM interrupt enable bit. Power-on default = 1. When FANIE = 1, the FAN-RPM interrupt is enabled. FANS = 1 or RPM-ALARM = 1 generates a FANORN interrupt, making the $\overline{\text{SMBALERT}}$ pin go low. When FANIE = 0, a FAN-RPM interrupt is disabled. Fan out-of-range = 1 does not generate an interrupt.
1	INT-EN	R/W	0	Setting this bit to '1' enables the interrupt from the $\overline{\text{SMBALERT}}$ pin. Clearing this bit ('0') disables the interrupt. Power-on default = 0.
0	START	R/W	0	Temperature monitoring and fan speed monitoring. When START = 0 , only software-DCY control mode works; software-RPM and auto temperature control modes do not work.

Table 8-15. Fan Driver Control Bits

FDRC1	FDRC0	FUNCTION
1	1	Maximum speed calculated control. The required duty cycle for remote temperature and local temperature is calculated respectively. The larger value is used to control the fan.
1	0	Auto remote-temperature-fan control. The PWM duty cycle is controlled by the remote temperature. Power-on default mode.
0	0	Software DCY control. Host writes DCY register to set the PWM duty cycle directly.
0	1	Software RPM control. Host writes the TACH setting register with the value corresponding to the desired RPM. The device measures the actual RPM and adjusts the PWM duty cycle to maintain the fan speed to the target value.

Table 8-16. Configuration Register 2 (Address 0x01, Value After Power-On Reset = 0x3D)

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	RST	R/W	0	Reset bits. RST = 1 resets the device. Self-clears after reset. Always read '0'. Power-on default = 0. Reset is immediate on rising edge of SCLK of data LSB with no acknowledge.
6	PSVIE	R/W	0	LPSV enable bit. Power-on default = 0. When LPSVIE = 1, the LPSV interrupt is enabled and an interrupt is generated when LPSV = 1. When LPSVIE = 0, LPSV is disabled and LPSV = 1 does not cause an interrupt.
5	RTOIE	R/W	1	Remote temperature interrupt enable bit. When RTIE = 1, the remote temperature interrupt is enabled and RTO = 1 causes an interrupt. When RTIE = 0, the remote temperature interrupt is disabled and RTO = 1 does not generate an interrupt. Power-on default = 1, except when a remote sensor failure is detected at power-on.
4	LTOIE	R/W	1	Local temperature interrupt enable bit. Power-on default = 1. When LTIE = 1, the local temperature interrupt is enabled and LTO = 1 causes an interrupt. When LTIE = 0, the local temperature interrupt is disabled and LTO = 1 does not generate an interrupt.
3	RTFIE	R/W	1	Remote sensor failure interrupt enable bit. Power-on default = 1. When RTFIE = 1, the remote sensor failure interrupt is enabled and RTF = 1 causes an interrupt through the $\overline{\text{SMBALERT}}$ pin. When RTFIE = 0, the remote sensor failure interrupt is disabled and RTF = 1 does not generate an interrupt through the $\overline{\text{SMBALERT}}$ pin.
2	TACH-EN	R/W	1	Setting this bit to '1' enables the TACH input. Clearing ('0') disables the TACH input and freezes the counter. Power-on default = 1. If TACH-EN is cleared, TACH-MODE must be set ('1').
1	TACH-MODE	R/W	0	When the TACH-MODE bit is cleared ('0'), the PWM-Out pin is forced *ON* during RPM measurement, and internal correction circuitry is enabled to correct the error caused by this extra duty cycle. Making TACH-MODE = 0 for the fans that are switched ON/OFF directly by the PWM requires *PWM ON* to provide TACH pulses. In the software RPM mode, the PWM-Out is forced to 30% duty cycle if the calculated duty cycle is less than 30% when TACH-MODE = 0. In all other modes the PWM-Out is forced to 0% if the calculated duty cycle is less than 7%. When the TACH mode is set ('1'), the internal correction circuit is disabled and PWM-Out is not forced *ON*. Instead, the PWM-Out pin is completely controlled by the value of the DCY register, just as in normal operation. Setting the TACH-MODE bit ('1') when the fans can provide TACH pulses output regardless the status of the PWM-Out pin. The TACH mode must be '1' for any fan which is powered directly by dc power, such as a four-wire fan. Power-on default = 0. (See the TACH-DATA Register section for details.)
0	PWM-EN	R/W	1	Setting this bit to '1' enables the PWM-Out pin. Clearing ('0') disables the PWM-Out pin (H-Z). Power-on default = 1.

Table 8-17. Configuration Register 3 (Address 0x3F, Value After Power-On Reset = 0x82)

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	THERM-FAN-EN	R/W	1	Setting this bit to '1' enables the fan to run at full-speed when the $\overline{\text{THERM}}$ pin as an output) is asserted low. This configuration allows the system to be run in performance mode. Clearing this bit to '0' disables the fan from running at full-speed whenever the $\overline{\text{THERM}}$ pin (as an output) is asserted low. This configuration allows the system to run in silent mode. Note that this bit has no effect whenever $\overline{\text{THERM}}$ is pulled low as an input. The fan always runs at full speed when the $\overline{\text{THERM}}$ pin is pulled low as an input. Power-on default = 1.
6	Reserved	R	0	Read-back '0'.
5	Reserved	R	0	Read-back '0'.
4	Reserved	R	0	Read-back '0'.
3	Part Revision Number	R	0	0, bit 3 (MSB) of 4-bit revision number.
2	Part Revision Number	R	0	0, bit 2 of revision number.
1	Part Revision Number	R	1	0, bit 1 of revision number.
0	Part Revision Number	R	0	0, bit 0 (LSB) of revision number.

Table 8-18. Configuration Register 4 (Address 0x04, Value After Power-On Reset = 0x08)

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	MODE	R/W	0	Required configure bit: User must write a 1 to this location.
6	PSPR	R/W	0	Number of pulses per revolution of the fan. Power-on default = 0. PLSPR = 0 for two pulses/revolution (default), PLSPR = 1 for four pulses per revolution.
5	TACH-FAST	R/W	0	When TACH-FAST = 1, the TACH data reading is updated every 250ms. This monitor is the fast RPM monitor. When TACH-FAST = 0, the TACH data reading is updated every second. Default = 0, power-on default = 0.
4	OVREN	R/W	0	Setting this bit to '1' enables the $\overline{\text{OVR}}$ pin. Clearing this bit ('0') disables the $\overline{\text{OVR}}$ pin (high-impedance). Default = 0.
3	Reserved	R	1	Read back '1'.
2	Reserved	R	0	Read-back '0'.
1	Reserved	R	0	Read-back '0'.
0	Reserved	R	0	Read-back '0'.

Writing the reserved bit has no effect.

8.5.1.2 Device Status Registers

Reading the status registers clears the appropriate status bit. Status register bits are sticky (except the RTF bit). Whenever a status bit is set, indicating an out-of-limit condition, it remains set until the event that caused it is resolved and the status register is read. The status bit can only be cleared by reading the status register after the event is resolved. All bits are cleared when reading the register, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle, unless otherwise noted.

Table 8-19. Status Register 1 (Address 0x02, Value After Power-On or Reset = 0x00)

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	LTL	R	0	LTL = 1 when the local temperature is less than or equal to the value of the Local-Low-Temp-Limit register. Otherwise, LTL = 0. If the local temperature is still outside the local temperature low limit, this bit reasserts on the next monitoring cycle.
6	LTH	R	0	LTH = 1 when the local temperature is greater than or equal to the value of the Local-High-Temp-Limit register. Otherwise, LTH = 0. If the local temperature is still outside the local temperature high limit, this bit reasserts on the next monitoring cycle.
5	RTF	R	0	Remote sensor-failure interrupt. RTF = 1 when the remote temperature sensor fails (short- or open-circuit). RTF = 0 when the remote sensor is in normal condition. When RTF = 1, the $\overline{\text{OVR}}$ pin is asserted and the remote temperature data register is set to –128°C. RTF = 1 also generates an interrupt through the $\overline{\text{SMBALERT}}$ pin if an interrupt is enabled (RTFIE = 1). Once RTF is set ('1'), it always remains ('1') until power-on reset or software reset occurs, whether or not the failure condition continues. Reading the status register does not clear the RTF bit.
4	R-THERM	R	0	Remote temperature over the remote THERM limit flag. R-THERM = 1 when the temperature is greater than the value of the Remote-THERM-Limit register. Otherwise, R-THERM = 0. When R-THERM = 1, the $\overline{\text{THERM}}$ pin goes low. It also generates a THERM interrupt if THERMOVIE = 1. This bit is cleared on a read of Status Register 1. Once cleared, this bit is not reasserted until the remote temperature falls 5°C below this THERM limit, even if the THERM condition persists. Refer to the THERM Pin and External Hardware Control section.
3	RTL	R	0	RTL = 1 when the remote temperature is less than or equal to the value of the Remote-Low-Temp-Limit register. Otherwise, RTL = 0. If the remote temperature is still beyond the remote temperature low limit, this bit reasserts on the next monitoring cycle.
2	RTH	R	0	RTH = 1 when the remote temperature is greater than or equal to the value of Remote-High-Temp-Limit register. Otherwise, RTH = 0. If the remote temperature is still beyond the remote temperature high limit, this bit reasserts on the next monitoring cycle.
1	FANS	R	0	Fan-slow flag. FANS = 1 if the TACH data are greater than or equal to the value of the TACH-Low-Limit register. This bit indicates if the fan becomes stuck or goes under the minimum speed. FANS = 0 if the TACH data are smaller than the TACH low limit. This bit is cleared ('0') only after reading this register, and reasserts '1' in the next monitoring if a fan-slow is detected. After spin-up, FANS is set ('1') even if the TACH data are less than the TACH low limit until the register is read. FANS = 1 generates a fan out-of-range interrupt through the $\overline{\text{SMBALERT}}$ pin if fan out-of-range is enabled (FANIE = 1). Five consecutive fan-slow events result in a *FAN FAILURE* status; which asserts the $\overline{\text{FAN-FAULT}}$ pin low. See the FAN-FAULT PIN section for details. Note that a FANS (fan-slow) detection is not performed during spin-up.
0	RPM-ALARM	R	0	RPM-ALARM = 1 when the TACH data are less than or equal to the value of the TACH-High-Limit register. This means the RPM is over the maximum limit defined by the TACH high limit. Otherwise, RPM-ALARM = 0. This bit is cleared when reading this register. Once cleared, this bit is not reasserted on the next monitoring cycle even if the condition still persists. This bit may be reasserted only if the RPM drops below the allowed maximum speed. RPM-ALARM = 1 generates a fan out-of-range interrupt through the $\overline{\text{SMBALERT}}$ pin if fan out-of-range is enabled (FANIE = 1), but does not cause an interrupt through the $\overline{\text{FAN-FAULT}}$ pin.

Table 8-20. Status Register 2 (Address 0x03, Value After Power-On or Reset = 0x00)

BIT	NAME	R/W	DEFAULT	DESCRIPTION
7	THERM-IN	R	0	Status of the $\overline{\text{THERM}}$ pin as an input. When this input is pulled low, THERM-IN = 1, and the fan is driven at full speed. This bit is cleared when reading this register and be written to '1' if the pin persists "pulled-low".
6	L-THERM	R	0	Local temperature over the local THERM limit flag. L-THERM = 1 when the local temperature is greater than the value of the Local-THERM-Limit register. Otherwise, L-THERM = 0. When L-THERM is set to 1, the $\overline{\text{THERM}}$ pin goes low. It also generates a THERM interrupt through the $\overline{\text{SMBALERT}}$ pin, if enabled (THERMOVIE = 1). This bit is cleared on a read of Status Register 1. Once cleared, this bit is not reasserted until the temperature falls 5°C below the THERM limit, even if the THERM condition persists. Refer to the THERM Pin and External Hardware Control section.
5	LPSV	R	0	Active control temperature below the PSV (passive cooling) temperature flag. This bit is set to '1' when the active control temperature is equal to or below the PSV temperature. Otherwise, this bit is cleared ('0'). LPSV = 1 generates a PSV interrupt on $\overline{\text{SMBALERT}}$, if enabled (PSVIE = 1). This bit is cleared when reading this register. If the active control temperature remains equal to or below the PSV temperature, this bit reasserts on the next monitoring cycle.
4	LTC	R	0	Local temperature over the local critical temperature flag. This bit is set ('1') when the local temperature is equal to or above the local critical temperature. LTC = 0 if the local critical temperature is below this value. LTC = 1 asserts the $\overline{\text{OVR}}$ pin low and generates an LTC interrupt (non-maskable) though the $\overline{\text{SMBALERT}}$ pin. This bit is cleared when reading this register. If the over-critical limit condition persists, this bit reasserts on the next monitoring cycle.
3	RTC	R	0	Remote temperature over the remote critical temperature flag. This bit is set to '1' when the remote temperature is equal to or above the remote critical temperature. RTC = 0 if the remote critical temperature is below this value. RTC = 1 asserts the $\overline{\text{OVR}}$ pin low and generates an RTC interrupt (non-maskable) though the $\overline{\text{SMBALERT}}$ pin. This bit is cleared when reading this register. If the over-critical limit condition persists, this bit reasserts on next monitoring cycle.
2	Reserved	R	0	Reserved. Reading returns '0'.
1	Reserved	R	0	Reserved. Reading returns '0'.
0	Reserved	R	0	Reserved. Reading returns '0'.

8.5.1.3 Fan Controller Registers

Table 8-21. DCY (Duty Cycle) Register (Address 0x22, Value After Power-On or Reset = 0x55)

BIT	NAME	DEFAULT	DESCRIPTION		
7 (MSB)	DCY7 (MSB)	0		**DCY CODE**	**DUTY CYCLE**
6	DCY6	1		0x00	0%
5	DCY5	0		0x01	0.392%
4	DCY4	1		... ...	... ...
3	DCY3	0		0x40	25%
2	DCY2	1		... ...	... ...
1	DCY1	0		0x80	50%
0	DCY0	1		... ...	... ...
				0xFF	100%

The DCY register stores the value of the PWM duty cycle, 0x00 corresponds to 0%, and 0xFF to 100%. 1LSB corresponds to 0.392%. Power-on default = 0x55, 33.2%.

In a read operation, with the two following exceptions, the returned data are the actual duty cycle (DCY) value driving the PWM-Out pin:

1. When TACH-MODE = 0 and the system is in software-RPM control mode, if the calculated duty cycle is less than 30%, the returned value is the calculated value, not the actual PWM-OUT pin duty cycle which is forced to 30%.

2. When TACH-MODE = 0 and the system is in software DCY-control mode or Auto Temperature-Fan mode, if the calculated duty cycle is less than 7%, the returned value is the calculated value, not the actual PWM-OUT pin duty cycle which is forced to 0%.

In a write operation, the data written are the actual DCY driving the PWM-Out pin in the software DCY control mode. However, in all other control modes, the data being written are not used to drive the PWM. Instead, it is stored in a temporary register, and controls the PWM immediately after the control mode is changed to the software DCY control mode.

Table 8-22. Fan Characteristics Register (Address 0x20, Value After Power-On or Reset = 0x1D)

BIT	NAME	DEFAULT	DESCRIPTION			
7	FSPD	0	Fan Spin Disable Bit When FSPD = 1, the fan spin-up process is disabled. When FSPD = 0, the fan spin-up process is enabled.			
6	0	0	Reserved			
5	PWM2	0	PWM Frequency Bits			
4	PWM1	1	**PWM2**	**PWM1**	**PWM0**	**PWM Frequency**
3	PWM0	1	When PWM-MODE pin is floating or tied to V_{DD}			
			0	0	0	10Hz
			0	0	1	15Hz
			0	1	0	23Hz
			0	1	1	30Hz (Default)
			1	0	0	38Hz
			1	0	1	47Hz
			1	1	0	62Hz
			1	1	1	94Hz
			When PWM-MODE pin is tied to GND			
			0	0	0	1kHz
			0	0	1	10kHz
			0	1	0	20kHz
			0	1	1	25kHz (Default)
			1	0	0	30kHz
			1	0	1	40kHz
			1	1	0	40kHz
			1	1	1	40kHz
2	STIME2	1	Spin-Up Time Bit			
1	STIME1	0	**STIME2**	**STIME1**	**STIME0**	**Spin-Up Time (in Seconds)**
0	STIME0	1	0	0	0	0.2
			0	0	1	0.4
			0	1	0	0.6
			0	1	1	0.8
			1	0	0	1
			1	0	1	2 (Default)
			1	1	0	4
			1	1	1	8

This register specifies the PWM frequency and the fan spin-up functions.

Fan Spin Disable Bit: FSPD

This bit enables or disables the spin-up function.

PWM Frequency Bits: [PWM2:PWM0]

These bits specify the PWM frequency; the high range (1kHz–40kHz) has a default value of 25kHz, and the low range (10Hz–94Hz) has a default value of 30Hz. The clock frequency is 3.2MHz. The PWM-MODE pin determines which range is selected. When the PWM mode is tied to ground, the high range is selected; otherwise, the low range is selected.

Spin-Up Time Bits: [STIME2:STIME0]

These bits specify a predetermined time period, or spin-up time, during which the 100% duty cycle is applied to start the fan spinning. These bits are ignored when FSPD = 1.

Table 8-23. DCY-Low-Temp Register (Address 0x21, Value After Power-On or Reset = 0x55, 33.2%)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
L-DCY 7	L-DCY 6	L-DCY 5	L-DCY 4	L-DCY 3	L-DCY 2	L-DCY 1	L-DCY 0

This register specifies the duty cycle in Auto Temp-Fan Control mode when the control temperature is less than or equal to the value of the Low-Temp bits in the TEMP-FAN Control Register.

Table 8-24. Local Temp-Fan Control Register (Address 0x24, Value After Power-On or Reset = 0x41)

BIT	NAME	DEFAULT	DESCRIPTION					
7	L-TEMP4	0	Low Temperature Bit of Local Sensor					
6	L-TEMP3	1	**L-TEMP4**	**L-TEMP3**	**L-TEMP2**	**L-TEMP1**	**L-TEMP0**	**Low Temp**
5	L-TEMP2	0	0	0	0	0	0	0°C
4	L-TEMP1	0	0	0	0	0	1	4°C
3	L-TEMP0	0	0	0	0	1	0	8°C
			0	0	0	1	1	12°C
			...	...	...	...	...	...
			0	1	0	0	0	32°C (Default)
			...	...	...	...	...	...
			1	1	1	1	0	120°C
			1	1	1	1	1	124°C
2	L-SLP2	0	Slope Bits of Local Sensor					
1	L-SLP1	0				**Slope**		**Temp Range in °C (DCY 33.3% to 100%)**
0	L-SLP0	1	**L-SLP2**	**L-SLP1**	**L-SLP0**	**LSB/°C**	**%/°C**	
			0	0	0	32	12.55	5.31
			0	0	1	16	6.27	10.62 (default)
			0	1	0	8	3.14	21.25
			0	1	1	4	1.57	42.5
			1	0	0	2	0.78	85

This register specifies the parameters of the local Temperature-Fan Control mode.

Low Temperature Bits: [L-TEMP4:L-TEMP0]

These bits specify the low temperature of the local temperature fan control loop. The calculated duty cycle is equal to the value of the DCY-LOW-TEMP register when the local temperature is less than or equal to the value defined by bits [L-TEMP4:L-TEMP0]. Refer to the Auto Temperature Fan Mode section for details.

Slope Bits: [L-SLP2:L-SLP0]

These bits define the increment of the duty cycle when the local temperature rises every 1°C in the auto local temperature-fan control.

Table 8-25. Remote Temp-Fan Control Register (Address 0x25, Value After Power-On or Reset = 0x61)

BIT	NAME	DEFAULT	DESCRIPTION					
7	R-TEMP4	0	Low Temperature Bit of Remote Sensor					
6	R-TEMP3	1	**R-TEMP4**	**R-TEMP3**	**R-TEMP2**	**R-TEMP1**	**R-TEMP0**	**Low Temp**
5	R-TEMP2	1	0	0	0	0	0	0°C
4	R-TEMP1	0	0	0	0	0	1	4°C
3	R-TEMP0	0	0	0	0	1	0	8°C
			0	0	0	1	1	12°C
			...	...	...	...	...	...
			0	1	1	0	0	48°C (Default)
			...	...	...	...	...	...
			1	1	1	1	0	120°C
			1	1	1	1	1	124°C
2	R-SLP2	0	Slope Bits of Remote Sensor					
1	R-SLP1	0				**Slope**		**Temp Range in °C (DCY 33.3% to 100%)**
0	R-SLP0	1	**R-SLP2**	**R-SLP1**	**R-SLP0**	**LSB/°C**	**%/°C**	
			0	0	0	32	12.55	5.31
			0	0	1	16	6.27	10.62 (default)
			0	1	0	8	3.14	21.25
			0	1	1	4	1.57	42.5
			1	0	0	2	0.78	85

This register specifies the parameters of the Remote Temperature-Fan Control mode.

Low Temperature Bits: [R-TEMP 4:R-TEMP0]

These bits specify the low temperature of the auto remote temperature-fan control. In this control mode, the duty cycle is equal to the value of the DCY-LOW-TEMP register when the remote temperature is less than or equal to the value defined by bits [R-TEMP4:R-TEMP0].

Slope Bits: [R-SLP2:R-SLP0]

These bits define the increment of the duty cycle when the remote temperature rises every 1°C in the auto remote temperature-fan control.

Table 8-26. DCY-Ramp Register (Address 0x23, Value After Power-On or Reset = 0x52)

BIT	NAME	DEFAULT	DESCRIPTION
7	RAMPE	0	Ramp Enable Bit. Ignored in software-RPM control. When RAMPE = 1, Ramp is enabled. The DCY changes to the desired value gradually according to STEP bits and RATE bits. When RAMPE = 0, Ramp is disabled. DCY changes to the desired target value immediately. Default = 0.
6	STEP1	1	Adjustment Step Bits.
5	STEP0	0	**STEP1** / **STEP0** / **Max Adjustment** 0 / 0 / 1/256 0 / 1 / 2/256 1 / 0 / 4/256 (Default) 1 / 1 / 8/256
4	RATE2	1	DCY Updating Rate Bits in Auto Temp-Fan Control Mode.
3	RATE1	0	**RATE2** / **RATE1** / **RATE0** / **DCY Updates/Sec (Auto Temp-Fan CTR)** 0 / 0 / 0 / 0.0625 0 / 0 / 1 / 0.125 0 / 1 / 0 / 0.25 0 / 1 / 1 / 0.5 1 / 0 / 0 / 1 (Default) 1 / 0 / 1 / 2 1 / 1 / 0 / 4 1 / 1 / 1 / 8
2	RATE0	0	
1	THRE1	1	Adjustment Threshold Bits in Auto Temp-Fan Control Mode.
0	THRE0	0	**THRE1** / **THRE0** / **Threshold** 0 / 0 / 1/256 0 / 1 / 2/256 1 / 0 / 3/256 (Default) 1 / 1 / 4/256

This register is ignored in the software DCY control mode. This register determines how fast the PWM duty cycle is adjusted to the desired value when the temperature changes in the automatic temperature-fan control, or when the fan speed varies from the predetermined value in the software RPM control mode.

RAMPE: Ramp Enable bit.

This bit is ignored in the software RPM control mode. The duty cycle always gradually ramps to the target value in Software-RPM mode.

Adjustment Step Bits: [STEP1:STEP0]

In the software RPM control, these bits specify the amount that duty cycle changes each time.

In the auto fan temperature control mode, these bits are ignored when RAMPE = 0. When RAMPE = 1, these bits define the maximum amount that the duty cycle can change each time if the duty cycle needs to be adjusted. For example, if the current value of the duty cycle is 50% and the desired value is 75%, the total required increment is 25%. If the step is 1/256 (bits [STEP1:STEP0] = '00'), then the duty cycle increases by 1/256 (0.39%) each time the duty cycle is updated, and the duty cycle reaches the desired value (75%) after 64 updates. This takes eight seconds if the update rate is 8/sec (bits [RATE2:RATE0] = '111'), and takes 64 seconds if the update rate is 1/sec. (bits [RATE2:RATE0] = '100'). However, if the step is 2/256, then the time reduces to half. If the required adjustment is less than the value specified by step bits, the actual required value is used. For example, if the current duty cycle is 50%, the required value is 73%, and the step is 4/256, a total of 15

updates are needed. The duty cycle increases 21.875% after the first 14 updates, and increases 1.125% in the last update.

Updating Rate Bits: [RATE2:RATE0]

These bits define the rate (time/sec) that the duty cycle is recalculated in the auto temp-fan control mode. The value of [RATE2:RATE0] does not affect the ADC conversion rate. Both external and local temperature readings are updated continuously, even if the DCY is updated slowly.

The RPM monitoring rate and DCY updating rate in the software RPM control mode are specified by the TACH-FAST bit of Configuration Register 3. The [RATE2:RATE0] bits are ignored in this mode.

Adjustment Threshold Bits: [THRE1:THRE0]

These bits determine the threshold of the duty cycle adjustment in the auto temp-fan control mode, and are ignored in all other modes. When the auto fan temperature control loop is active, the duty cycle is not adjusted if the required adjustment is less than or equal to the threshold defined by bits [THRE1:THRE0]. This provides a hysteresis to improve the control stability. For example, if the current duty cycle is 50% and the desired value is 71%, the total required increment is 21%. If the step is 4/256 and the threshold is 2/256 (0.78%), the duty cycle reaches 70.31% after 13 updates, 0.6875% less than the desired value. This difference is less than the threshold (0.78%); therefore, the adjustment stops. However, if the threshold is 1/256 (0.39%), then one more update occurs, and the duty cycle increases by 0.39% (1LSB) because 0.39% (1LSB) < 0.6875% < 0.78% (2LSB). Finally, the duty cycle reaches 70.7%, 0.3% less than the desired value because of the limitation of 8-bit resolution.

Note that bits [THRE1:THRE0] are ignored in the software RPM control. In this mode, the DCY adjustment stops when the difference between the TACH data and TACH setting is less than or equal to 0x000A.

8.5.1.4 Temperature Data Registers

Local Temperature Data Register Bits: [LT10:LT0]

Bits [LT10:LT0] are the newest local temperature reading.

Remote Temperature Register Bits: [RT10:RT0]

Bits [RT10:RT0] are the newest remote temperature reading.

Table 8-27. Temp-Data-LByte Register (Address 0x06, Value After Power-On or Reset = 0x00)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
LT2	LT1	LT0 (LSB)	0	0	RT2	RT1	RT0

Bits [LT2:LT0] are the three LSBs of the newest local temperature reading.

Bits [RT2:RT0] are the three LSBs of the newest remote temperature reading.

Table 8-28. Local-Temp-Data-HByte Register (Address 0x0A, Value After Power-On or Reset = 0x80, –128°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
LT10 (MSB)	LT9	LT8	LT7	LT6	LT5	LT4	LT3

Bits [LT10:LT3] are the eight MSBs of the newest local temperature reading.

Table 8-29. Remote-Temp-Data-HByte Register (Address 0x0B, Value After Power-On or Reset = 0x80, –128°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RT10 (MSB)	RT9	RT8	RT7	RT6	RT5	RT4	RT3

Bits [RT10:RT3] are the eight MSBs of the newest remote temperature reading.

It is important to note that temperature can be read as an 8-bit value (with 1°C resolution) from the Temp-DATA-Hbyte register, or as an 11-bit value (with 0.125°C resolution) from the Temp-DATA-LByte and Temp-DATA-

HByte registers. If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order. If the 11-bit measurement is required, this involves a two-register read for each measurement. The Temp-DATA-LByte register (0x06) should be read first. This condition causes all temperature reading registers to be frozen until the Remote-Temp-DATA-HByte Register (0x0B) is read. This architecture also prevents an MSB reading from being updated while the 3LSBs are being read, and vice versa. See the Reading Temperature Data section for details.

8.5.1.5 Temperature Limit Registers

All temperature limits are 11 bits with three LSBs always '0'. Only eight MSBs need to be set in one register for each limit.

Table 8-30. Local-High-Temp-Limit Register (Address 0x14, Value After Power-On or Reset = 0x3C, +60°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
LT-H10 (MSB)	LT-H9	LT-H8	LT-H7	LT-H6	LT-H5	LT-H4	LT-H3

These bits are the upper bounds of the local temperature.

Table 8-31. Local-Low-Temp-Limit Register (Address 0x15, Value After Power-On or Reset = 0x00, 0°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
LT-L10 (MSB)	LT-L9	LT-L8	LT-L7	LT-L6	LT-L5	LT-L4	LT-L3

These bits are the lower bounds of the local temperature.

Table 8-32. Local-Therm-Limit Register (Address 0x16, Value After Power-On or Reset = 0x46, +70°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
LT-T10 (MSB)	LT-T9	LT-T8	LT-T7	LT-T6	LT-T5	LT-T4	LT-T3

These bits are the thermal threshold of the local temperature.

Table 8-33. Remote-High-Temp-Limit Register (Address 0x18, Value After Power-On or Reset = 0x50, +80°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RT-H10 (MSB)	RT-H9	RT-H8	RT-H7	RT-H6	RT-H5	RT-H4	RT-H3

These bits are the upper bounds of the remote temperature.

Table 8-34. Remote-Low-Temp-Limit Register (Address 0x19, Value After Power-On or Reset = 0x00, 0°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RT-L10 (MSB)	RT-L9	RT-L8	RT-L7	RT-L6	RT-L5	RT-L4	RT-L3

These bits are the lower bounds of the remote temperature.

Table 8-35. Remote-Therm-Limit Register (Address 0x1A, Value After Power-On or Reset = 0x64, +100°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RT-T10 (MSB)	RT-T9	RT-T8	RT-T7	RT-T6	RT-T5	RT-T4	RT-T3

These bits are the thermal threshold of the remote temperature.

Table 8-36. Local-Critical-Temp Register (Address 0x1B, Value After Power-On or Reset = 0x50, +80°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
LT-C10	LT-C9	LT-C8	LT-C7	LT-C6	LT-C5	LT-C4	LT-C3

These bits are the critical threshold of the local temperature.

Table 8-37. PSV-Temp Register (Address 0x1C, Value After Power-On or Reset = 0x00, 0°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	0	PSV8	PSV7	PSV6	PSV5	PSV4	PSV3

Bits [PSV10:PSV0] are the passive cooling temperature threshold. Bits PSV10, PSV9, and [PSV2:PSV0] are always '0'. The PSV ranges from 0°C to +64°C.

In the auto fan temperature loop, the fan stops and the duty cycle is forced to 0% when the active temperature is equal to or below the PSV temperature.

Table 8-38. Remote-Critical-Temp Register (Address 0x1D, Value After Power-On or Reset = 0x69, +105°C)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
RT-C10	RT-C9	RT-C8	RT-C7	RT-C6	RT-C5	RT-C4	RT-C3

Bits [RT-C10:RT-C0] are the critical threshold of the remote temperature.

8.5.1.5.1 Tach-Data Register

Table 8-39. Tach-Data-LByte Register (Address 0x08, Power-On Default = 0x00)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-DATA7	TACH-DATA6	TACH-DATA5	TACH-DATA4	TACH-DATA3	TACH-DATA2	TACH-DATA1	TACH-DATA0

Table 8-40. Tach-Data-HByte Register (Address 0x09, Power-On Default = 0x00)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-DATA15	TACH-DATA14	TACH-DATA13	TACH-DATA12	TACH-DATA11	TACH-DATA10	TACH-DATA9	TACH-DATA8

Bits [TACH-DATA15:TACH-DATA0] are the number of clock pulses counted during one fan revolution and represents the period of the fan revolution (refer to the Fan Speed Measurement section). Reading the TACH data register involves a two-register read. The low byte should be read first. This method causes the high byte to be frozen until both the high and low byte registers have been read from, preventing erroneous TACH readings.

8.5.1.5.2 Tach Setting Register

Table 8-41. Tach-Setting-LByte Register (Address 0x1E, Power-On Default = 0xFF)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-SETTING7	TACH-SETTING6	TACH-SETTING5	TACH-SETTING4	TACH-SETTING3	TACH-SETTING2	TACH-SETTING1	TACH-SETTING0

Table 8-42. Tach-Setting-HByte Register (Address 0x1F, Power-On Default = 0xFF)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-SETTING15	TACH-SETTING14	TACH-SETTING13	TACH-SETTING12	TACH-SETTING11	TACH-SETTING10	TACH-SETTING9	TACH-SETTING8

Bits [TACH-SETTING15:TACH-SETTING0] represent the period of the fan revolution (in the number of clock pulses counted during one revolution), which is equal to the reciprocal of the target fan speed. Refer to the Fan Speed Measurement section. Software writes this register to set the target RPM in the Software-RPM Control mode. When the TACH-MODE bit (bit 1, 0x02) is cleared ('0'), the TACH setting must be not greater than the value corresponding to the RPM for a 30% duty cycle. When the TACH mode is equal to '1', the TACH setting must be not greater than the value corresponding to the allowed minimum RPM at which the fan properly runs.

8.5.1.5.3 Tach Low Limit Register

Table 8-43. Tach-Low-Limit-LByte Register (Address 0x10, Power-On Default = 0xFF)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-Low-Limit7	TACH-Low-Limit6	TACH-Low-Limit5	TACH-Low-Limit4	TACH-Low-Limit3	TACH-Low-Limit2	TACH-Low-Limit1	TACH-Low-Limit0

Table 8-44. Tach-Low-Limit-HByte Register (Address 0x11, Power-On Default = 0xFF)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-Low-Limit15	TACH-Low-Limit14	TACH-Low-Limit13	TACH-Low-Limit12	TACH-Low-Limit11	TACH-Low-Limit10	TACH-Low-Limit9	TACH-Low-Limit8

Bits [TACH-Low-Limit15:TACH-Low-Limit0] are the value that corresponds to the predetermined minimum allowable fan speed (RPM). If the value of the TACH data register is greater than this bound, the fan speed is below the minimum allowed RPM.

8.5.1.5.4 Tach High Limit Register

Table 8-45. Tach-High-Limit-LByte Register (Address 0x12, Power-On Default = 0x00)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-High-Limit7	TACH-High-Limit6	TACH-High-Limit5	TACH-High-Limit4	TACH-High-Limit3	TACH-High-Limit2	TACH-High-Limit1	TACH-High-Limit0

Table 8-46. Tach-High-Limit-HByte Register (Address 0x13, Power-On Default = 0x00)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
TACH-High-Limit15	TACH-High-Limit14	TACH-High-Limit13	TACH-High-Limit12	TACH-High-Limit11	TACH-High-Limit10	TACH-High-Limit9	TACH-High-Limit8

Bits [TACH-High-Limit15:TACH-High-Limit0] are the value that corresponds to the predetermined maximum allowable fan speed (RPM). If the value of the TACH data register is smaller than this bound, the fan speed is above the maximum allowed RPM.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Power Supply Recommendations

The AMC6821-Q1 device operates with power supply in the range of 3 V to 5 V. The device is optimized for operation at 5-V supply but can operate in the full supply range.

A power-supply bypass capacitor is required for proper operation. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC6821SQDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	C6821Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF AMC6821-Q1 :

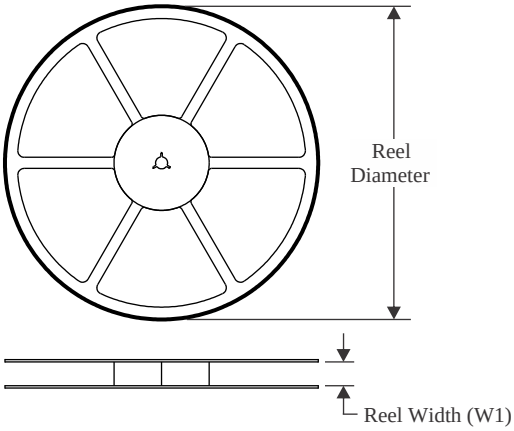
- Catalog : AMC6821

NOTE: Qualified Version Definitions:

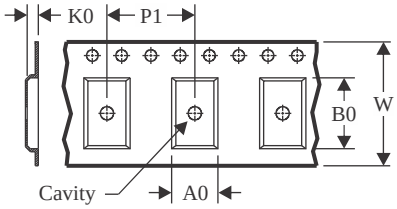
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

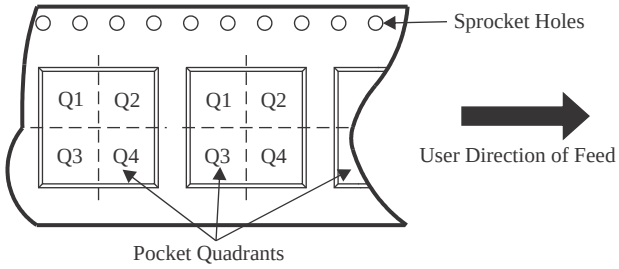


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

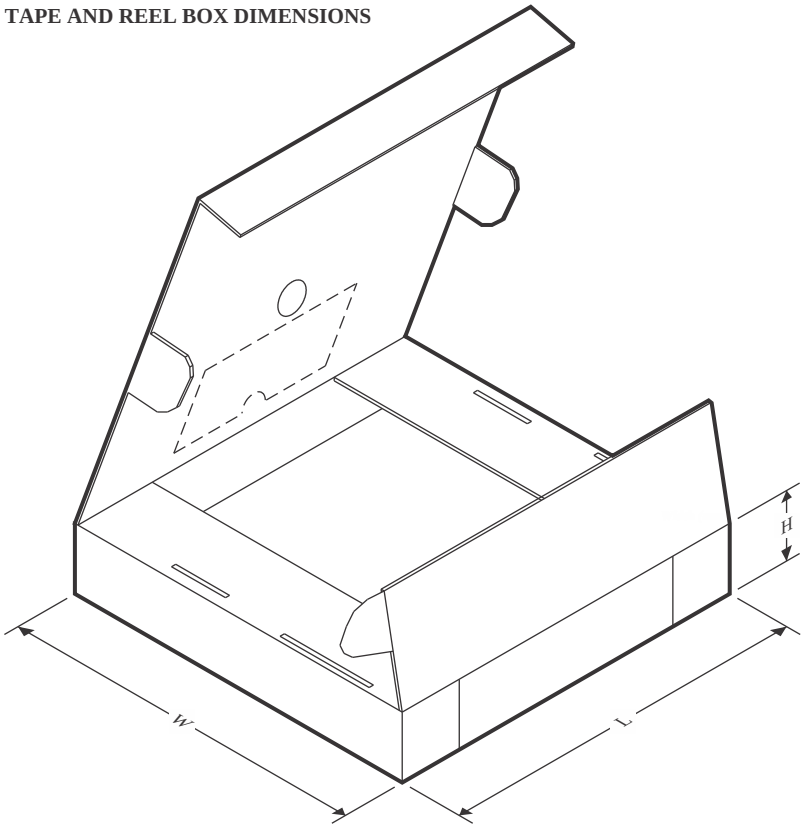
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

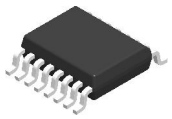
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC6821SQDBQRQ1	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC6821SQDBQRQ1	SSOP	DBQ	16	2500	350.0	350.0	43.0

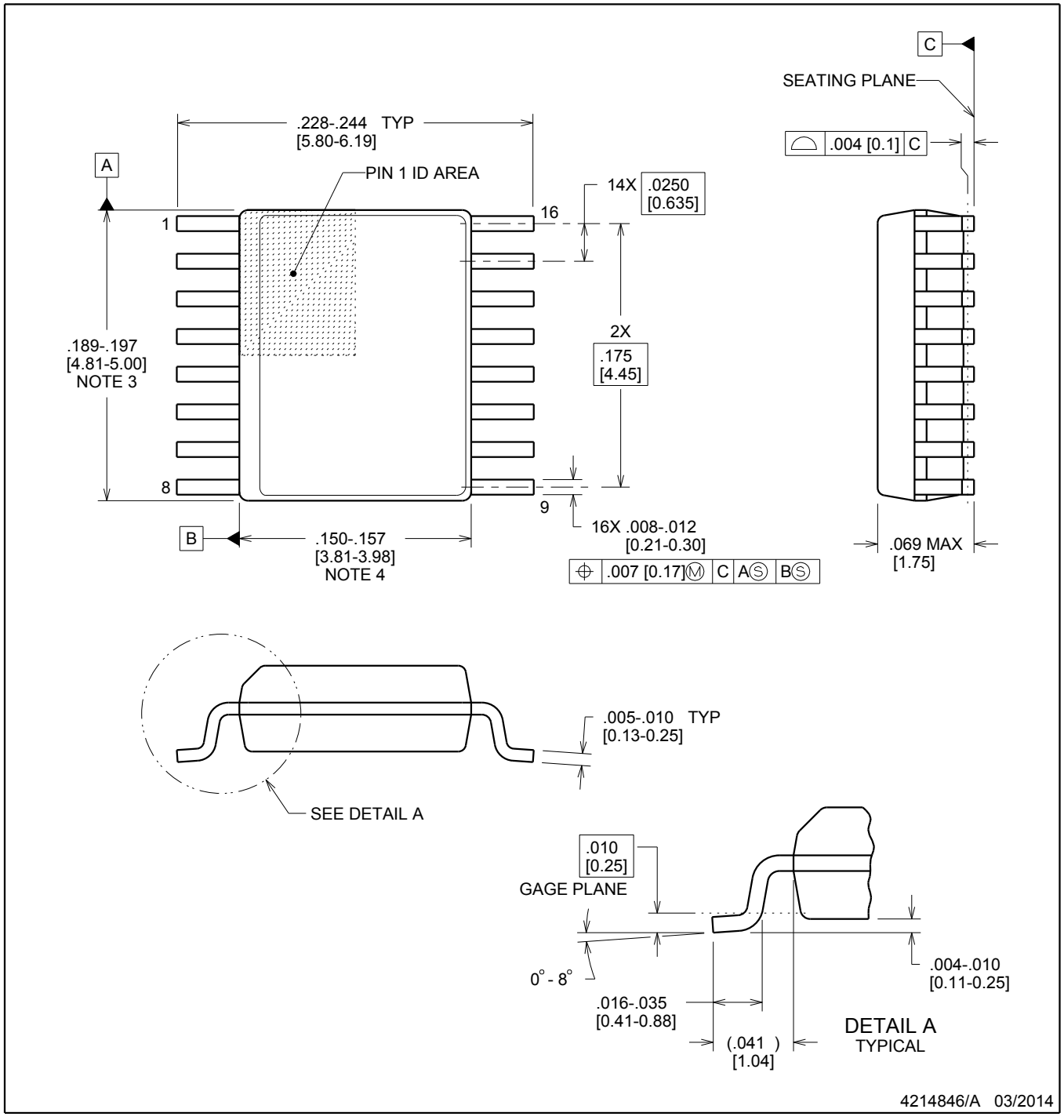


PACKAGE OUTLINE

DBQ0016A

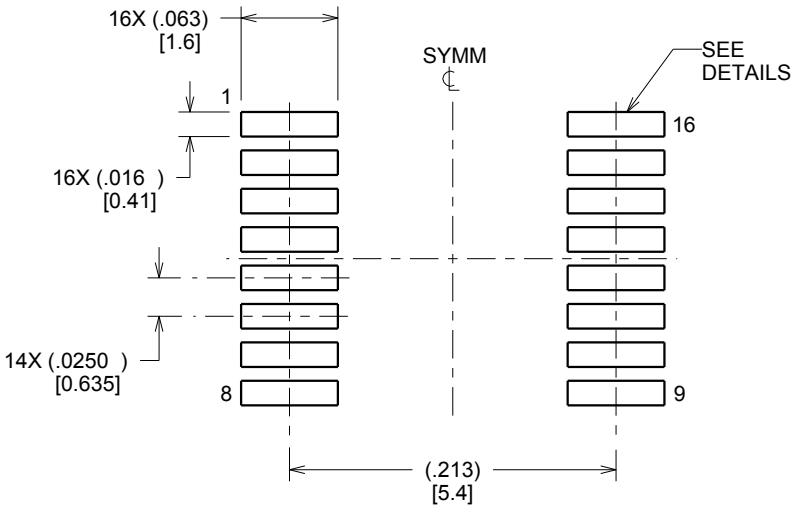
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

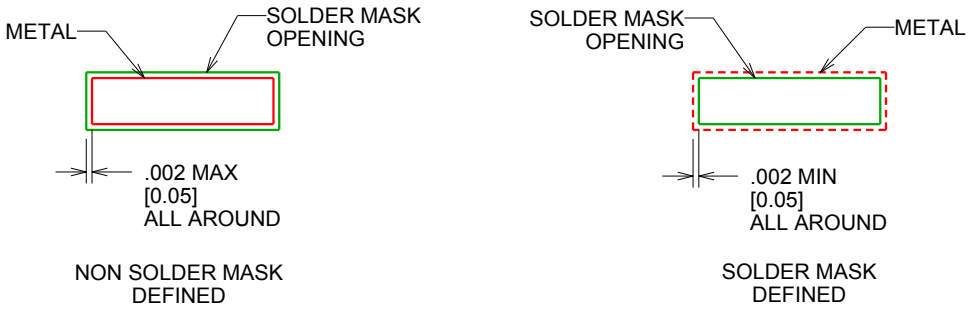


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

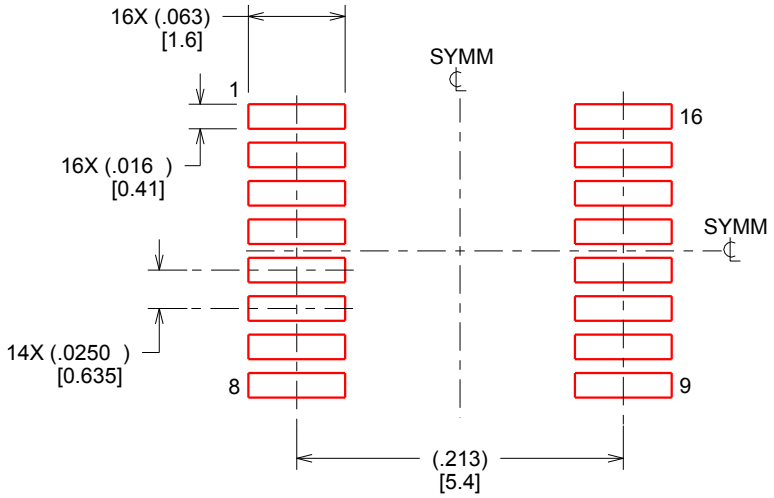
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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