bq27546-G1 Single-Cell Li-Ion Battery Fuel Gauge for Battery Pack Integration

1 Features

- Battery Fuel Gauge for 1-Series (1sXp) Li-Ion Applications up to 14,500-mAh Capacity
- Microcontroller Peripheral Provides:
  - Internal or External Temperature Sensor for Battery Temperature Reporting
  - SHA-1/HMAC Authentication
  - Lifetime Data Logging
  - 64 Bytes of Non-Volatile Scratch Pad FLASH
- Battery Fuel Gauging Based on Patented Impedance Track™ Technology
  - Models Battery Discharge Curve for Accurate Time-To-Empty Predictions
  - Automatically Adjusts for Battery Aging, Battery Self-Discharge, and Temperature/Rate Inefficiencies
  - Low-Value Sense Resistor (5 mΩ to 20 mΩ)
- Advanced Fuel Gauging Features
  - Internal Short Detection
  - Tab Disconnection Detection
- HDQ and I²C™ Interface Formats for Communication with Host System
- Small 15-Ball Nano-Free™ (DSBGA) Packaging

2 Applications

- Smartphones
- Tablets
- Digital Still and Video Cameras
- Handheld Terminals
- MP3 or Multimedia Players

3 Description

The bq27546-G1 Li-Ion battery fuel gauge is a microcontroller peripheral that provides fuel gauging for single-cell Li-Ion battery packs. The device requires minimal system microcontroller firmware development for accurate battery fuel gauging. The bq27546-G1 resides within the battery pack or on the system's main-board with an embedded battery (non-removable).

The bq27546-G1 uses the patented Impedance Track™ algorithm for fuel gauging, and provides information such as remaining battery capacity (mAh), state-of-charge (%), run-time to empty (min.), battery voltage (mV), and temperature (°C). It also provides detections for internal short or tab disconnection events.

The bq27546-G1 features integrated support for secure battery pack authentication, using the SHA-1/HMAC authentication algorithm.

The device comes in a 15-ball Nano-Free™ DSBGA package (2.61 mm × 1.96 mm) that is ideal for space-constrained applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq27546-G1	YZF (15)	2.61 mm × 1.96 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

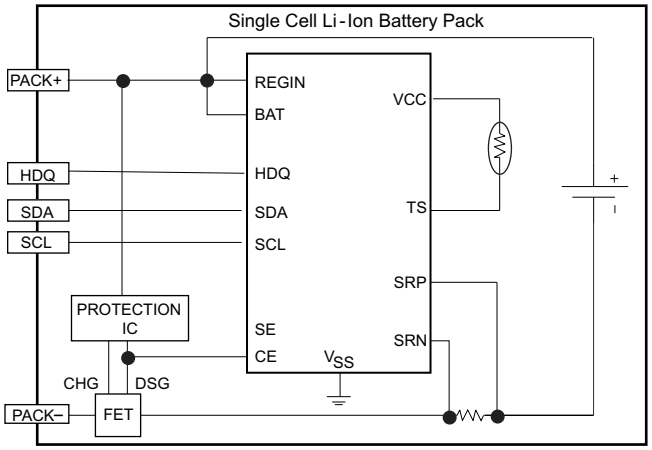


Table of Contents

4 Revision History

Changes from Revision A (December 2015) to Revision B **Page**

- Changed *Simplified Schematic* ... 1
- Changed the description for the SRP pin ... 3

Changes from Original (May 2015) to Revision A **Page**

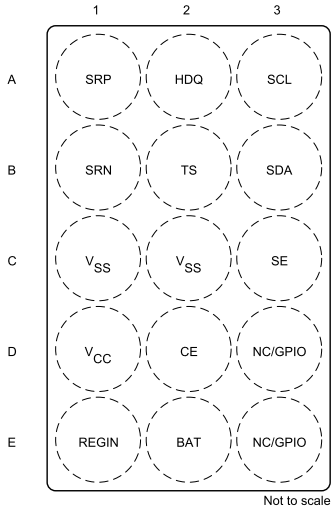
- Changed the descriptions for the SRP and SRN pins ... 3
- Changed Pin Configuration and Functions ... 3
- Changed *Power-On Reset* ... 5
- Added "FULLSLEEP mode" to the introduction in *Power Modes* ... 15

5 Device Comparison Table

PART NUMBER(1)	FIRMWARE VERSION	PACKAGE(1)	T_A	COMMUNICATION FORMAT	TAPE AND REEL QUANTITY
BQ27546YZFR-G1	2.00	DSBGA-15	–40°C to 85°C	I^2C, HDQ(1)	3000
BQ27546YZFT-G1					250

(1) bq27546-G1 is shipped in I^2C mode.

6 Pin Configuration and Functions



Pin Functions

NUMBER	NAME	TYPE	DESCRIPTION
A1	SRP	IA(1)	Analog input pin connected to the internal coulomb counter where SRP is nearest the CELL– connection. Connect to a 5-mΩ to 20-mΩ sense resistor.
B1	SRN	IA	Analog input pin connected to the internal coulomb counter where SRN is nearest the PACK– connection. Connect to a 5-mΩ to 20-mΩ sense resistor.
C1, C2	V_{SS}	P	Device ground
C3	SE	O	Shutdown Enable output. Push-pull output
D1	V_{CC}	P	Regulator output and processor power. Decouple with a 1.0-µF ceramic capacitor to V_{SS}.
E1	REGIN	P	Regulator input. Decouple with a 0.1-µF ceramic capacitor to V_{SS}.
A2	HDQ	I/O	HDQ serial communications line (Slave). Open-drain
B2	TS	IA	Pack thermistor voltage sense (use 103AT-type thermistor). ADC input
D2	CE	I	Chip Enable. Internal LDO is disconnected from REGIN when driven low.
E2	BAT	IA	Cell-voltage measurement input. ADC input. Recommendation is 4.8 V maximum for conversion accuracy.
A3	SCL	I	Slave I^2C serial communications clock input line for communication with system (Master). Use with a 10-kΩ pull-up resistor (typical).
B3	SDA	I/O	Slave I^2C serial communications data line for communication with system (Master). Open-drain I/O. Use with a 10-kΩ pull-up resistor (typical).
D3, E3	NC/GPIO	NC	Do not connect for proper operation. Reserved for future GPIO.

(1) IA = Analog input, I/O = Digital input/output, P = Power connection, NC = No connect

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Regulator input, REGIN	–0.3	5.5	V
V_{CC}	Supply voltage range	–0.3	2.75	V
V_{IOD}	Open-drain I/O pins (SDA, SCL, HDQ)	–0.3	5.5	V
V_{BAT}	BAT input (pin E2)	–0.3	5.5	V
V_I	Input voltage range to all others (pins GPIO, SRP, SRN, TS)	–0.3	V_{CC} + 0.3	V
T_A	Operating free-air temperature range	–40	85	°C
T_F	Functional temperature range	–40	100	°C
T_{stg}	Storage temperature range	–65	150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic Discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001(1), BAT pin	1500	V
		Human Body Model (HBM), all pins	2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

T_A = –40°C to 85°C; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage, REGIN	No operating restrictions	2.8		4.5	V
		No FLASH writes	2.45		2.8	
C_{REGIN}	External input capacitor for internal LDO between REGIN and V_{SS}	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1		µF
C_{LDO25}	External output capacitor for internal LDO between V_{CC} an V_{SS}		0.47	1		µF
t_{PUCD}	Power-up communication delay			250		ms

7.4 Thermal Information

THERMAL METRIC(1)		bq27546-G1 YZF (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	17	
$R_{\theta JB}$	Junction-to-board thermal resistance	20	
ψ_{JT}	Junction-to-top characterization parameter	1	
ψ_{JB}	Junction-to-board characterization parameter	18	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report (SPRA953).

7.5 Supply Current

T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	NORMAL operating mode current (1)	Fuel gauge in NORMAL mode. I_{LOAD} > ***Sleep Current***		118		µA
$I_{(SLP)}$	Low-power operating mode current(1)	Fuel gauge in SLEEP mode. I_{LOAD} < ***Sleep Current***		62		µA
$I_{(FULLSLP)}$	Low-power operating mode current(1)	Fuel gauge in FULLSLEEP mode. I_{LOAD} < ***Sleep Current***		23		µA
$I_{(HIB)}$	HIBERNATE operating mode current (1)	Fuel gauge in HIBERNATE mode. I_{LOAD} < ***Hibernate Current***		8		µA

(1) Specified by design. Not tested in production.

7.6 Digital Input and Output DC Characteristics

T_A = –40°C to 85°C; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output voltage low (HDQ, SDA, SCL, SE)	I_{OL} = 3 mA			0.4	V
$V_{OH(PP)}$	Output high voltage (SE)	I_{OH} = –1 mA	V_{CC}–0.5			V
$V_{OH(OD)}$	Output high voltage (HDQ, SDA, SCL)	External pullup resistor connected to V_{CC}	V_{CC}–0.5			V
V_{IL}	Input voltage low (HDQ, SDA, SCL)		–0.3		0.6	V
V_{IH}	Input voltage high (HDQ, SDA, SCL)		1.2		5.5	V
$V_{IL(CE)}$	CE Low-level input voltage	V_{REGIN} = 2.8 to 4.5 V	2.65		0.8	V
$V_{IH(CE)}$	CE High-level input voltage		V_{REGIN}–0.5		0.8	
I_{lkg}	Input leakage current (I/O pins)				0.3	µA

7.7 Power-On Reset

T_A = –40°C to 85°C, $C_{(REG)}$ = 0.47 µF, 2.45 V < $V_{(REGIN)}$ = V_{BAT} < 5.5 V; typical values at T_A = 25°C and $V_{(REGIN)}$ = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going battery voltage input at V_{CC}		2.05	2.15	2.20	V
V_{HYS}	Power-on reset hysteresis			115		mV

7.8 2.5-V LDO Regulator

T_A = –40°C to 85°C, $C_{(REG)}$ = 0.47 µF, 2.45 V < $V_{(REGIN)}$ = V_{BAT} < 5.5 V; typical values at T_A = 25°C and $V_{(REGIN)}$ = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{REG25}	Regulator output voltage, REG25	2.8 V ≤ $V_{(REGIN)}$ ≤ 4.5 V, I_{OUT} ≤ 16 mA	2.3	2.5	2.6	V
		2.45 V ≤ $V_{(REGIN)}$ < 2.8 V (low battery), I_{OUT} ≤ 3 mA	2.3			V

7.9 Internal Clock Oscillators

T_A = –40°C to 85°C, 2.4 V < V_{CC} < 2.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency			2.097		MHz
$f_{(LOSC)}$	Operating frequency			32.768		kHz

7.10 Integrating ADC (Coulomb Counter) Characteristics

T_A = –40°C to 85°C, $C_{(REG)}$ = 0.47 µF, 2.45 V < $V_{(REGIN)}$ = V_{BAT} < 5.5 V; typical values at T_A = 25°C and $V_{(REGIN)}$ = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR}	Input voltage range, $V_{(SRN)}$ and $V_{(SRP)}$	V_{SR} = $V_{(SRN)}$ – $V_{(SRP)}$	–0.125		0.125	V
$t_{CONV(SR)}$	Conversion time	Single conversion		1		s
	Resolution		14		15	bits
$V_{OS(SR)}$	Input offset			10		µV
INL	Integral nonlinearity error			±0.007	±0.034	FSR
$Z_{IN(SR)}$	Effective input resistance(1)		2.5			MΩ
$I_{lkg(SR)}$	Input leakage current(1)				0.3	µA

(1) Specified by design. Not production tested.

7.11 ADC (Temperature and Cell Voltage) Characteristics

T_A = –40°C to 85°C, $C_{(REG)}$ = 0.47 µF, 2.45 V < $V_{(REGIN)}$ = V_{BAT} < 5.5 V; typical values at T_A = 25°C and $V_{(REGIN)}$ = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(TS)}$	Input voltage range (TS)		V_{SS} – 0.125		V_{CC}	V
$V_{IN(BAT)}$	Input voltage range (BAT)		V_{SS} – 0.125		5	V
$V_{IN(ADC)}$	Input voltage range to ADC		0.05		1	V
$G_{(TEMP)}$	Temperature sensor voltage gain			–2.0		mV/°C
$t_{CONV(ADC)}$	Conversion time				125	ms
	Resolution		14		15	bits
$V_{OS(ADC)}$	Input offset			1		mV
$Z_{(TS)}$	Effective input resistance (TS)(1)	bq27546-G1 not measuring external temperature	8			MΩ
$Z_{(BAT)}$	Effective input resistance (BAT)(1)	bq27546-G1 not measuring cell voltage	8			MΩ
		bq27546-G1 measuring cell voltage		100		kΩ
$I_{lkg(ADC)}$	Input leakage current				0.3	µA

(1) Specified by design. Not production tested.

7.12 Data Flash Memory Characteristics

T_A = –40°C to 85°C, $C_{(REG)}$ = 0.47 µF, 2.45 V < $V_{(REGIN)}$ = V_{BAT} < 5.5 V; typical values at T_A = 25°C and $V_{(REGIN)}$ = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention(1)		10			Years
	Flash programming write-cycles(1)		20,000			Cycles
$t_{WORDPROG}$	Word programming time(1)				2	ms
I_{CCPROG}	Flash-write supply current(1)			5	10	mA
$t_{DFERASE}$	Data flash master erase time(1)		200			ms
$t_{PGERASE}$	Flash page erase time(1)		20			ms

(1) Specified by design. Not production tested.

7.13 HDQ Communication Timing Characteristics

T_A = –40°C to 85°C, C_{REG} = 0.47 µF, 2.45 V < V_{REGIN} = V_{BAT} < 5.5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(CYCH)}$	Cycle time, host to bq27546-G1		190			µs
$t_{(CYCD)}$	Cycle time, bq27546-G1 to host		190	205	250	µs
$t_{(HW1)}$	Host sends 1 to bq27546-G1		0.5		50	µs

HDQ Communication Timing Characteristics (continued)

T_A = –40°C to 85°C, C_{REG} = 0.47 µF, 2.45 V < V_{REGIN} = V_{BAT} < 5.5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(DW1)}$	bq27546-G1 sends 1 to host		32		50	µs
$t_{(HW0)}$	Host sends 0 to bq27546-G1		86		145	µs
$t_{(DW0)}$	bq27546-G1 sends 0 to host		80		145	µs
$t_{(RSPS)}$	Response time, bq27546-G1 to host		190		950	µs
$t_{(B)}$	Break time		190			µs
$t_{(BR)}$	Break recovery time		40			µs
$t_{(RISE)}$	HDQ line rising time to logic 1 (1.2 V)				950	ns

7.14 I²C-Compatible Interface Timing Characteristics

T_A = –40°C to 85°C, C_{REG} = 0.47 µF, 2.45 V < V_{REGIN} = V_{BAT} < 5.5 V; typical values at T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_r	SCL/SDA rise time				300	ns
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse width (high)		600			ns
$t_{w(L)}$	SCL pulse width (low)		1.3			µs
$t_{su(STA)}$	Setup for repeated start		600			ns
$t_{d(STA)}$	Start to first falling edge of SCL		600			ns
$t_{su(DAT)}$	Data setup time		1000			ns
$t_{h(DAT)}$	Data hold time		0			ns
$t_{su(STOP)}$	Setup time for stop		600			ns
t_{BUF}	Bus free time between stop and start		66			µs
f_{SCL}	Clock frequency (1)				400	kHz

(1) If the clock frequency (f_{SCL}) is > 100 kHz, use 1-byte write commands for proper operation. All other transactions types are supported at 400 kHz. (Refer to I²C Interface.)

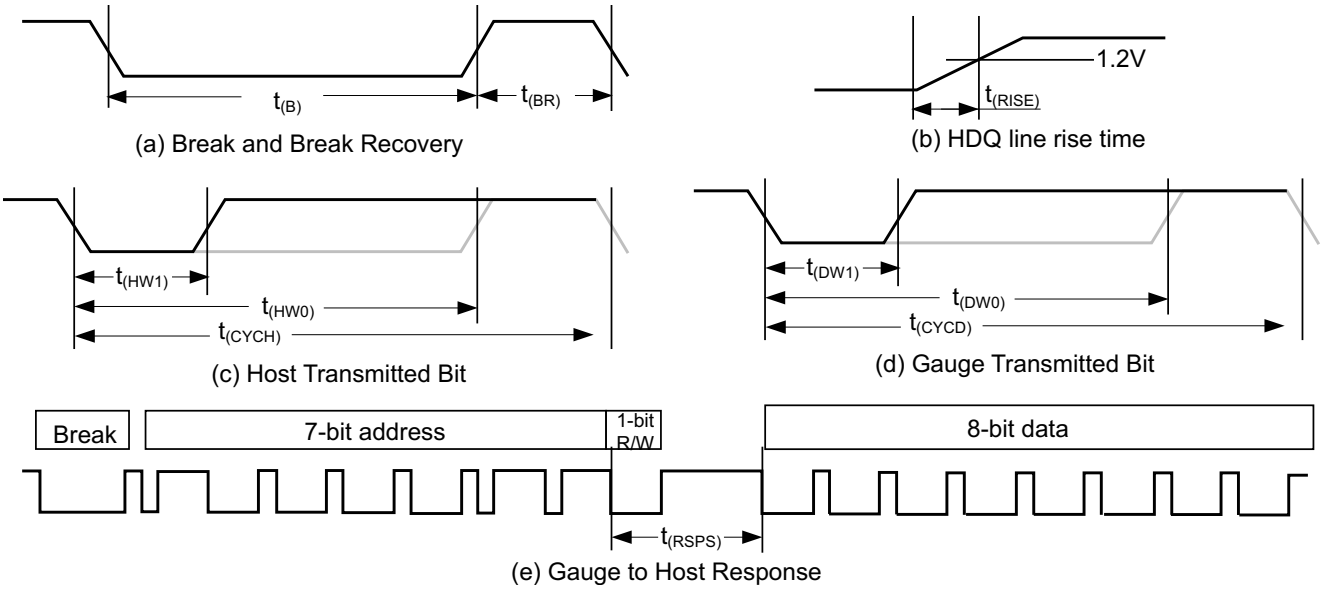


Figure 1. HDQ Timing Diagrams

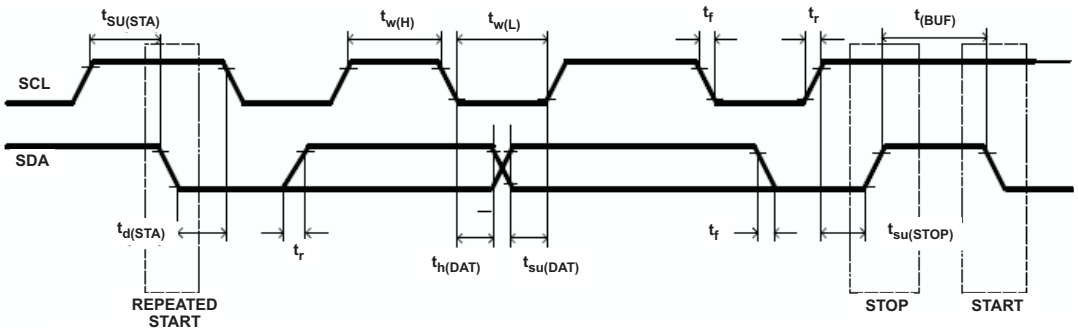


Figure 2. I²C-Compatible Interface Timing Diagrams

7.15 Typical Characteristics

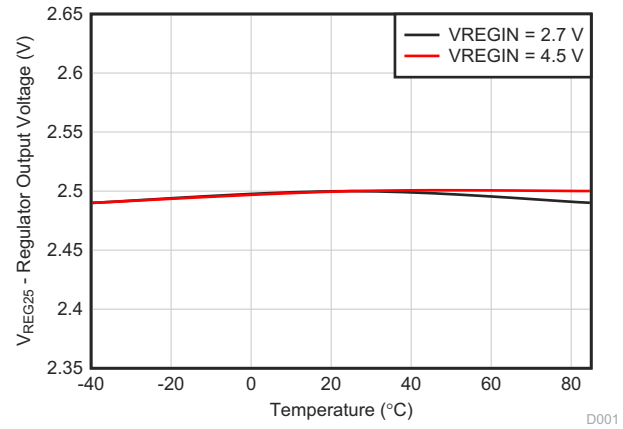


Figure 3. Regulator Output Voltage Vs. Temperature

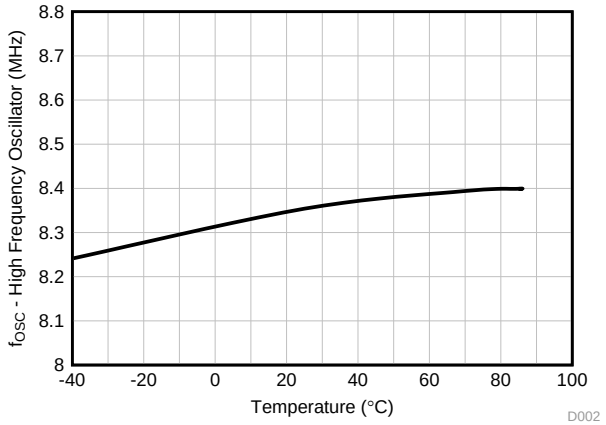


Figure 4. High-Frequency Oscillator Frequency Vs. Temperature

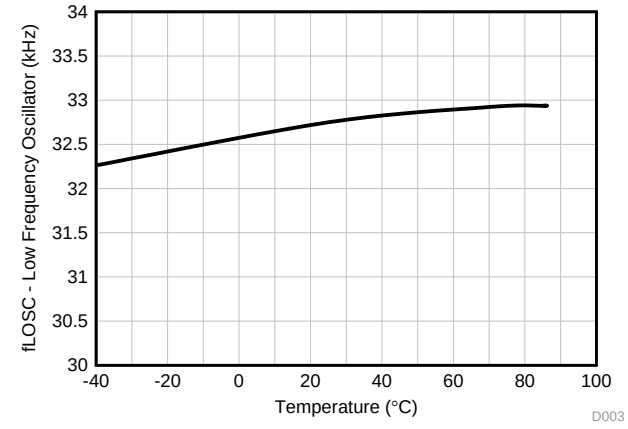


Figure 5. Low-Frequency Oscillator Frequency Vs. Temperature

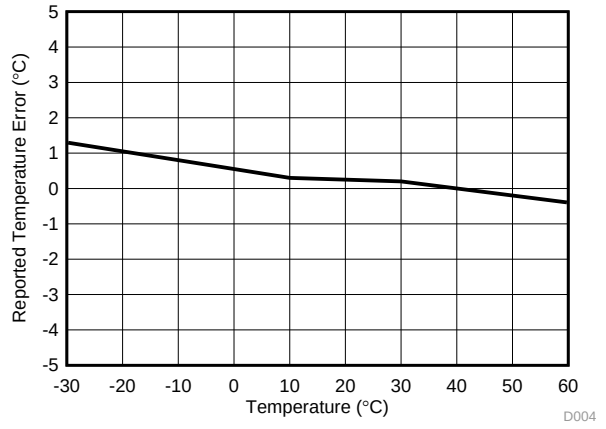


Figure 6. Reported Internal Temperature Measurement Vs. Temperature

8 Detailed Description

8.1 Overview

The bq27546-G1 accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as state-of-charge (SOC) and time-to-empty (TTE).

Information is accessed through a series of commands, called Standard Commands. Further capabilities are provided by the additional Extended Commands set. Both sets of commands, indicated by the general format *Command()*, are used to read and write information contained within the bq27546-G1 control and status registers, as well as its data flash locations. Commands are sent from the system to gauge using the bq27546-G1 serial communications engine, and can be executed during application development, pack manufacture, or end-equipment operation.

Cell information is stored in the bq27546-G1 in non-volatile flash memory. Many of these data flash locations are accessible during application development. They cannot, generally, be accessed directly during end-equipment operation. To access to these locations, use the bq27546-G1 companion evaluation software, individual commands, or a sequence of data-flash-access commands. To access a desired data flash location, the correct data flash Subclass and offset must be known. For detailed data flash information, see the *bq27546-G1 Technical Reference Manual* (SLUUB74).

The bq27546-G1 provides 64 bytes of user-programmable data flash memory, partitioned into two (2) 32-byte blocks: ***Manufacturer Info Block A*** and ***Manufacturer Info Block B***. This data space is accessed through a data flash interface. For specifics on accessing the data flash, see section Manufacturer Information Blocks in the *bq27546-G1 Technical Reference Manual* (SLUUB74).

The key to the bq27546-G1 high-accuracy gas gauging prediction is the Texas Instruments proprietary Impedance Track™ algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve less than 1% error across a wide variety of operating conditions and over the lifetime of the battery.

The bq27546-G1 measures charge/discharge activity by monitoring the voltage across a small-value series sense resistor (5 mΩ to 20 mΩ typ.) located between the CELL– and the battery's PACK– terminal. When a cell is attached to the bq27546-G1, cell impedance is learned based on cell current, cell open-circuit voltage (OCV), and cell voltage under loading conditions.

The bq27546-G1 external temperature sensing is optimized with the use of a high accuracy negative temperature coefficient (NTC) thermistor with R25 = 10 kΩ ± 1% and B25/85 = 3435K ± 1% (such as Semitec 103AT) for measurement. The bq27546-G1 can also be configured to use its internal temperature sensor. The bq27546-G1 uses temperature to monitor the battery-pack environment, which is used for fuel gauging and cell protection functionality.

To minimize power consumption, the bq27546-G1 has different power modes: NORMAL, SLEEP, FULLSLEEP, and HIBERNATE. The bq27546-G1 passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly. More details can be found in *Power Modes*.

NOTE

FORMATTING CONVENTIONS IN THIS DOCUMENT:

Commands: *italics* with *parentheses()* and no breaking spaces. e.g. *RemainingCapacity()*

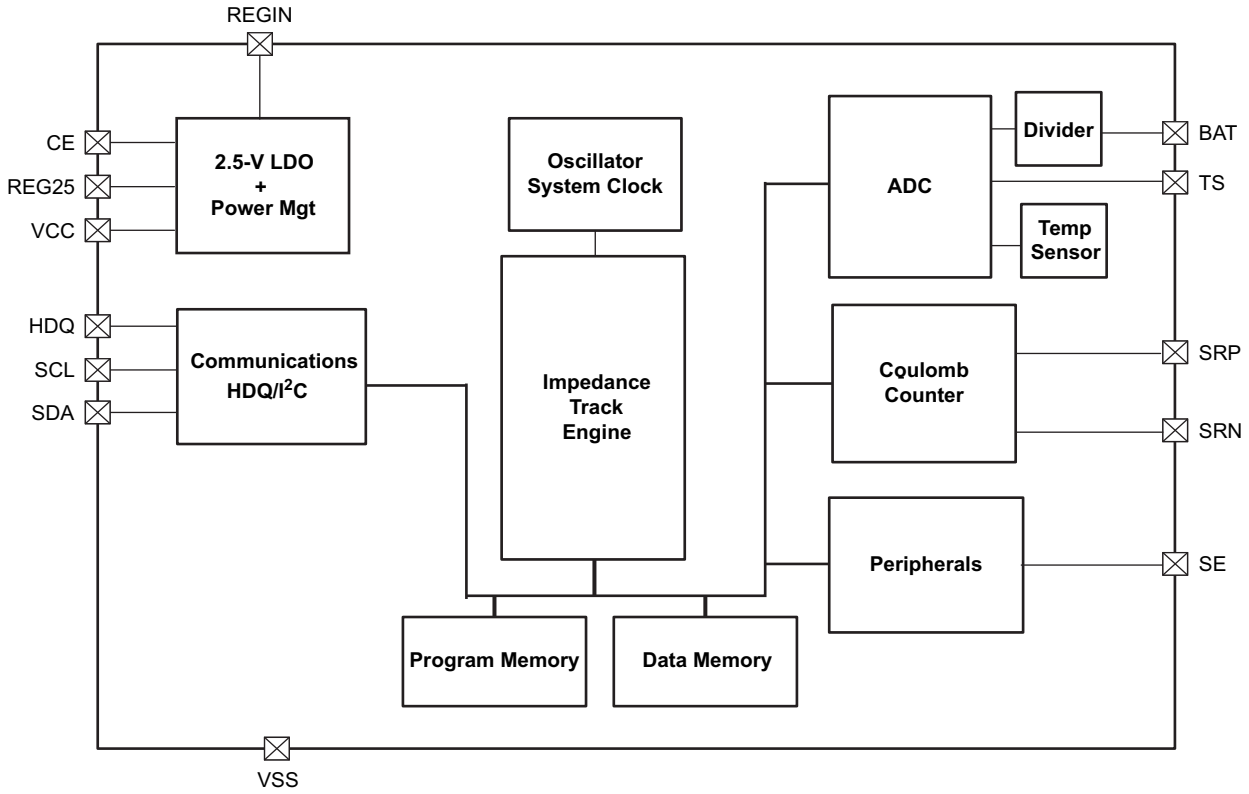
Data Flash: *italics*, **bold**, and *breaking spaces.* e.g. ***Design Capacity***

Register bits and flags: italics with brackets[ ]. *e.g. [TDA]*

Data flash bits: *italics*, **bold**, and brackets[ ]. e.g. ***[LED1]***

Modes and states: ALL CAPITALS. e.g. UNSEALED mode

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fuel Gauging

The bq27546-G1 fuel gauge measures the cell voltage, temperature, and current to determine battery SOC based on the Impedance Track algorithm. (For more information, refer to the *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm Application Report* [SLUA450].) The device monitors charge and discharge activity by sensing the voltage across a small-value resistor (5-mΩ to 20-mΩ typical) between the SRP and SRN pins and in series with the cell. By integrating the charge passing through the battery, the battery SOC is adjusted during battery charge or discharge.

The total battery capacity is found by comparing states of charge before and after applying the load with the amount of charge passed. When an application load is applied, the impedance of the cell is measured by comparing the OCV obtained from a predefined function for present SOC with the measured voltage under load. Measurements of OCV and charge integration determine chemical state of charge and chemical capacity (Qmax). The initial Qmax values are taken from a cell manufacturer's data sheet multiplied by the number of parallel cells. It is also used for the value in ***Design Capacity***. The fuel gauge acquires and updates the battery-impedance profile during normal battery usage. It uses this profile, along with SOC and the Qmax value, to determine *FullChargeCapacity()* and *StateOfCharge()*, specifically for the present load and temperature. *FullChargeCapacity()* is reported as capacity available from a fully charged battery under the present load and temperature until *Voltage()* reaches the ***Terminate Voltage***. *NominalAvailableCapacity()* and *FullAvailableCapacity()* are the uncompensated (no or light load) versions of *RemainingCapacity()* and *FullChargeCapacity()*, respectively.

8.3.2 Impedance Track Variables

The bq27546-G1 fuel gauge has several data flash variables that permit the user to customize the Impedance Track algorithm for optimized performance. These variables depend on the power characteristics of the application, as well as the cell itself.

Feature Description (continued)

8.3.3 Power Control

8.3.3.1 Reset Functions

When the bq27546-G1 detects a software reset by sending *[RESET] Control()* subcommand, it determines the type of reset and increments the corresponding counter. This information is accessible by issuing the command *Control()* function with the RESET_DATA subcommand.

8.3.3.2 Wake-Up Comparator

The wake-up comparator is used to indicate a change in cell current while the bq27546-G1 is in SLEEP mode. ***Pack Configuration*** uses bits ***[RSNS1–RSNS0]*** to set the sense resistor selection. ***Pack Configuration*** also uses the ***[IWAKE]*** bit to select one of two possible voltage threshold ranges for the given sense resistor selection. An internal interrupt is generated when the threshold is breached in either charge or discharge directions. Setting both ***[RSNS1]*** and ***[RSNS0]*** to 0 disables this feature.

Table 1. I_{WAKE} Threshold Settings(1)

IWAKE	RSNS1	RSNS0	Vth(SRP-SRN)
0	0	0	Disabled
1	0	0	Disabled
0	0	1	+1.0 mV or –1.0 mV
1	0	1	+2.2 mV or –2.2 mV
0	1	0	+2.2 mV or –2.2 mV
1	1	0	+4.6 mV or –4.6 mV
0	1	1	+4.6 mV or –4.6 mV
1	1	1	+9.8 mV or –9.8 mV

(1) The actual resistance value vs. the sense resistor setting is not important; however, the actual voltage threshold when calculating the configuration is important. The voltage thresholds are typical values under room temperature.

8.3.3.3 Flash Updates

Data flash can only be updated if *Voltage()* ≥ ***Flash Update OK Voltage***. Flash programming current can cause an increase in LDO dropout. The value of ***Flash Update OK Voltage*** should be selected such that the bq27546-G1 V_{CC} voltage does not fall below its minimum of 2.4 V during flash write operations.

8.3.4 Autocalibration

The bq27546-G1 device provides an autocalibration feature that measures the voltage offset error across SRP and SRN from time-to-time as operating conditions change. It subtracts the resulting offset error from normal sense resistor voltage, V_{SR}, for maximum measurement accuracy.

Autocalibration of the ADC begins on entry to SLEEP mode, except if *Temperature()* is ≤ 5°C or *Temperature()* ≥ 45°C.

The fuel gauge also performs a single offset calibration when (1) the condition of *AverageCurrent()* ≤ 100 mA and (2) {voltage change since the last offset calibration ≥ 256 mV} or {temperature change since last offset calibration is greater than 8°C for ≥ 60 seconds}.

Capacity and current measurements will continue at the last measured rate during the offset calibration when these measurements cannot be performed. If the battery voltage drops more than 32 mV during the offset calibration, the load current has likely increased considerably; therefore, the offset calibration will be stopped.

8.3.5 Communications

8.3.5.1 Authentication

The bq27546-G1 device can act as a SHA-1/HMAC authentication slave by using its internal engine. Sending a 160-bit SHA-1 challenge message to the bq27546-G1 fuel gauge causes the gauge to return a 160-bit digest, based upon the challenge message and a hidden, 128-bit plain-text authentication key. If this digest matches an identical one generated by a host or dedicated authentication master, and when operating on the same challenge message and using the same plain text keys, the authentication process is successful.

8.3.5.2 Key Programming (Data Flash Key)

By default, the bq27546-G1 contains a default plain-text authentication key of 0x0123456789ABCDEFFEDCBA9876543210. This default key is intended for development purposes. It should be changed to a secret key and the part should be immediately sealed before putting a pack into operation. Once written, a new plain-text key cannot be read again from the fuel gauge while in SEALED mode.

Once the bq27546-G1 is UNSEALED, the authentication key can be changed from its default value by writing to the *Authenticate()* Extended Data Command locations. A 0x00 is written to *BlockDataControl()* to enable the authentication data commands. The *DataFlashClass()* is issued 112 (0x70) to set the Security class. Up to 32 bytes of data can be read directly from the *BlockData()* (0x40...0x5F) and the authentication key is located at 0x48 (0x40 + 0x08 offset) to 0x57 (0x40 + 0x17 offset). The new authentication key can be written to the corresponding locations (0x48 to 0x57) using the *BlockData()* command. The data is transferred to the data flash when the correct checksum for the whole block (0x40 to 0x5F) is written to *BlockDataChecksum()* (0x60). The checksum is (255 – x) where x is the 8-bit summation of the *BlockData()* (0x40 to 0x5F) on a byte-by-byte basis. Once the authentication key is written, the gauge can then be sealed again.

8.3.5.3 Key Programming (Secure Memory Key)

The bq27546-G1 secure-memory authentication key is stored in the secure memory of the bq27546-G1 device. If a secure-memory key has been established, only this key can be used for authentication challenges (the programmable data flash key is not available). The selected key can only be established/programmed by special arrangements with TI, using TI's *Secure B-to-B Protocol*. The secure-memory key can never be changed or read from the bq27546-G1 fuel gauge.

8.3.5.4 Executing an Authentication Query

To execute an authentication query in UNSEALED mode, a host must first write 0x01 to the *BlockDataControl()* command to enable the authentication data commands. If in SEALED mode, 0x00 must be written to *DataFlashBlock()* instead.

Next, the host writes a 20-byte authentication challenge to the *Authenticate()* address locations (0x40 through 0x53). After a valid checksum for the challenge is written to *AuthenticateChecksum()*, the bq27546-G1 uses the challenge to perform the SHA-1/HMAC computation in conjunction with the programmed key. The bq27546-G1 completes the SHA-1/HMAC computation and writes the resulting digest to *Authenticate()*, overwriting the pre-existing challenge. The host should wait at least 45 ms to read the resulting digest. The host may then read this response and compare it against the result created by its own parallel computation.

8.3.5.5 HDQ Single-Pin Serial Interface

The HDQ interface is an asynchronous return-to-one protocol where a processor sends the command code to the bq27546-G1 device. With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first. Note that the DATA signal on pin 12 is open-drain and requires an external pull-up resistor. The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0–6) and the 1-bit R/W field (MSB bit 7). The R/W field directs the bq27546-G1 either to

- Store the next 8 or 16 bits of data to a specified register or
- Output 8 bits of data from the specified register.

The HDQ peripheral can transmit and receive data as either an HDQ master or slave.

HDQ serial communication is normally initiated by the host processor sending a break command to the bq27546-G1 device. A break is detected when the DATA pin is driven to a logic-low state for a time $t_{(B)}$ or greater. The DATA pin should then be returned to its normal ready high logic state for a time $t_{(BR)}$. The bq27546-G1 fuel gauge is now ready to receive information from the host processor.

The bq27546-G1 device is shipped in I^2C mode. TI provides tools to enable the HDQ peripheral. The *HDQ Communication Basics Application Report* (SLUA408A) provides details of HDQ communication.

8.3.5.6 HDQ Host Interruption Feature

The default bq27546-G1 gauge behaves as an HDQ slave-only device when HDQ mode is enabled. If the HDQ interrupt function is enabled, the bq27546-G1 is capable of mastering and also communicating to an HDQ device. There is no mechanism for negotiating what is to function as the HDQ master and care must be taken to avoid message collisions. The interrupt is signaled to the host processor with the bq27546-G1 mastering an HDQ *message*. This message is a fixed message that will be used to signal the interrupt condition. The message itself is 0x80 (slave write to register 0x00) with no data byte being sent as the command, and is not intended to convey any status of the interrupt condition. The HDQ interrupt function is disabled by default and needs to be enabled by command.

When the SET_HDQINTEN subcommand is received, the bq27546-G1 device detects any of the interrupt conditions and asserts the interrupt at 1-s intervals until the CLEAR_HDQINTEN command is received or the count of ***HDQHostIntrTries*** has lapsed.

The number of tries for interrupting the host is determined by the data flash parameter named ***HDQHostIntrTries***.

8.3.5.6.1 Low Battery Capacity

This feature works identically to SOC1. It uses the same data flash entries as SOC1 and triggers interrupts as long as SOC1 = 1 and ***HDQIntEN*** = 1.

8.3.5.6.2 Temperature

This feature triggers an interrupt based on the OTC (Overtemperature in Charge) or OTD (Overtemperature in Discharge) condition being met. It uses the same data flash entries as OTC or OTD and triggers interrupts as long as either the OTD or OTC condition is met and *HDQIntEN* = 1.

8.3.5.7 I^2C Interface

The fuel gauge supports the standard I^2C read, incremental read, one-byte write quick read, and functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for a write or read, respectively.

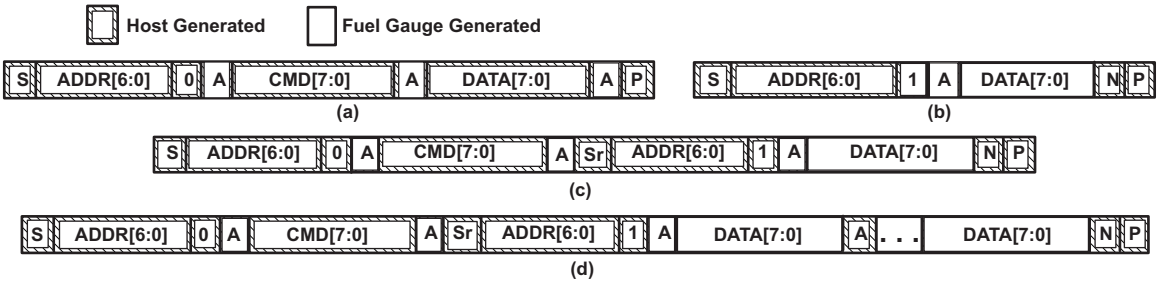


Figure 7. Supported I^2C formats: (a) 1-byte write, (b) quick read, (c) 1 byte-read, and (d) incremental read (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The *quick read* returns data at the address indicated by the address pointer. The address pointer, a register internal to the I^2C communication engine, increments whenever data is acknowledged by the bq27546-G1 or the I^2C master. *Quick writes* function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

Attempt to write a read-only address (NACK after data sent by master):

Attempt to read an address above 0x7F (NACK command):

Attempt at incremental writes (NACK all extra data bytes sent):

Incremental read at the maximum allowed read address:

The I^2C engine releases both SDA and SCL if the I^2C bus is held low for $t_{(BUSERR)}$. If the fuel gauge was holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I^2C engine enters the low-power SLEEP mode.

8.3.5.7.1 I^2C Time Out

The I^2C engine will release both SDA and SCL if the I^2C bus is held low for about 2 seconds. If the bq27546-G1 device were holding the lines, releasing them frees for the master to drive the lines.

8.3.5.7.2 I^2C Command Waiting Time

To ensure there are correct results of a command with the 400-KHz I^2C operation, a proper waiting time should be added between issuing command and reading results. For subcommands, the following diagram shows the waiting time required between issuing the control command the reading the status with the exception of the checksum command. A 100-ms waiting time is required between the checksum command and reading result. For read-write standard commands, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host should not issue all standard commands more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.

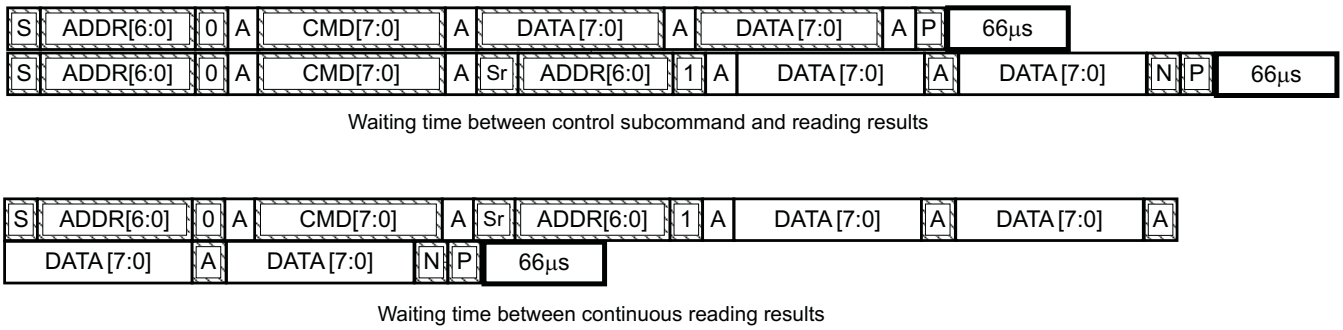


Figure 8. I^2C Command Waiting Time

8.3.5.7.3 I²C Clock Stretching

I²C clock stretches can occur during all modes of fuel gauge operation. In the SLEEP and HIBERNATE modes, a short clock stretch will occur on all I²C traffic as the device must wake-up to process the packet. In NORMAL and SLEEP modes, clock stretching will only occur for packets addressed for the fuel gauge. The timing of stretches will vary as interactions between the communicating host and the gauge are asynchronous. The I²C clock stretches may occur after start bits, the ACK/NAK bit, and first data bit transmit on a host read cycle. The majority of clock stretch periods are small (≤ 4 ms) as the I²C interface peripheral and CPU firmware perform normal data flow control. However, less frequent but more significant clock stretch periods may occur when data flash (DF) is being written by the CPU to update the resistance (Ra) tables and other DF parameters, such as Qmax. Due to the organization of DF, updates need to be written in data blocks consisting of multiple data bytes.

An Ra table update requires erasing a single page of DF, programming the updated Ra table and a flag. The potential I²C clock stretching time is 24-ms max. This includes 20-ms page erase and 2-ms row programming time (×2 rows). The Ra table updates occur during the discharge cycle and at up to 15 resistance grid points that occur during the discharge cycle.

A DF block write typically requires a max of 72 ms. This includes copying data to a temporary buffer and updating DF. This temporary buffer mechanism is used for protection from power failure during a DF update. The first part of the update requires 20 ms time to erase the copy buffer page, 6 ms to write the data into the copy buffer, and the program progress indicator (2 ms for each individual write). The second part of the update is writing to the DF and requires 44-ms DF block update time. This includes a 20-ms each page erase for two pages and a 2-ms each row write for two rows.

In the event that a previous DF write was interrupted by a power failure or reset during the DF write, an additional 44-ms max DF restore time is required to recover the data from a previously interrupted DF write. In this power failure recovery case, the total I²C clock stretching is 116-ms max.

Another case where I²C clock stretches is at the end of discharge. The update to the last discharge data will go through the DF block update twice because two pages are used for the data storage. The clock stretching in this case is 144-ms max. This occurs if there has been a Ra table update during the discharge.

8.4 Device Functional Modes

8.4.1 Power Modes

The bq27546-G1 device has four power modes: NORMAL, SLEEP, FULLSLEEP, and HIBERNATE.

- In NORMAL mode, the bq27546-G1 is fully powered and can execute any allowable task.
- In SLEEP mode, the fuel gauge exists in a reduced-power state, periodically taking measurements and performing calculations.
- During FULLSLEEP mode, the bq27545-G1 periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.
- In HIBERNATE mode, the fuel gauge is in a very low power state, but can be awoken by communication or certain I/O activity.

Figure 9 shows the relationship among these modes. Details are described in the sections that follow.

Device Functional Modes (continued)

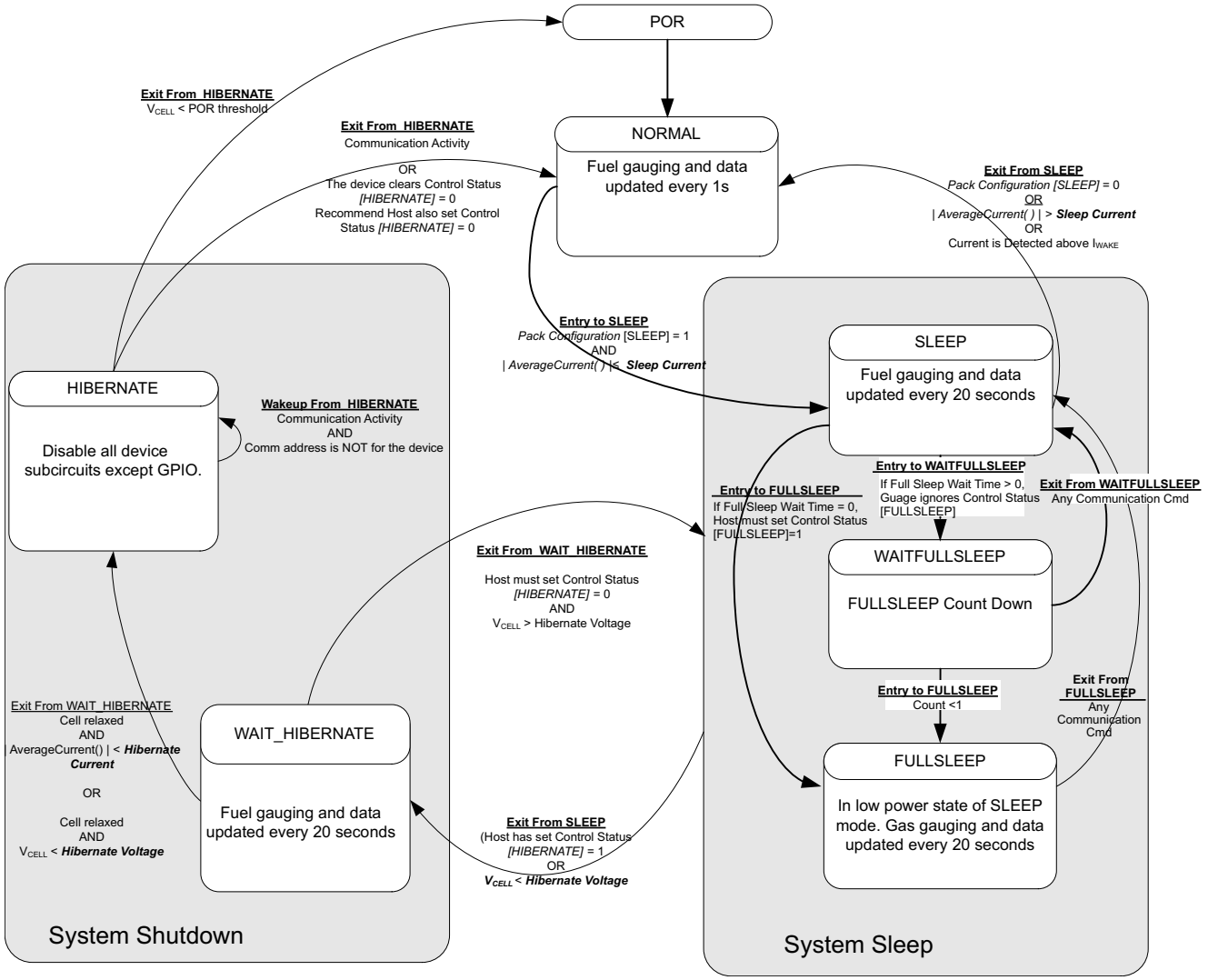


Figure 9. Power Mode Diagram

8.4.1.1 NORMAL Mode

The fuel gauge is in NORMAL mode when not in any other power mode. During this mode, *AverageCurrent()*, *Voltage()*, and *Temperature()* measurements are taken, and the interface data set is updated. Decisions to change states are also made. This mode is exited by activating a different power mode.

Because the gauge consumes the most power in NORMAL mode, the Impedance Track™ algorithm minimizes the time the fuel gauge remains in this mode.

8.4.1.2 SLEEP Mode

SLEEP mode is entered automatically if the feature is enabled (***Pack Configuration [SLEEP]***) = 1) and *AverageCurrent()* is below the programmable level ***Sleep Current***. Once entry into SLEEP mode is qualified, but prior to entering it, the bq27546-G1 performs an ADC autocalibration to minimize offset.

While in SLEEP mode, the fuel gauge can suspend serial communications as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, since the fuel gauge processor is mostly halted in SLEEP mode.

Device Functional Modes (continued)

During SLEEP mode, the bq27546-G1 periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The bq27546-G1 exits SLEEP if any entry condition is broken, specifically when (1) *AverageCurrent()* rises above ***Sleep Current***, or (2) a current in excess of I_{WAKE} through R_{SENSE} is detected when the I_{WAKE} comparator is enabled.

8.4.1.3 FULLSLEEP Mode

FULLSLEEP mode is entered automatically when the bq27546-G1 is in SLEEP mode and the timer counts down to 0 (*Full Sleep Wait Time* > 0). FULLSLEEP mode is entered immediately after entry to SLEEP if ***Full Sleep Wait Time*** is set to 0 and the host sets the [FULLSLEEP] bit in the CONTROL_STATUS register using the SET_FULLSLEEP subcommand.

The gauge exits the FULLSLEEP mode when there is any communication activity. The [*FULLSLEEP*] bit can remain set (*Full Sleep Wait Time* > 0) or be cleared (*Full Sleep Wait Time* ≤ 0) after exit of FULLSLEEP mode. Therefore, EVSW communication activity might cause the gauge to exit FULLSLEEP mode and display the [*FULLSLEEP*] bit as clear. The execution of SET_FULLSLEEP to set [*FULLSLEEP*] bit is required when *Full Sleep Wait Time* ≤ 0 in order to re-enter FULLSLEEP mode. FULLSLEEP mode can be verified by measuring the current consumption of the gauge. In this mode, the high frequency oscillator is turned off. The power consumption is further reduced in this mode compared to SLEEP mode.

While in FULLSLEEP mode, the fuel gauge can suspend serial communications as much as 4 ms by holding the comm line(s) low. This delay is necessary to correctly process host communication, since the fuel gauge processor is mostly halted in SLEEP mode.

The bq27546-G1 exits FULLSLEEP if any entry condition is broken, specifically when (1) *AverageCurrent()* rises above ***Sleep Current***, or (2) a current in excess of I_{WAKE} through R_{SENSE} is detected when the I_{WAKE} comparator is enabled.

8.4.1.4 HIBERNATE Mode

HIBERNATE mode should be used for long-term pack storage or when the host system needs to enter a low-power state and minimal gauge power consumption is required. This mode is ideal when the host is set to its own HIBERNATE, SHUTDOWN, or OFF mode. The gauge waits to enter HIBERNATE mode until it has taken a valid OCV measurement (cell relaxed) and the value of the average cell current has fallen below ***Hibernate Current***. When the conditions are met, the fuel gauge can enter HIBERNATE due to either low cell voltage or by having the [HIBERNATE] bit of the CONTROL_STATUS register set. The gauge remains in HIBERNATE mode until any communication activity appears on the communication lines and the address is for the bq27546-G1 device. In addition, the SE pin SHUTDOWN mode function is supported only when the fuel gauge enters HIBERNATE due to low cell voltage.

When the gauge wakes up from HIBERNATE mode, the [HIBERNATE] bit of the CONTROL_STATUS register is cleared. The host is required to set the bit in order to allow the gauge to re-enter HIBERNATE mode if desired.

Because the fuel gauge is dormant in HIBERNATE mode, the battery should not be charged or discharged in this mode, because any changes in battery charge status will not be measured. If necessary, the host equipment can draw a small current (generally infrequent and less than 1 mA) for purposes of low-level monitoring and updating; however, the corresponding charge drawn from the battery will not be logged by the gauge. Once the gauge exits to NORMAL mode, the IT algorithm will take approximately 3 s to re-establish the correct battery capacity and measurements, regardless of the total charge drawn in HIBERNATE mode. During this period of re-establishment, the gauge reports values previously calculated prior to entering HIBERNATE mode. The host can identify exit from HIBERNATE mode by checking if *Voltage()* < ***Hibernate Voltage*** or [HIBERNATE] bit is cleared by the gauge.

If a charger is attached, the host should immediately take the fuel gauge out of HIBERNATE mode before beginning to charge the battery. Charging the battery in HIBERNATE mode will result in a notable gauging error that will take several hours to correct. It is also recommended to minimize discharge current during exit from HIBERNATE.

Device Functional Modes (continued)

8.4.2 System Control Function

The fuel gauge provides system control functions that allow the fuel gauge to enter SHUTDOWN mode in order to power-off with the assistance of an external circuit or provide interrupt function to the system. Table 2 shows the configurations for SE and HDQ pins.

Table 2. SE and HDQ Pin Functions

[INTSEL]	COMMUNICATION MODE	SE PIN FUNCTION	HDQ PIN FUNCTION
0 (default)	I^2C	Interrupt Mode (1)	Not Used
	HDQ		HDQ Mode(2)
1	I^2C	Shutdown Mode	Interrupt Mode
	HDQ		HDQ Mode(2)

(1) The [SE_EN] bit in ***Pack Configuration*** can be enabled to use the *[SE]* and *[SHUTDWN]* bits in the *CONTROL_STATUS()* function. The SE pin shutdown function is disabled.
(2) The HDQ pin is used for communication and the HDQ Host Interrupt Feature is available.

8.4.2.1 SHUTDOWN Mode

In SHUTDOWN mode, the SE pin is used to signal the external circuit to power-off the fuel gauge. This feature is useful to shut down the fuel gauge in a deeply discharged battery to protect the battery. By default, SHUTDOWN mode is in NORMAL state. By sending the SET_SHUTDOWN subcommand or setting the ***[SE_EN]*** bit in ***the Pack Configuration*** register, the *[SHUTDWN]* bit is set and enables the shutdown feature. When this feature is enabled and *[INTSEL]* is set, the SE pin can be in NORMAL state or SHUTDOWN state. The SHUTDOWN state can be entered in HIBERNATE mode (only if HIBERNATE mode is enabled due to low cell voltage). All other power modes will default the SE pin to NORMAL state. Table 3 shows the SE pin state in NORMAL or SHUTDOWN mode. The CLEAR_SHUTDOWN subcommand or clearing ***[SE_EN]*** bit in the ***Pack Configuration*** register can be used to disable SHUTDOWN mode.

The SE pin will be high impedance at power-on reset (POR), and the *[SE_POL]* does not affect the state of SE pin at POR. Also, *[SE_PU]* configuration changes will only take effect after POR. In addition, the *[INTSEL]* only controls the behavior of the SE pin; it does not affect the function of *[SE]* and *[SHUTDWN]* bits.

Table 3. SE Pin State

		SHUTDOWN Mode *[INTSEL] = 1* and (*[SE_EN] or [SHUTDOWN]* = 1)	
[SE_PU]	*[SE_POL]*	NORMAL State	SHUTDOWN State
0	0	High Impedance	0
0	1	0	High Impedance
1	0	1	0
1	1	0	1

8.4.2.2 INTERRUPT Mode

By using the INTERRUPT mode, the system can be interrupted based on detected fault conditions, as specified in Table 6. The SE or HDQ pin can be selected as the interrupt pin by configuring the ***[INTSEL]*** bit based on . In addition, the pin polarity and pullup (SE pin only) can be configured according to the system's needs, as described in Table 4 or Table 5.

Table 4. SE Pin in Interrupt Mode ([INTSEL] = 0)

[SE_PU]	*[INTPOL]*	INTERRUPT CLEAR	INTERRUPT SET
0	0	High Impedance	0
0	1	0	High Impedance
1	0	1	0
1	1	0	1

Table 5. HDQ Pin in Interrupt Mode ([INTSEL] = 1)

[INTPOL]	INTERRUPT CLEAR	INTERRUPT SET
0	High Impedance	0
1	0	High Impedance

Table 6. Interrupt Mode Fault Conditions

INTERRUPT CONDITION	Flags() STATUS BIT	ENABLE CONDITION	COMMENT
SOC1 Set	*[SOC1]*	Always	This interrupt is raised when the *[SOC1]* flag is set.
Battery High	*[BATHI]*	Always	This interrupt is raised when the *[BATHI]* flag is set.
Battery Low	*[BATLOW]*	Always	This interrupt is raised when the *[BATLOW]* flag is set.
Over-Temperature Charge	*[OTC]*	***OT Chg Time*** ≠ 0	This interrupt is raised when the *[OTC]* flag is set.
Over-Temperature Discharge	*[OTD]*	***OT Dsg Time*** ≠ 0	This interrupt is raised when the *[OTD]* flag is set.
Internal Short Detection	*[ISD]*	***[SE_ISD]*** = 1 in ***Pack Configuration B***	This interrupt is raised when the *[ISD]* flag is set.
Tab Disconnect Detection	*[TDD]*	***[SE_TDD]*** = 1 in ***Pack Configuration B***	This interrupt is raised when the *[TDD]* flag is set.
Imax	*[IMAX]*	***[IMAXEN]*** = 1 in ***Pack Configuration D***	This interrupt is raised when the *[IMAX]* flag is set.
Battery Trip Point (BTP)	*[SOC1]*	***[BTP_EN]*** = 1 in ***Pack Configuration C***. The BTP interrupt supersedes all other interrupt sources, which are unavailable when BTP is active.	This interrupt is raised when *RemainingCapacity()* ≤ *BTPSOC1Set()* or *RemainingCapacity()* ≥ *BTPSOC1Clear()* during battery discharge or charge, respectively. The interrupt remains asserted until new values are written to both the *BTPSOC1Set()* and *BTPSOC1Clear()* registers.

8.4.3 Security Modes

The bq27546-G1 provides three security modes (FULL ACCESS, UNSEALED, and SEALED) that control data flash access permissions. *Data flash* refers to those data flash locations that are accessible to the user. *Manufacture Information* refers to the two 32-byte blocks.

8.4.3.1 Sealing and Unsealing Data Flash

The bq27546-G1 implements a key-access scheme to transition between SEALED, UNSEALED, and FULL ACCESS modes. Each transition requires that a unique set of two keys be sent to the bq27546-G1 via the *Control()* command. The keys must be sent consecutively with no other data being written to the *Control()* register in between.

NOTE

To avoid conflict, the keys must be different from the codes presented in the *CNTL DATA* column of Table 8 subcommands.

When in SEALED mode the *[SS]* bit of CONTROL_STATUS is set, but when the UNSEAL keys are correctly received by the bq27546-G1, the *[SS]* bit is cleared. When the full-access keys are correctly received the CONTROL_STATUS *[FAS]* bit is cleared.

Both ***Unseal Key*** and ***Full-Access Key*** have two words and are stored in data flash. The first word is Key 0 and the second word is Key 1. The order of the keys sent to bq27546-G1 are Key 1 followed by Key 0. The order of the bytes for each key entered through the *Control()* command is the reverse of what is read from the part. For an example, if the Unseal Key is 0x56781234, key 1 is 0x1234 and key 0 is 0x5678. Then *Control()* should supply 0x3412 and 0x7856 to unseal the part. The ***Unseal Key*** and the ***Full-Access Key*** can only be updated when in FULL ACCESS mode.

8.5 Programming

8.5.1 Standard Data Commands

The bq27546-G1 uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in Table 7. Each protocol has specific means to access the data at each Command Code. DataRAM is updated and read by the gauge only once per second. Standard commands are accessible in NORMAL operation mode.

Table 7. Standard Commands

COMMAND NAME	COMMAND CODE	UNIT	SEALED ACCESS
Control()	0x00 and 0x01	—	RW
AtRate()	0x02 and 0x03	mA	RW
UnfilteredSOC()	0x04 and 0x05	%	R
Temperature()	0x06 and 0x07	0.1°K	R
Voltage()	0x08 and 0x09	mV	R
Flags()	0x0A and 0x0B	—	R
NomAvailableCapacity()	0x0C and 0x0D	mAh	R
FullAvailableCapacity()	0x0E and 0x0F	mAh	R
RemainingCapacity()	0x10 and 0x11	mAh	R
FullChargeCapacity()	0x12 and 0x13	mAh	R
AverageCurrent()	0x14 and 0x15	mA	R
TimeToEmpty()	0x16 and 0x17	min	R
FullChargeCapacityFiltered()	0x18 and 0x19	mAh	R
SafetyStatus()	0x1A and 0x1B	—	R
FullChargeCapacityUnfiltered()	0x1C and 0x1D	mAh	R
Imax()	0x1E and 0x1F	mA	R
RemainingCapacityUnfiltered()	0x20 and 0x21	mAh	R
RemainingCapacityFiltered()	0x22 and 0x23	mAh	R
BTPSOC1Set()	0x24 and 0x25	mAh	RW
BTPSOC1Clear()	0x26 and 0x27	mAh	RW
InternalTemperature()	0x28 and 0x29	0.1°K	R
CycleCount()	0x2A and 0x2B	Counts	R
StateofCharge()	0x2C and 0x2D	%	R
StateofHealth()	0x2E and 0x2F	% / num	R
ChargingVoltage()	0x30 and 0x31	mV	R
ChargingCurrent)	0x32 and 0x33	mA	R
PassedCharge()	0x34 and 0x35	mAh	R
DOD0()	0x36 and 0x37	hex	R
SelfDischargeCurrent()	0x34 and 0x35	mA	R

8.5.1.1 Control(): 0x00 and 0x01

Issuing a *Control()* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control()* command allows the system to control specific features of the bq27546-G1 during normal operation and additional features when the bq27546-G1 is in different access modes, as described in Table 8.

Table 8. *Control()* Subcommands

SUBCOMMAND NAME	SUBCOMMAND CODE	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of DF Checksum, Impedance Track, and so on
DEVICE_TYPE	0x0001	Yes	Reports the device type of 0x0541 (indicating bq27546-G1)

Table 8. *Control()* Subcommands (continued)

SUBCOMMAND NAME	SUBCOMMAND CODE	SEALED ACCESS	DESCRIPTION
FW_VERSION	0x0002	Yes	Reports the firmware version on the device type
HW_VERSION	0x0003	Yes	Reports the hardware version on the device type
RESET_DATA	0x0005	Yes	Returns reset data
PREV_MACWRITE	0x0007	Yes	Returns previous *Control()* subcommand code
CHEM_ID	0x0008	Yes	Reports the chemical identifier of the Impedance Track configuration
BOARD_OFFSET	0x0009	No	Forces the device to measure and store the board offset
CC_OFFSET	0x000A	No	Forces the device to measure the CC offset
DF_VERSION	0x000C	Yes	Reports the data flash version of the device
SET_FULLSLEEP	0x0010	Yes	Sets the *CONTROL_STATUS[FULLSLEEP]* bit to 1
SET_SHUTDOWN	0x0013	Yes	Sets the *CONTROL_STATUS[SHUTDWN]* bit to 1
CLEAR_SHUTDOWN	0x0014	Yes	Clears the *CONTROL_STATUS[SHUTDWN]* bit to 1
SET_HDQINTEN	0x0015	Yes	Forces CONTROL_STATUS [HDQHOSTIN] to 1
CLEAR_HDQINTEN	0x0016	Yes	Forces CONTROL_STATUS [HDQHOSTIN] to 0
STATIC_CHEM_CHKSUM	0x0017	Yes	Calculates chemistry checksum
ALL_DF_CHKSUM	0x0018	Yes	Reports checksum for all data flash excluding device specific variables
STATIC_DF_CHKSUM	0x0019	Yes	Reports checksum for static data flash excluding device specific variables
SYNC_SMOOTH	0x001E	Yes	Synchronizes *RemCapSmooth()* and *FCCSmooth()* with *RemCapTrue()* and *FCCTrue()*
SEALED	0x0020	No	Places the fuel gauge in SEALED access mode
IT_ENABLE	0x0021	No	Enables the Impedance Track algorithm
IMAX_INT_CLEAR	0x0023	Yes	Clears an Imax interrupt that is currently asserted on the RC2 pin
CAL_ENABLE	0x002D	No	Toggle CALIBRATION mode
RESET	0x0041	No	Forces a full reset of the fuel gauge
EXIT_CAL	0x0080	No	Exit CALIBRATION mode
ENTER_CAL	0x0081	No	Enter CALIBRATION mode
OFFSET_CAL	0x0082	No	Reports internal CC offset in CALIBRATION mode

8.6 Register Maps

8.6.1 Pack Configuration Register

Some bq27546-G1 pins are configured via the ***Pack Configuration*** data flash register, as indicated in Table 9. This register is programmed/read via the methods described in the *bq27546-G1 Technical Reference Manual* (SLUUB74). The register is located at Subclass = 64, offset = 0.

Table 9. Pack Configuration Bit Definition

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	RESCAP	CALEN	INTPOL	INTSEL	RSVD	IWAKE	RSNS1	RSNS0
Default =	0	0	0	1	0	0	0	1
	0x11							
Low Byte	GNDSEL	RFACTSTEP	SLEEP	RMFCC	SE_PU	SE_POL	SE_EN	TEMPS
Default =	0	1	1	1	0	1	1	1
	0x77							

RESCAP = No-load rate of compensation is applied to the reserve capacity calculation. True when set.

CALEN = Calibration mode is enabled.

INTPOL = Polarity for Interrupt pin. (See *INTERRUPT Mode*.)

INTSEL = Interrupt Pin select: 0 = SE pin, 1 = HDQ pin. (See *INTERRUPT Mode*.)

RSVD = Reserved. Must be 0.

IWAKE/RSNS1/RSNS0 = These bits configure the current wake function (see *Wake-Up Comparator*).

GNDSEL = The ADC ground select control. The V_{SS} (pins C1, C2) is selected as ground reference when the bit is clear. Pin A1 is selected when the bit is set.

RFACTSTEP = Enables Ra step up/down to Max/Min Res Factor before disabling Ra updates.

SLEEP = The fuel gauge can enter sleep, if operating conditions allow. True when set. (See *SLEEP Mode*.)

RMFCC = RM is updated with the value from FCC, on valid charge termination. True when set.

SE_PU = Pull-up enable for SE pin. True when set (push-pull).

SE_POL = Polarity bit for SE pin. SE is active high when set (makes SE high when gauge is ready for shutdown).

SE_EN = Indicates if set the shutdown feature is enabled. True when set.

TEMPS = Selects external thermistor for *Temperature()* measurements. True when set.

8.6.2 Pack Configuration B Register

Some bq27546-G1 pins are configured via the ***Pack Configuration B*** data flash register, as indicated in Table 10. This register is programmed/read via the methods described in the *bq27546-G1 Technical Reference Manual* (SLUUB74). The register is located at Subclass = 64, offset = 2.

Table 10. Pack Configuration B Bit Definition

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	ChgDoD EoC	SE_TDD	VconsEN	SE_ISD	RSVD	LFPRelax	DoDWT	FConvEn
Default =	1	0	1	0	0	1	1	1
	0x67							

ChgDoDEoC = Enable DoD at EoC recalculation during charging only. True when set. The default setting is recommended.
SE_TDD = Enable Tab Disconnection Detection. True when set.
VconsEN = Enable voltage consistency check. True when set. The default setting is recommended.
SE_ISD = Enable Internal Short Detection. True when set.
RSVD = Reserved. Must be 0.
LFPRelax = Enable LiFePO4 long relaxation mode. True when set.
DoDWT = Enable DoD weighting feature of gauging algorithm. This feature can improve accuracy during relaxation in a flat portion of the voltage profile, especially when using LiFePO4 chemistry. True when set.
FConvEn = Enable fast convergence algorithm. The default setting is recommended.

8.6.3 Pack Configuration C Register

Some bq27546-G1 algorithm settings are configured via the ***Pack Configuration C*** data flash register, as indicated in Table 11. This register is programmed/read via the methods described in the *bq27546-G1 Technical Reference Manual* (SLUUB74). The register is located at Subclass = 64, offset = 3.

Table 11. Pack Configuration C Bit Definition

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	RSVD	RSVD	RelaxRCJumpOK	SmoothEn	SleepWk Chg	RSVD	RSVD	RSVD
Default =	0	0	0	1	1	0	0	0
	0x18							

RSVD = Reserved. Must be 0.
RelaxRCJumpOK = Allow SOC to change due to temperature change during relaxation when SOC smoothing algorithm is enabled. True when set.
SmoothEn = Enable SOC smoothing algorithm. True when set.
SleepWkChg = Enables compensation for the passed charge missed when waking from SLEEP mode.

9 Application and Implementation

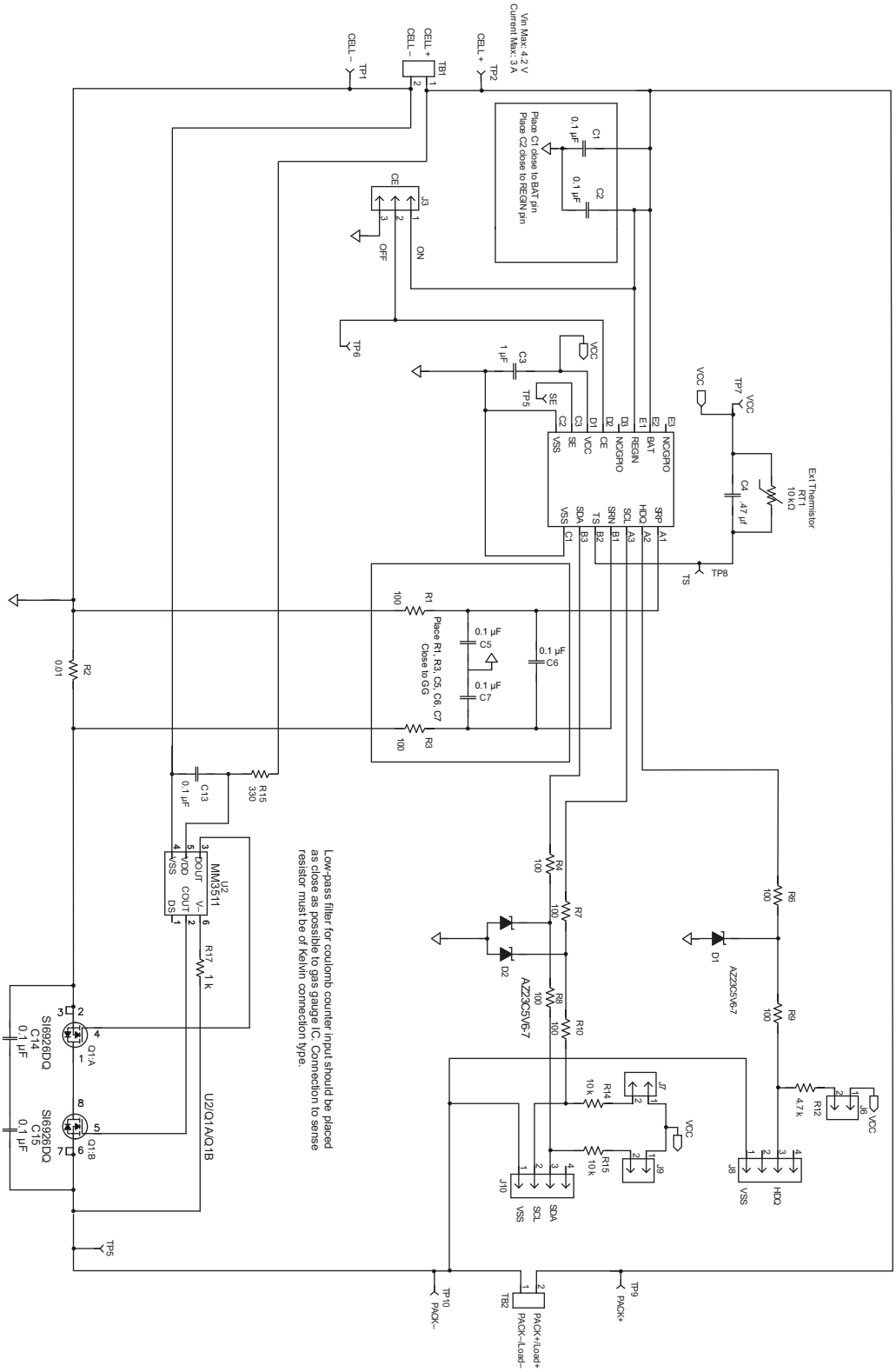
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq27546-G1 measures the cell voltage, temperature, and current to determine battery SOC based on Impedance Track™ algorithm (see *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm Application Note* (SLUA450) for more information). The bq27546-G1 monitors charge and discharge activity by sensing the voltage across a small-value resistor (5 mΩ to 20 mΩ typ.) between the SRP and SRN pins and in series with the cell. By integrating charge passing through the battery, the battery's SOC is adjusted during battery charge or discharge.

9.2 Typical Applications



R7, R8, and R9 are optional pull-down resistors if pull-up resistors are applied.

Figure 10. Schematic

Typical Applications (continued)

9.2.1 Design Requirements

Several key parameters must be updated to align with a given application's battery characteristics. For highest accuracy gauging, it is important to follow-up this initial configuration with a learning cycle to optimize resistance and maximum chemical capacity (Qmax) values prior to sealing and shipping systems to the field. Successful and accurate configuration of the fuel gauge for a target application can be used as the basis for creating a "golden" file that can be written to all gauges, assuming identical pack design and Li-Ion cell origin (chemistry, lot, and so on). Calibration data is included as part of this golden file to cut down on system production time. If using this method, it is recommended to average the voltage and current measurement calibration data from a large sample size and use these in the golden file. Table 12 shows the items that should be configured to achieve reliable protection and accurate gauging with minimal initial configuration.

Table 12. Key Data Flash Parameters for Configuration

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
Design Capacity	1000	mAh	Set based on the nominal pack capacity as interpreted from the cell manufacturer's data sheet. If multiple parallel cells are used, should be set to N × Cell Capacity.
Design Energy Scale	1	—	Set to 10 to convert all power values to cWh or to 1 for mWh. ***Design Energy*** is divided by this value.
Reserve Capacity-mAh	0	mAh	Set to desired runtime remaining (in seconds/3600) × typical applied load between reporting 0% SOC and reaching ***Terminate Voltage***, if needed.
Cycle Count Threshold	900	mAh	Set to 90% of configured ***Design Capacity***.
Chem ID	0100	hex	Should be configured using TI-supplied Battery Management Studio (bqStudio) software. Default open-circuit voltage and resistance tables are also updated in conjunction with this step. Do not attempt to manually update reported Device Chemistry as this does not change all chemistry information. Always update chemistry using the bqStudio software tool.
Load Mode	1	—	Set to applicable load model, 0 for constant current or 1 for constant power.
Load Select	1	—	Set to load profile which most closely matches typical system load.
Qmax Cell 0	1000	mAh	Set to initial configured value for Design Capacity. The gauge will update this parameter automatically after the optimization cycle and for every regular Qmax update thereafter.
Cell0 V at Chg Term	4200	mV	Set to nominal cell voltage for a fully charged cell. The gauge will update this parameter automatically each time full charge termination is detected.
Terminate Voltage	3200	mV	Set to empty point reference of battery based on system needs. Typical is between 3000 and 3200 mV.
Ra Max Delta	44	mΩ	Set to 15% of Cell0 R_a 4 resistance after an optimization cycle is completed.
Charging Voltage	4200	mV	Set based on nominal charge voltage for the battery in normal conditions (25°C, and so on). Used as the reference point for offsetting by ***Taper Voltage*** for full charge termination detection.
Taper Current	100	mA	Set to the nominal taper current of the charger + taper current tolerance to ensure that the gauge will reliably detect charge termination.
Taper Voltage	100	mV	Sets the voltage window for qualifying full charge termination. Can be set tighter to avoid or wider to ensure possibility of reporting 100% SOC in outer JEITA temperature ranges that use derated charging voltage.
Dsg Current Threshold	60	mA	Sets threshold for gauge detecting battery discharge. Should be set lower than minimal system load expected in the application and higher than ***Quit Current***.
Chg Current Threshold	75	mA	Sets the threshold for detecting battery charge. Can be set higher or lower depending on typical trickle charge current used. Also should be set higher than ***Quit Current***.
Quit Current	40	mA	Sets threshold for gauge detecting battery relaxation. Can be set higher or lower depending on typical standby current and exhibited in the end system.
Avg I Last Run	–299	mA	Current profile used in capacity simulations at onset of discharge or at all times if ***Load Select*** = 0. Should be set to nominal system load. Is automatically updated by the gauge every cycle.
Avg P Last Run	–1131	mW	Power profile used in capacity simulations at onset of discharge or at all times if ***Load Select*** = 0. Should be set to nominal system power. Is automatically updated by the gauge every cycle.

Typical Applications (continued)

Table 12. Key Data Flash Parameters for Configuration (continued)

NAME	DEFAULT	UNIT	RECOMMENDED SETTING
Sleep Current	15	mA	Sets the threshold at which the fuel gauge enters SLEEP mode. Take care in setting above typical standby currents else entry to SLEEP may be unintentionally blocked.
Charge T0	0	°C	Sets the boundary between charging inhibit and charging with T0 parameters.
Charge T1	10	°C	Sets the boundary between charging with T0 and T1 parameters.
Charge T2	45	°C	Sets the boundary between charging with T1 and T2 parameters.
Charge T3	50	°C	Sets the boundary between charging with T2 and T3 parameters.
Charge T4	60	°C	Sets the boundary between charging with T3 and T4 parameters.
Charge Current T0	50	% Des Cap	Sets the charge current parameter for T0.
Charge Current T1	50	% Des Cap	Sets the charge current parameter for T1.
Charge Current T2	50	% Des Cap	Sets the charge current parameter for T2.
Charge Current T3	50	% Des Cap	Sets the charge current parameter for T3.
Charge Current T4	0	% Des Cap	Sets the charge current parameter for T4.
Charge Voltage T0	210	20 mV	Sets the charge voltage parameter for T0.
Charge Voltage T1	210	20 mV	Sets the charge voltage parameter for T1.
Charge Voltage T2	207	20 mV	Sets the charge voltage parameter for T2.
Charge Voltage T3	205	20 mV	Sets the charge voltage parameter for T3.
Charge Voltage T4	0	20 mV	Sets the charge voltage parameter for T4.
Chg Temp Hys	5	°C	Adds temperature hysteresis for boundary crossings to avoid oscillation if temperature is changing by a degree or so on a given boundary.
Chg Disabled Regulation V	4200	mV	Sets the voltage threshold for voltage regulation to system when charge is disabled. It is recommended to program to same value as Charging Voltage and maximum charge voltage that is obtained from Charge Voltage T0–4 parameters.
CC Gain	10	mΩ	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines conversion of coulomb counter measured sense resistor voltage to current.
CC Delta	10	mΩ	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines conversion of coulomb counter measured sense resistor voltage to passed charge.
CC Offset	–1418	Counts	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines native offset of coulomb counter hardware that should be removed from conversions.
Board Offset	0	Counts	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines native offset of the printed circuit board parasitics that should be removed from conversions.
Pack V Offset	0	mV	Calibrate this parameter using TI-supplied bqStudio software and calibration procedure in the TRM. Determines voltage offset between cell tab and ADC input node to incorporate back into or remove from measurement, depending on polarity.

9.2.2 Detailed Design Procedure

9.2.2.1 BAT Voltage Sense Input

A ceramic capacitor at the input to the BAT pin is used to bypass AC voltage ripple to ground, greatly reducing its influence on battery voltage measurements. It proves most effective in applications with load profiles that exhibit high-frequency current pulses (that is, cell phones), but is recommended for use in all applications to reduce noise on this sensitive high-impedance measurement node.

9.2.2.2 SRP and SRN Current Sense Inputs

The filter network at the input to the coulomb counter is intended to improve differential mode rejection of voltage measured across the sense resistor. These components should be placed as close as possible to the coulomb counter inputs and the routing of the differential traces length-matched to best minimize impedance mismatch-induced measurement errors.

9.2.2.3 Sense Resistor Selection

Any variation encountered in the resistance present between the SRP and SRN pins of the fuel gauge will affect the resulting differential voltage and derived current it senses. As such, it is recommended to select a sense resistor with minimal tolerance and temperature coefficient of resistance (TCR) characteristics. The standard recommendation based on best compromise between performance and price is a 1% tolerance, 100-ppm drift sense resistor with a 1-W power rating.

9.2.2.4 TS Temperature Sense Input

Similar to the BAT pin, a ceramic decoupling capacitor for the TS pin is used to bypass AC voltage ripple away from the high-impedance ADC input, minimizing measurement error. Another helpful advantage is that the capacitor provides additional ESD protection since the TS input to system may be accessible in systems that use removable battery packs. It should be placed as close as possible to the respective input pin for optimal filtering performance.

9.2.2.5 Thermistor Selection

The fuel gauge temperature sensing circuitry is designed to work with a negative temperature coefficient-type (NTC) thermistor with a characteristic 10-kΩ resistance at room temperature (25°C). The default curve-fitting coefficients configured in the fuel gauge specifically assume a 103AT-2 type thermistor profile and so that is the default recommendation for thermistor selection purposes. Moving to a separate thermistor resistance profile (for example, JT-2 or others) requires an update to the default thermistor coefficients in data flash to ensure highest accuracy temperature measurement performance.

9.2.2.6 REGIN Power Supply Input Filtering

A ceramic capacitor is placed at the input to the fuel gauge internal LDO to increase power supply rejection (PSR) and improve effective line regulation. It ensures that voltage ripple is rejected to ground instead of coupling into the internal supply rails of the fuel gauge.

9.2.2.7 V_{CC} LDO Output Filtering

A ceramic capacitor is also needed at the output of the internal LDO to provide a current reservoir for fuel gauge load peaks during high peripheral utilization. It acts to stabilize the regulator output and reduce core voltage ripple inside of the fuel gauge.

9.3 Application Curves

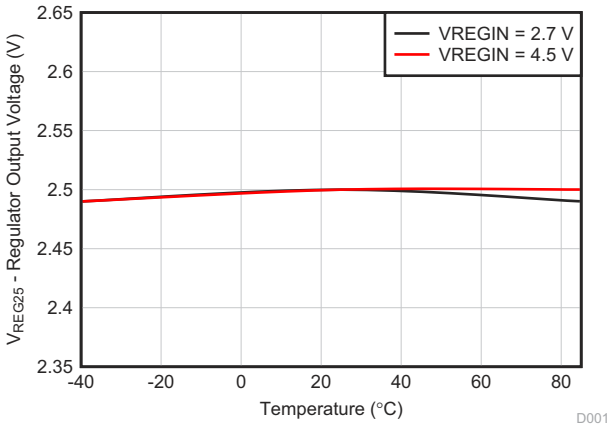


Figure 11. Regulator Output Voltage Vs. Temperature

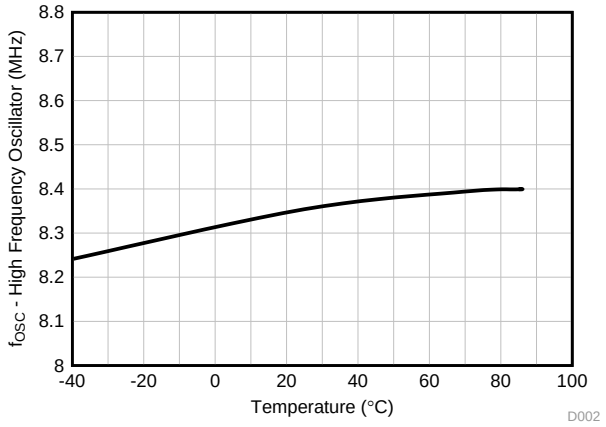


Figure 12. High-Frequency Oscillator Frequency Vs. Temperature

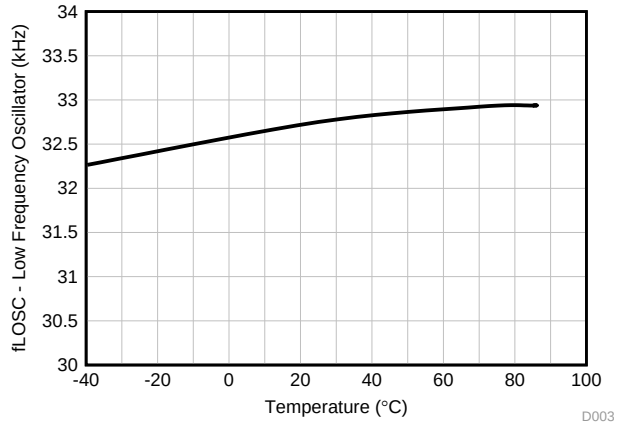


Figure 13. Low-Frequency Oscillator Frequency Vs. Temperature

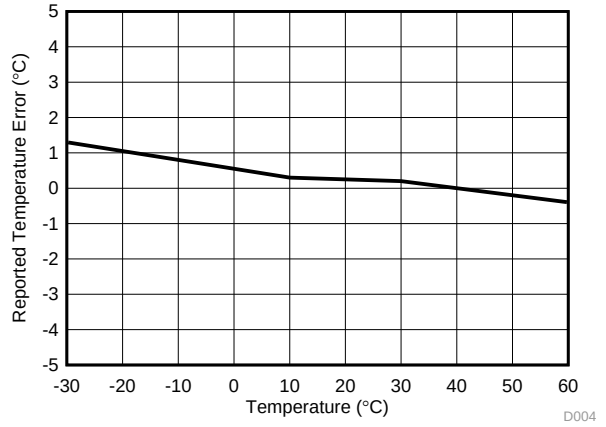


Figure 14. Reported Internal Temperature Measurement Vs. Temperature

10 Power Supply Recommendations

10.1 Power Supply Decoupling

Both the REGIN input pin and the V_{CC} output pin require low equivalent series resistance (ESR) ceramic capacitors placed as close as possible to the respective pins to optimize ripple rejection and provide a stable and dependable power rail that is resilient to line transients. A 0.1-µF capacitor at the REGIN and a 1-µF capacitor at V_{CC} will suffice for satisfactory device performance.

11 Layout

11.1 Layout Guidelines

11.1.1 Sense Resistor Connections

Kelvin connections at the sense resistor are as critical as those for the battery terminals. The differential traces should be connected at the inside of the sense resistor pads and not along the high-current trace path to prevent false increases to measured current that could result when measuring between the sum of the sense resistor and trace resistance between the tap points. In addition, the routing of these leads from the sense resistor to the input filter network and finally into the SRP and SRN pins needs to be as closely matched in length as possible or else additional measurement offset could occur. It is further recommended to add copper trace or pour-based "guard rings" around the perimeter of the filter network and coulomb counter inputs to shield these sensitive pins from radiated EMI into the sense nodes. This prevents differential voltage shifts that could be interpreted as real current change to the fuel gauge. All of the filter components need to be placed as close as possible to the coulomb counter input pins.

11.1.2 Thermistor Connections

The thermistor sense input should include a ceramic bypass capacitor placed as close to the TS input pin as possible. The capacitor helps to filter measurements of any stray transients as the voltage bias circuit pulses periodically during temperature sensing windows.

11.1.3 High-Current and Low-Current Path Separation

NOTE

For best possible noise performance, it is important to separate the low-current and high-current loops to different areas of the board layout.

The fuel gauge and all support components should be situated on one side of the boards and tap off of the high-current loop (for measurement purposes) at the sense resistor. Routing the low-current ground around instead of under high-current traces will further help to improve noise rejection.

11.2 Layout Example

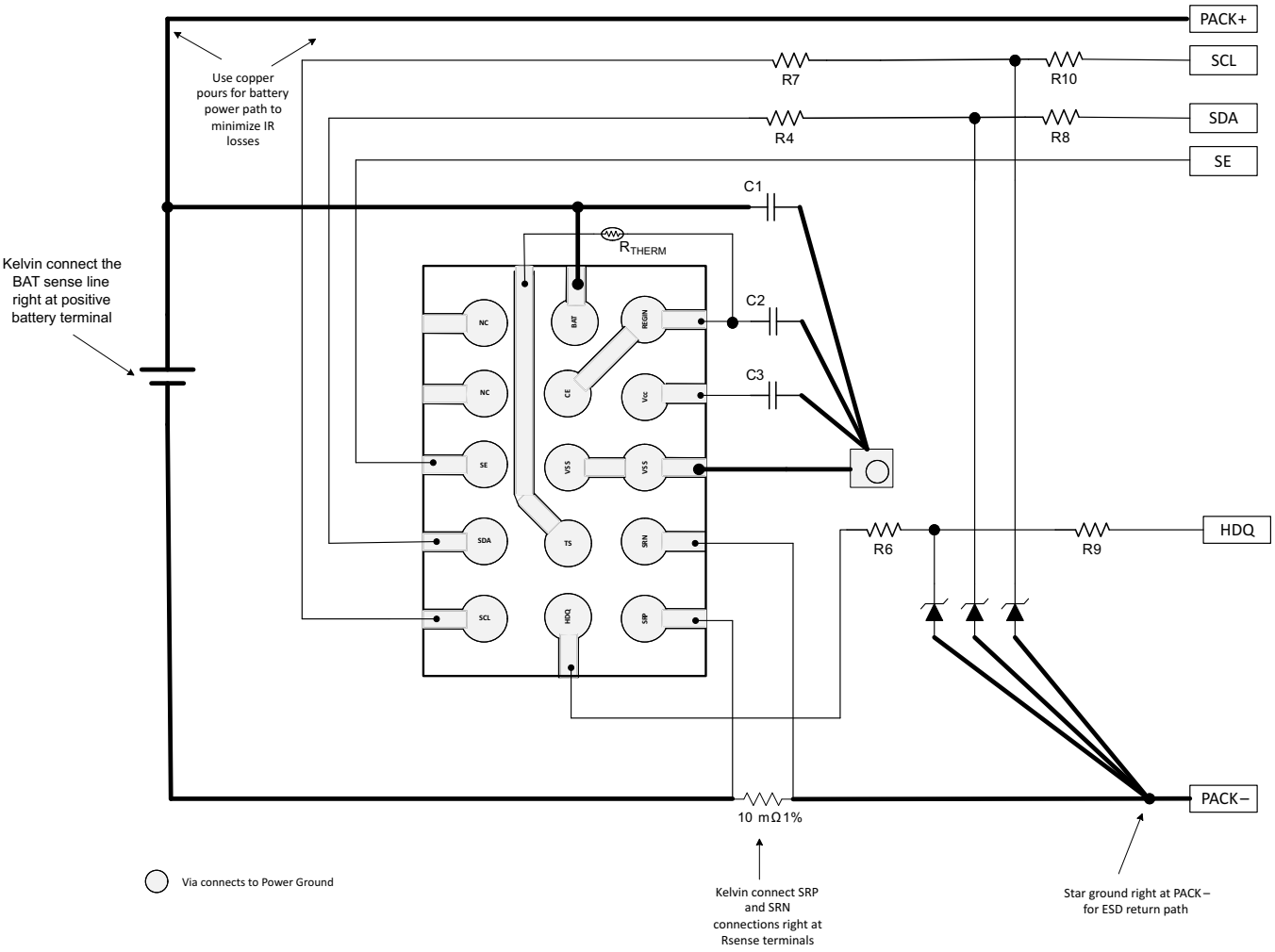


Figure 15. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For more information, see *bq27546-G1 Technical Reference Manual* (SLUUB74).

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

Impedance Track, Nano-Free, E2E are trademarks of Texas Instruments.
I^2C is a trademark of NXP Semiconductors, N.V.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ27546YZFR-G1	ACTIVE	DSBGA	YZF	15	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27546	Samples
BQ27546YZFT-G1	ACTIVE	DSBGA	YZF	15	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27546	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

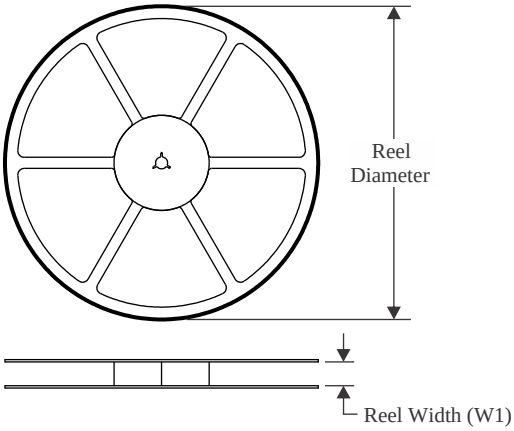
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

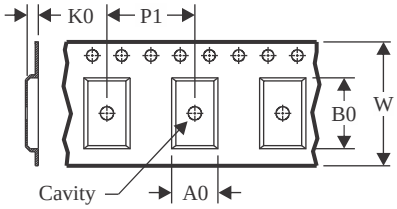
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

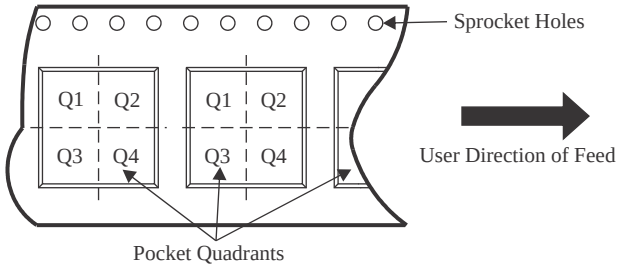


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

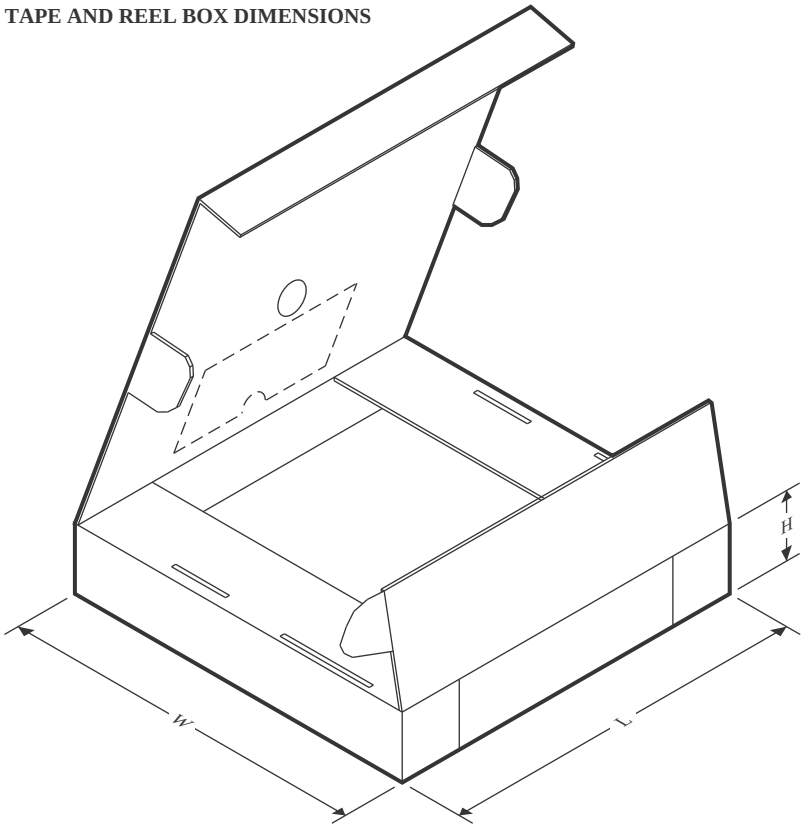
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27546YZFR-G1	DSBGA	YZF	15	3000	180.0	8.4	2.1	2.76	0.81	4.0	8.0	Q1
BQ27546YZFT-G1	DSBGA	YZF	15	250	180.0	8.4	2.1	2.76	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

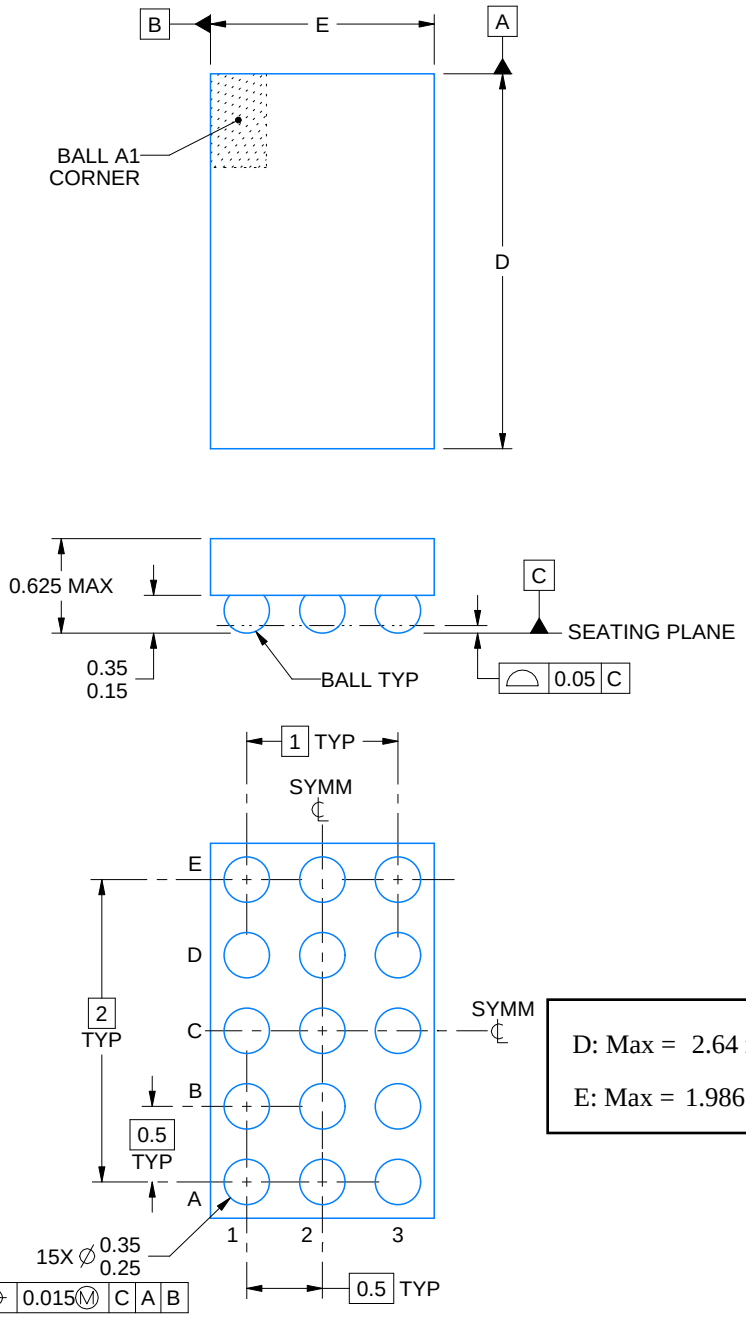
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27546YZFR-G1	DSBGA	YZF	15	3000	182.0	182.0	20.0
BQ27546YZFT-G1	DSBGA	YZF	15	250	182.0	182.0	20.0

PACKAGE OUTLINE

YZF0015

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY

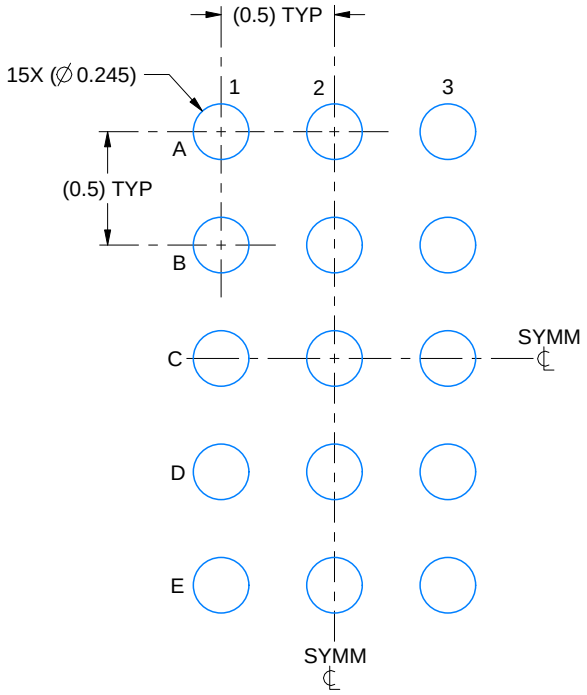


4219381/A 02/2017

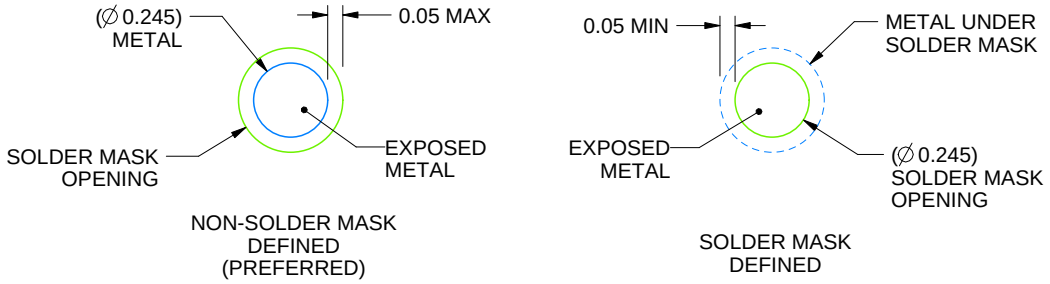
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219381/A 02/2017

NOTES: (continued)

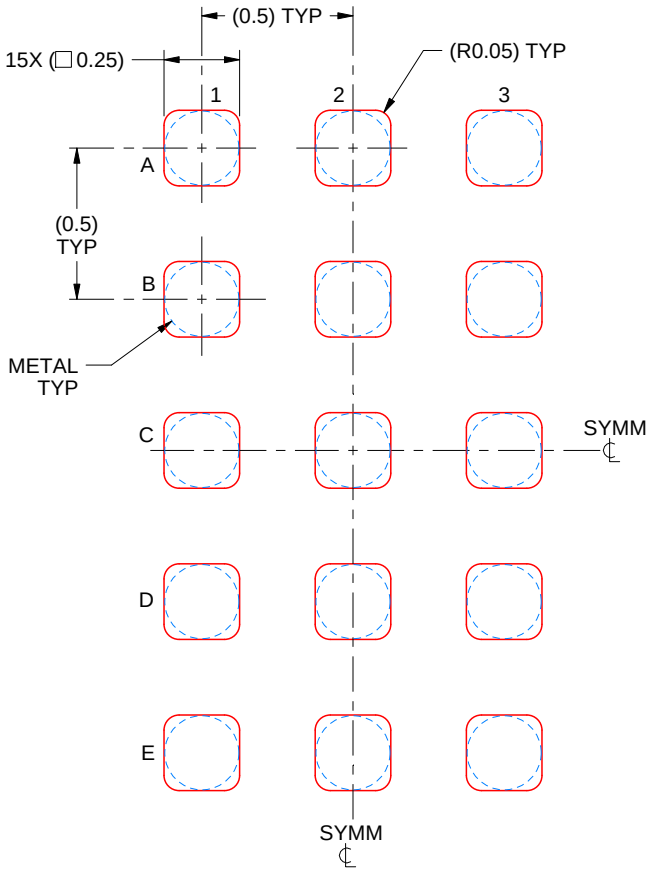
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZF0015

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219381/A 02/2017

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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