TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS092C – Revised July 2003

CD4724B Types

CMOS
8-Bit Addressable Latch

High-Voltage Types (20-Volt Rating)

■ CD4724B 8-bit addressable latch is a serial-input, parallel-output storage register that can perform a variety of functions.

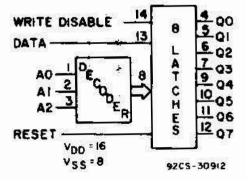
Data are inputted to a particular bit in the latch when that bit is addressed (by means of inputs A0, A1, A2) and when WRITE DISABLE is at a low level. When WRITE DISABLE is high, data entry is inhibited; however, all 8 outputs can be continuously read independent of WRITE DISABLE and address inputs.

A master RESET input is available, which resets all bits to a logic "0" level when RESET and WRITE DISABLE are at a high level. When RESET is at a high level, and WRITE DISABLE is at a low level, the latch acts as a 1-of-8 demultiplexer; the bit that is addressed has an active output which follows the data input, while all unaddressed bits are held to a logic "0" level.

The CD4724B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Feature

- **Serial data input** ■ **Active parallel output**
- **Storage register capability** ■ **Master clear**
- **Can function as demultiplexer**
- **Standardized, symmetrical output characteristics**
- **100% tested for quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V (full package-temperature range), 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range) = 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

Applications:

- **Multi-line decoders**
- **A/D converters**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) Voltages referenced to V_{SS} Terminal)	−0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −55°C to +100°C	500mW
For T_A = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T_A)	−55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

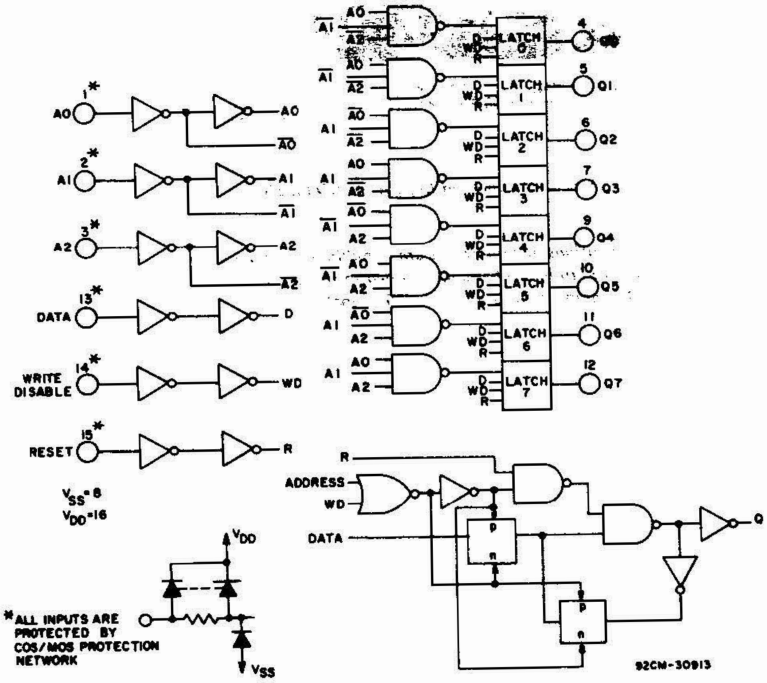
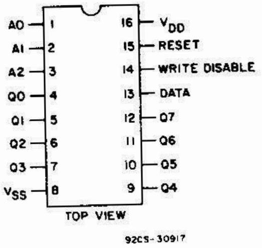


Fig. 1— Logic diagram of CD4724B and detail of 1 of 8 latches.



TERMINAL ASSIGNMENT

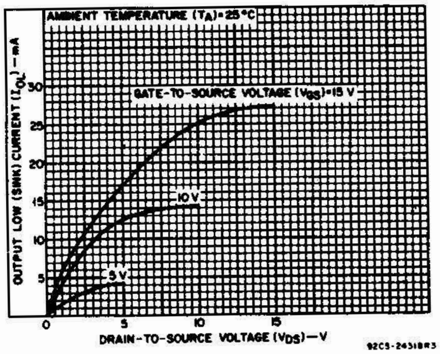


Fig. 2— Typical output low (sink) current characteristics.

RECOMMENDED OPERATING CONDITIONS *at $T_A = 25°$ C (Unless otherwise specified)*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	SEE FIG. 15*	V_{DD} (V)	LIMITS		UNITS
			MIN.	MAX.	
Supply Voltage Range: (At T_A = Full Package Temperature Range)			3	18	V
Pulse Width, t_W Data	④	5	200	–	ns
		10	100	–	
		15	80		
Address	⑧	5	400	–	
		10	200	–	
		15	125	–	
Reset	⑤	5	150	–	
		10	75	–	
		15	50	–	
Setup Time, t_S Data to WRITE DISABLE	⑥	5	100	–	ns
		10	50	–	
		15	35	–	
Hold Time, t_H Data to WRITE DISABLE	⑦	5	150	–	ns
		10	75	–	
		15	50	–	

* Circled numbers refer to times indicated on master timing diagram.

Note: In addition to the above characteristics, a WRITE DISABLE ON time (the time that WRITE DISABLE is at a high level) must be observed during an address change for the total time that the external address lines A0, A1, and A2 are settling to a stable level, to prevent a wrong cell from being addressed.

MODE SELECTION			
WD	R	ADDRESSED LATCH	UNADDRESSED LATCH
0	0	Follows Data	Holds Previous State
0	1	Follows Data (Active High 8-Channel Demultiplexer)	Reset to "0"
1	0	Holds Previous State	
1	1	Reset to "0"	Reset to "0"

WD = WRITE DISABLE R = RESET

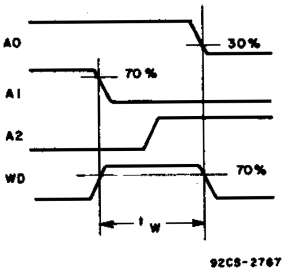


Fig. 3— Definition of WRITE DISABLE ON time.

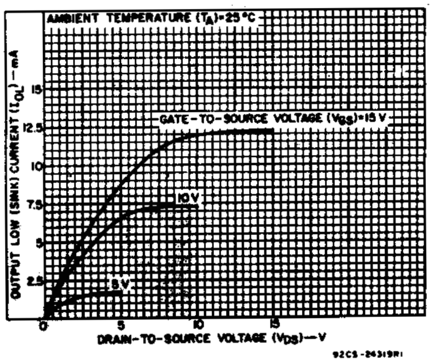


Fig. 4— Minimum output low (sink) current characteristics.

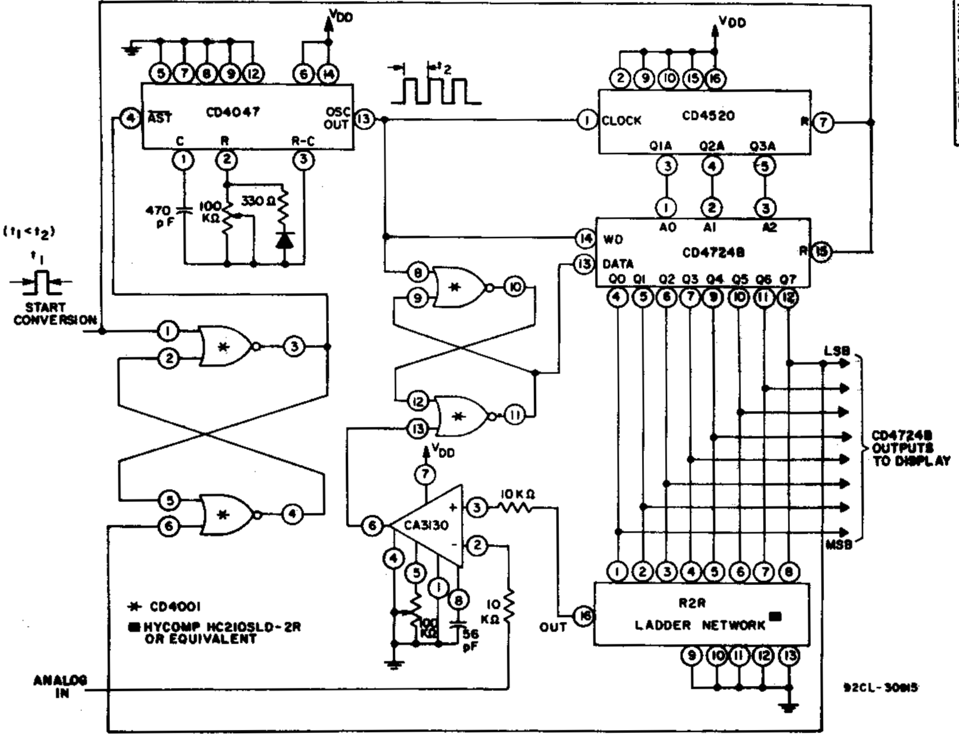


Fig. 5— A/D converter

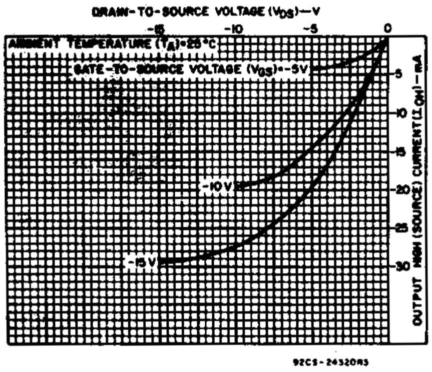


Fig.6 — Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	μA

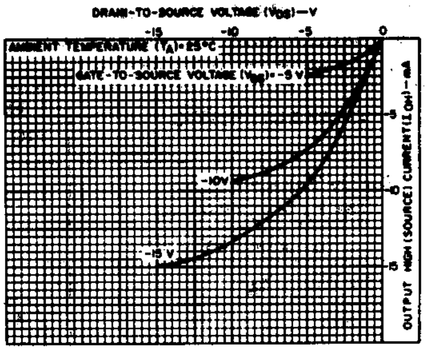


Fig.7 – Minimum output high (source) current characteristics.

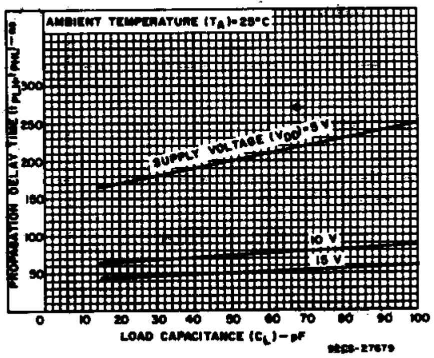


Fig. 8 – Typical propagation delay time (data to Qn) vs. load capacitance.

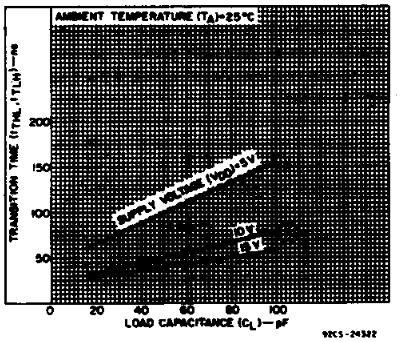


Fig. 9 – Typical transition time vs. load capacitance.

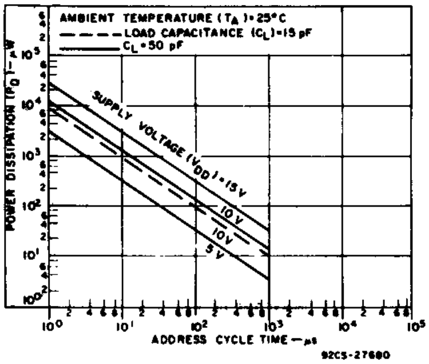
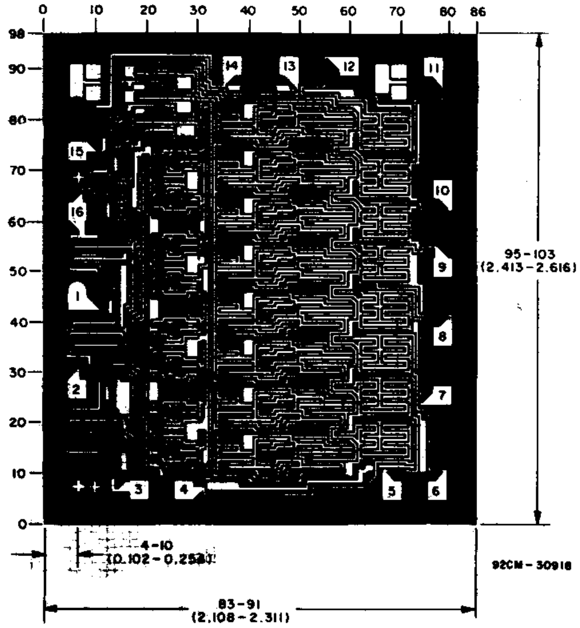


Fig.10 – Typical dynamic power dissipation vs. address cycle time.



CD4724BH
DIMENSIONS AND PAD LAYOUT

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

DYNAMIC ELECTRICAL CHARACTERISTICS *at $T_A = 25^\circ C$, $C_L = 50 pF$, Input t_r, $t_f = 20 ns$, $R_L = 200 K\Omega$*

CHARACTERISTIC	CONDITIONS		LIMITS ALL PACKAGE TYPES		UNITS
	SEE Fig. 15*	V_{DD} (V)	TYP.	MAX.	
Propagation Delay: t_{PLH}, t_{PHL} Data to Output,	①	5	200	400	ns
		10	75	150	
		15	50	100	
WRITE DISABLE to Output, t_{PLH}, t_{PHL}	②	5	200	400	
		10	80	160	
		15	60	120	
Reset to Output, t_{PHL}	③	5	175	350	
		10	80	160	
		15	65	130	
Address to Output, t_{PLH} t_{PHL}	⑨	5	225	450	
		10	100	200	
		15	75	150	
Transition Time, t_{THL} (Any Output) t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Minimum Pulse Width, t_W Data	④	5	100	200	ns
		10	50	100	
		15	40	80	
Address	⑧	5	200	400	ns
		10	100	200	
		15	65	125	
Reset	⑤	5	75	150	ns
		10	40	75	
		15	25	50	
Minimum Setup Time, t_S Data to WRITE DISABLE	⑥	5	50	100	ns
		10	25	50	
		15	20	35	
Minimum Hold Time, t_H Data to WRITE DISABLE	⑦	5	75	150	ns
		10	40	75	
		15	25	50	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

*Circled numbers refer to times indicated on master timing diagram.

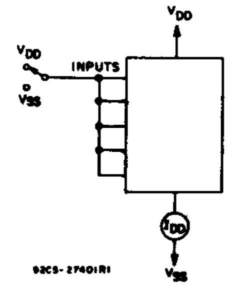


Fig. 11— Quiescent device current test circuit.

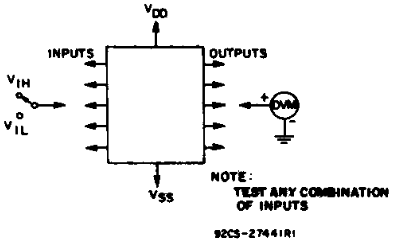


Fig. 12— Input voltage test circuit.

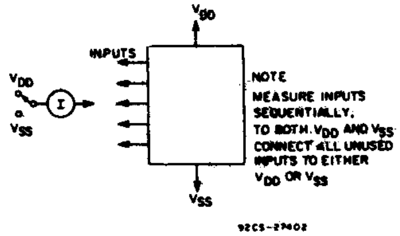


Fig. 13— Input current test circuit.

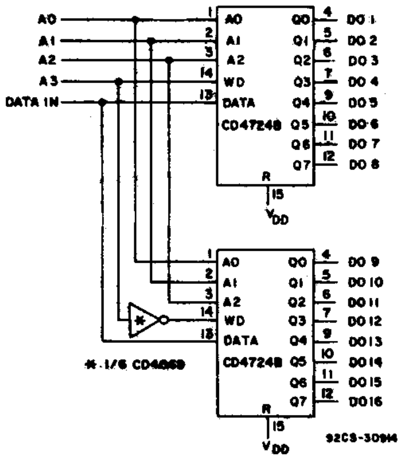


Fig. 14— 1 of 16 decoder/demultiplexer.

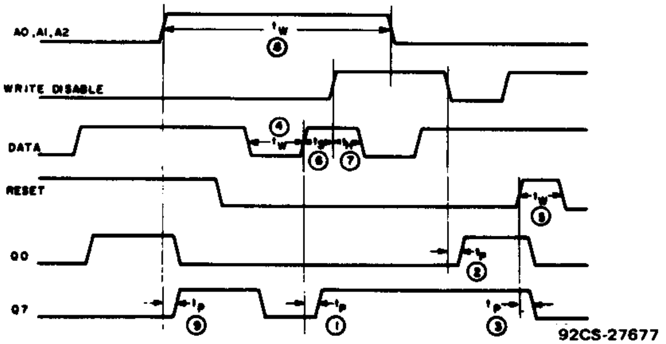


Fig. 15— Master timing diagram.

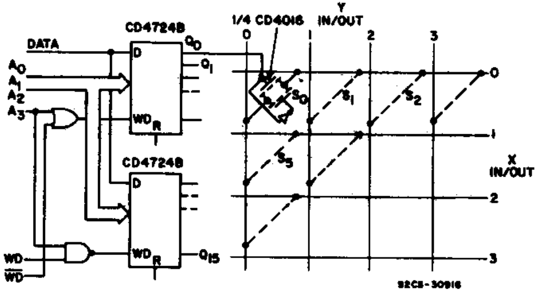


Fig 16— Multiple selection decoding – 4 x 4 crosspoint switch.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4724BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4724BE	Samples
CD4724BF3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4724BF3A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4724B, CD4724B-MIL :

- Catalog : CD4724B

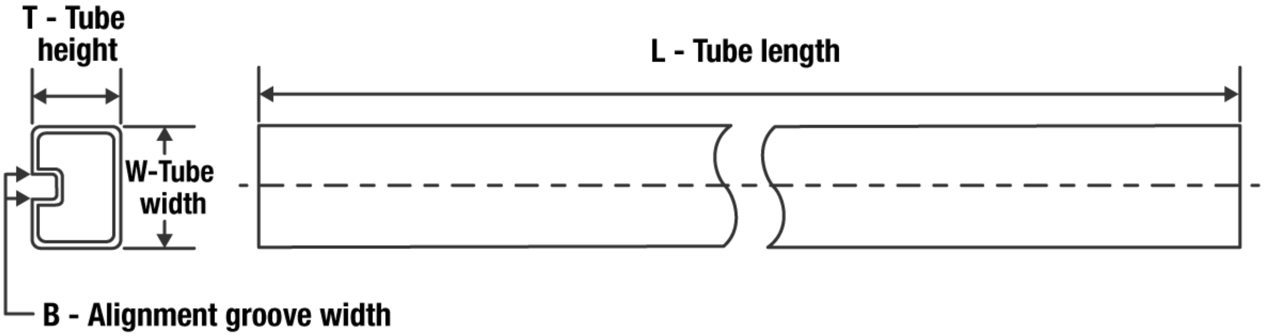
- Military : CD4724B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TUBE



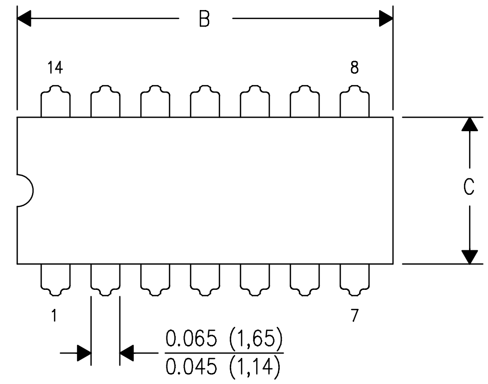
*All dimensions are nominal

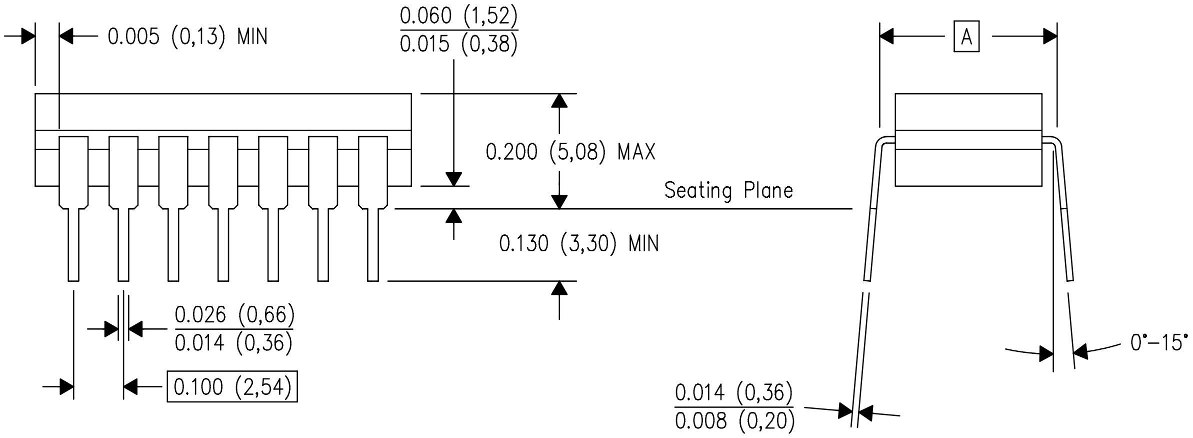
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4724BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4724BE	N	PDIP	16	25	506	13.97	11230	4.32

J (R-GDIP-T**) CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)





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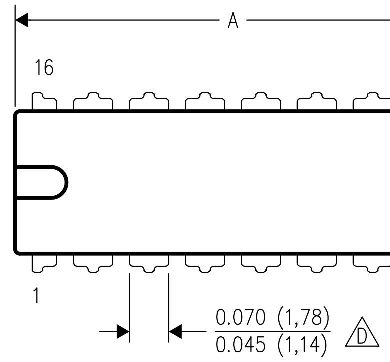
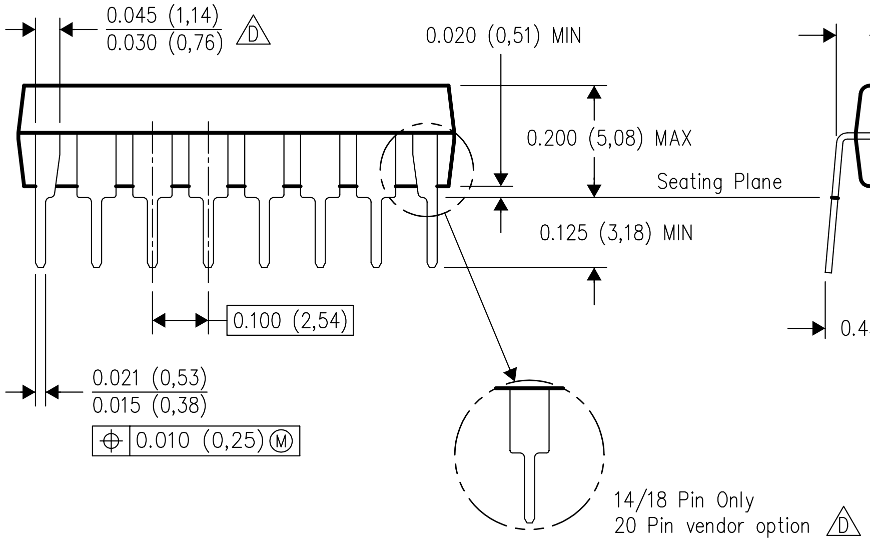
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

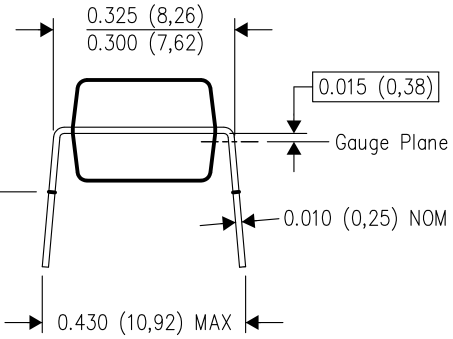
N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD





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NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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