CDx4AC299, CD74AC323, CDx4ACT299 8-Lnput Universal Shift/Storage Register with Common Parallel I/O Pins

1 Features

Type Features

- Buffered inputs
- Typical propagation delay:

  6ns @ V_{CC} = 5V, T_A = 25°C, C_L = 50pF

Family Features

- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ± 24mA output drive current
  - Fanout to 15 FAST* ICs
  - Drives 50ohm transmission lines

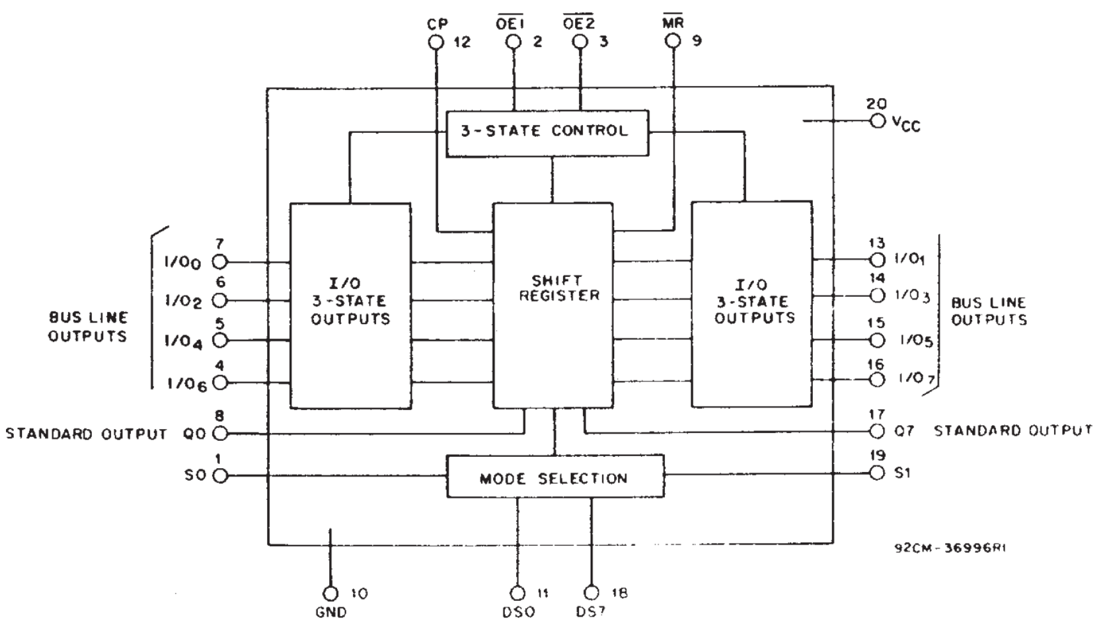
2 Description

The RCA CDx4AC299 and CD74AC323 and the CDx4ACT299 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
CDx4AC(T)299/ CD74AC323	DW (SOIC, 20)	12.80mm × 10.3mm	12.80mm × 7.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



Functional Diagram

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

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3 Pin Configuration and Functions

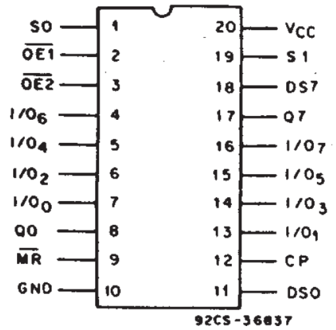

Figure 3-1. Terminal Assignment

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	SO	I	Mode select 0
2	!OE1	I	Output enable, active low
3	!OE2	I	Output enable, active low
4	I/O6	O	Parallel data input/output
5	I/O4	O	Parallel data input/output
6	I/O2	O	Parallel data input/output
7	I/O0	O	Parallel data input/output
8	Q0	O	Serial output
9	!MR	I	Master reset, active low
10	GND	-	Ground
11	DSO	I	Serial data input
12	CP	I	Clock, rising edge triggered
13	I/O1	O	Parallel data input/output
14	I/O3	O	Parallel data input/output
15	I/O5	O	Parallel data input/output
16	I/O7	O	Parallel data input/output
17	Q7	O	Serial output
18	DS7	I	Serial data input
19	S1	I	Mode select
20	V_{CC}	-	Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

4 Specifications

4.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
I_{IK}	Input diode current	(V_I < -0.5 V or V_I > V_{CC} ± 0.5 V)		±20	mA
I_{OK}	Output diode current	(V_O < -0.5 V or V_O > V_{CC} + 0.5 V)		±50	mA
I_O	Output source or sink current per output pin	(V_O > -0.5 V or V_O < V_{CC} + 0.5 V)		±50	mA
	V_{CC} or ground current, I_{CC} or I_{GND}			±100	mA [(1)]
T_A	Operating-temperature range		-55	+125	°C
T_{stg}	Storage temperature		-65	+150	°C

(1) For up to 4 outputs per device; add ± 25 mA for each additional output.

4.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

		MIN	MAX	UNIT
V_{CC} [(1)]	Supply-Voltage : (For T_A = Full Package-Temperature Range)			
	AC Types	1.5	5.5	V
	ACT Types	4.5	5.5	V
V_I, V_O	Input or Output voltage	0	V_{CC}	V
T_A	Operating Temperature	-55	+125	°C
dt/dv	Input Rise and Fall Slew Rate			
	at 1.5 V to 3 V (AC Types)	0	50	ns/V
	at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
	at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

(1) Unless otherwise specified, all voltages are referenced to ground.

4.4 Thermal Information

THERMAL METRIC[(1)]		CDx4AC(T)299/ CD74AC323	UNIT
		DW (SOIC, 20)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

4.5 Static Electrical Characteristics, AC Series

CHARACTERISTICS		TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNIT
		V_I (V)	I_O (mA)		+25 MIN	+25 MAX	-40 to+85 MIN	-40 to+85 MAX	-55 to +125 MIN	-55 to +125 MAX	
V_{IH}	High-Level Input Voltage			1.5	1.2	—	1.2	—	1.2	—	V
				3	2.1	—	2.1	—	2.1	—	
				5.5	3.85	—	3.85	—	3.85	—	
V_{IL}	Low-Level Input Voltage			1 5	—	0.3	—	0.3	—	0.3	V
				3	—	0.9	—	0.9	—	0.9	
				5.5	—	1.65	—	1.65	—	1.65	
V_{OH}	High-Level Output Voltage	V_{IH} or V_{IL}	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
		[1], [2]	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
V_{OL}	Low-Level Output Voltage	V_{IH} or V_{IL}	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
		[1], [2]	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
I_I	Input Leakage Current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
I_{OZ}	3-Stage Leakage Current	V_{IH} or V_{IL} V_O= V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA
Ice	Quiescent Supply Current, MSI	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

4.6 Static Electrical Characteristics, ACT Series

CHARACTERISTICS		TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C +25 MIN	+25 MAX	-40 to +85 MIN	-40 to +85 MAX	-55 to +125 MIN	-55 to +125 MAX	UNIT
V_{IH}	High-Level Input Voltage			4.5 to 5.5	2	—	2	—	2	—	V
V_{IL}	Low-Level Input Voltage			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V
V_{OH}	High-Level Output Voltage	V_{IH} or V_{IL}	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
		[1], [2]	-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
V_{OL}	Low-Level Output Voltage	V_{IH} or V_{IL}	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
		[1], [2]	75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
I_I	Input Leakage Current	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	µA
I_{OZ}	3-State Leakage Current	V_{IH} or V_{IL} V_O V_{CC} or GND		5.5	—	±0.5	—	±5	—	±10	µA
I_{CC}	Quiescent Supply Current, MSI	V_{CC} or GND	0	5.5	—	8	—	80	—	160	µA
	Additional Quiescent Supply Current per Input Pin	V_{CC}-2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA
ΔI_{CC}	TTL Inputs High										
	1 Unit Load										

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at + 125°C.

Table 4-1. Act Input Loading Table

INPUT	UNIT LOADS [1] 299	UNIT LOADS [1] 323
S1.S0, $\overline{OE1}$, $\overline{OE2}$	0.83	0.83
I/O_0 - I/O_7, CP, DS0, DS7	0.67	067
$\overline{MR}$	1.33	067

(1) Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

4.7 Switching Characteristics, AC Series

t_r, t_f = 3 ns, C_L = 50 pF

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C -40 to +85 MIN	-40 to +85 MAX	-55 to +125 MIN	-55 to +125 MAX	UNIT
t_{PLH} t_{PHL}	Propagation Delays: CP to Q0, Q7	1.5	—	147	—	162	ns
		3.3 [(1)]	4.7	16.5	4.5	18.1	
		5 [(2)]	3.3	11.7	3.2	12.9	
t_{PLH} t_{PHL}	CP to (I/O)n	1.5	—	154	—	169	ns
		3.3	4.9	17.2	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
t_{PLH} t_{PHL}	$\overline{MR}$ to Q0, Q7 (299 only)	1.5	—	127	—	140	ns
		3.3	4	14.3	3.9	15.7	
		5	2.9	10.2	2.8	11.2	
t_{PLH} t_{PHL}	$\overline{MR}$ to (I/O)n	1.5	—	158	—	174	ns
		3.3	5	17.7	4.9	19.5	
		5	3.6	12.6	3.5	13.9	
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Enable and Disable Times	1.5		169		186	ns
		3.3	5.8	20.4	5.6	22.4	
		5	3.8	13.5	3.7	14.9	
C_{pd} [(3)]	Power Dissipation Capacitance	—	280 Typ.		280 Typ.		pF
C_I	Input Capacitance	—	—	10	—	10	pF
C_O	3-State Output Capacitance	—	—	15	—	15	pF

(1) 3.3 V: min. is @ 3.6 V
(2) 5 V: min. is @ 5.5 V
(3) C_{pd} is used to determine the dynamic power consumption, per function.

4.8 Switching Characteristics, ACT Series

t_r, t_f = 3 ns, C_L = 50 pF

SYMBOL	CHARACTERISTICS	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C -40 to +85 MIN	-40 to +85 MAX	-55 to +125 MIN	-55 to +125 MAX	UNIT
t_{PLH} t_{PHL}	Propagation Delays: CP to Q0, Q7	5[(1)]	3.3	11.7	3.2	12.9	ns
t_{PLH} t_{PHL}	CP to (I/O)n	5	3.7	13.2	3.6	14.5	ns
t_{PLH} t_{PHL}	$\overline{MR}$ to Q0, Q7 (299 only)	5	3.1	11.1	3.1	12.2	ns
t_{PLH} t_{PHL}	$\overline{MR}$ to (I/O)n	5	4.8	16.9	4.7	18.6	ns
t_{PLZ} t_{PHZ} t_{PZL} t_{PZH}	Enable and Disable Times	5	3.8	13.5	3.7	14.9	ns
C_{PD}§	Power Dissipation Capacitance	—	280 Typ.		280 Typ.		pF
C_I	Input Capacitance	—	—	10	—	10	pF
C_O	3-State Output Capacitance	—	—	15	—	15	pF

(1) 5 V: min. is @ 5.5 V

5 Parameter Measurement Information

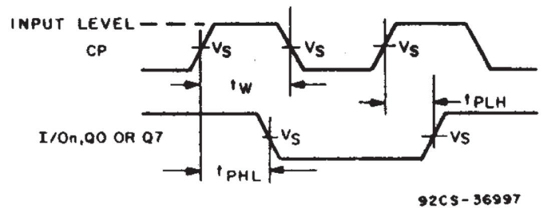

Figure 5-1. Clock Prerequisite and Propagation Delays

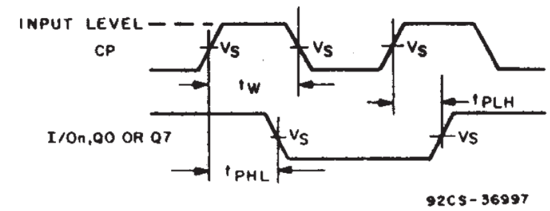

Figure 5-2. Clock Prerequisite and Propagation Delays

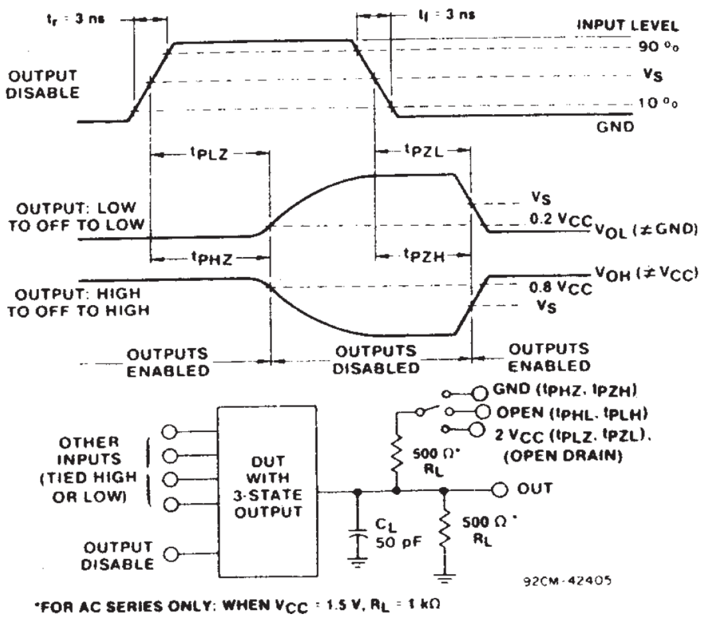

Figure 5-3. Three-state Propagation Delay Times and Test Circuit

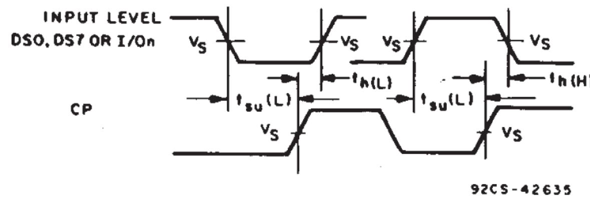

Figure 5-4. Data Prerequisite Times

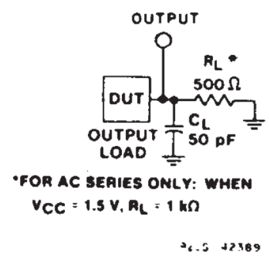

Figure 5-5. Test Circuit

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	0.5 V_{CC}	1.5 V
Output Switching Voltage, V_S	0.5 V_{CC}	0.5 V_{CC}

6 Detailed Description

6.1 Overview

The RCA CD54/74AC299 and CD54/74AC323 and the CD54/74ACT299 and CD54/74ACT323 are 3-state, 8-input universal shift/storage registers with common parallel I/O pins. These devices use the RCA ADVANCED CMOS technology. These registers have four synchronous-operating modes controlled by the two select inputs as shown in the Mode Select (S0, S1) table. The Mode Select, the Serial Data (DSO, DS7), and the Parallel Data (I/O_0 - I/O_7) respond only to the LOW-TO-HIGH transition of the clock (CP) pulse. S0, S1 and Data inputs must be present one setup time prior to the positive transition of the clock.

With the CD54/74AC/ACT299, the Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When $\overline{MR}$ is LOW, the register is cleared regardless of the status of all other inputs With the CD54/74AC/ACT323, the Master Reset ($\overline{MR}$) clears the register in sync with the clock input. The register can be expanded by cascading same units by tying the serial output (QO) to the serial data (DS7) input of the preceding register, and tying the serial output (Q7) to the serial data (DSO) input of the following register. Recirculating the (n x 8) bits is accomplished by tying the Q7 of the last stage to the DSO of the first stage.

The 3-state input/output (I/O) port has three modes of operation:

1. Both Output Enable ($\overline{OE1}$ and $\overline{OE2}$) inputs are LOW and S0 or S1 or both are LOW; the data in the register is present at the eight outputs.
2. When both S0 and S1 are HIGH, I/O terminals are in the high-impedance state but being input ports, ready for parallel data to be loaded into eight registers with one clock transition regardless of the status of $\overline{OE1}$ and $\overline{OE2}$.
3. Either one of the two Output Enable inputs being HIGH will force I/O terminals to be in the off state. It is noted that each I/O terminal is a 3-state output and a CMOS buffer input.

The CD74AC/ACT299 and CD74AC/ACT323 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85° C); and Extended Industrial/ Military (-55 to +125° C).

The CD54AC/ACT299 and CD54AC/ACT323, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

6.2 Functional Block Diagram

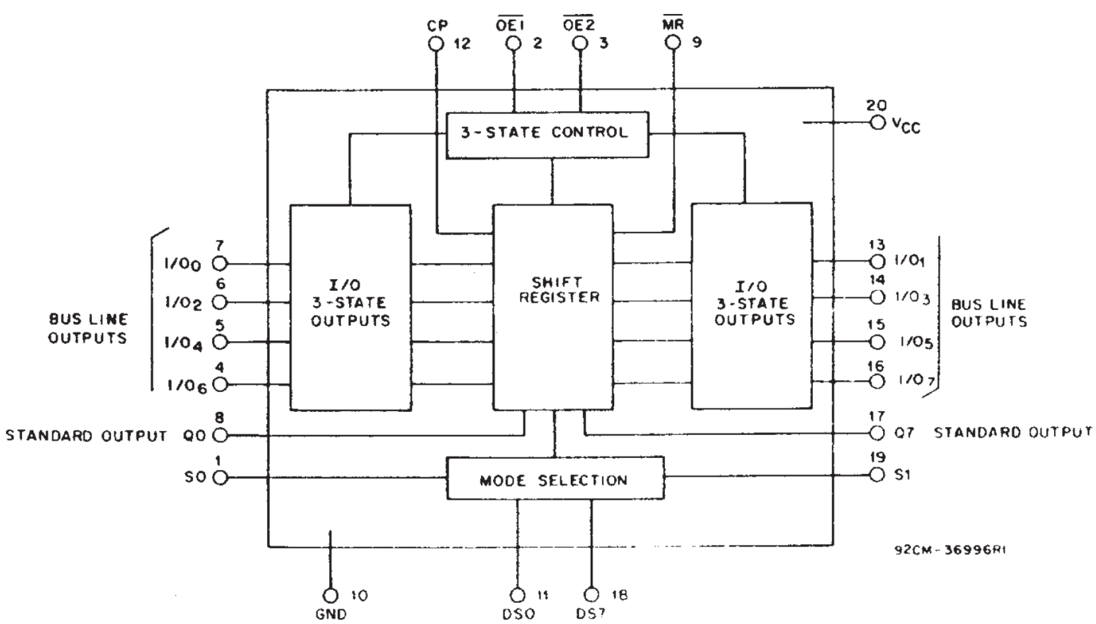

Figure 6-1. Functional Diagram

6.3 Device Functional Modes

FUNCTION	INPUTS							REGISTER OUTPUTS				
	$\overline{MR}$	CP	S0	S1	DS0	DS7	I/O_n	Q0	Q1	…	Q6	Q7
Reset (Clear)	L	X(1)	X	X	X	X	X	L	L	…	L	L
Shift Right	H	↑	h	l	l	X	X	L	q_0	…	q_5	q_6
	H	↑	h	l	h	X	X	H	q_0	…	q_5	q_6
Shift Left	H	↑	l	h	X	l	X	q_1	q_2	…	q_7	L
	H	↑	l	h	X	h	X	q_1	q_2	…	q_7	H
Hold (do nothing)	H	↑	l	l	X	X	X	q_0	q_1	…	q_6	q_7
Parallel Load	H	↑	h	h	X	X	l	L	L	…	L	L
	H	↑	h	h	X	X	h	H	H	…	H	H

Table 6-1. Mode Select

Function table 3-state I/O port operating mode

FUNCTION	INPUTS					INPUTS/OUTPUTS
	$\overline{OE1}$	$\overline{OE2}$	S0	S1	Qn (Register)	I/O_0 I/O_7
Read Register	L	L	L	X	L	L
	L	L	L	X	H	H
	L	L	X	L	L	L
	L	L	X	L	H	H
Load Register	X	X	H	H	Qn = I/O_n	I/O_n = Inputs
Disable I/O	H	X	X	X	X	(Z)
	X	H	X	X	X	(Z)

(1) H = Input voltage high level.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1μF and 1μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

- Bypass capacitor placement
  - Place near the positive supply terminal of the device
  - Provide an electrically short ground return path
  - Use wide traces to minimize impedance
  - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
  - 8mil to 12mil trace width
  - Lengths less than 12cm to minimize transmission line effects
  - Avoid 90° corners for signal traces
  - Use an unbroken ground plane below signal traces
  - Flood fill areas around signal traces with ground
  - For traces longer than 12cm
    - Use impedance controlled traces
    - Source-terminate using a series damping resistor near the output
    - Avoid branches; buffer signals that must branch separately

7.2.2 Layout Example

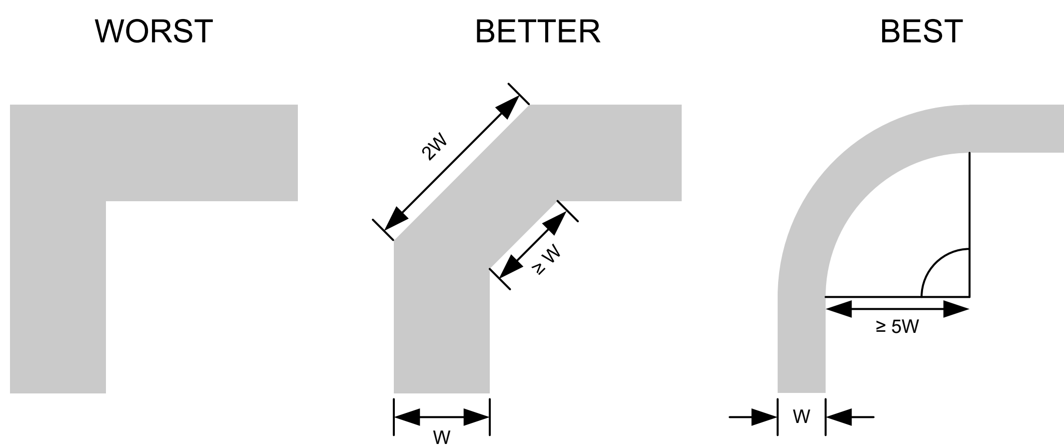

Figure 7-1. Example Trace Corners for Improved Signal Integrity

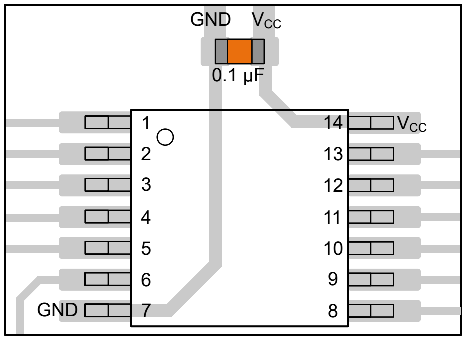

Figure 7-2. Example Bypass Capacitor Placement for TSSOP and Similar Packages

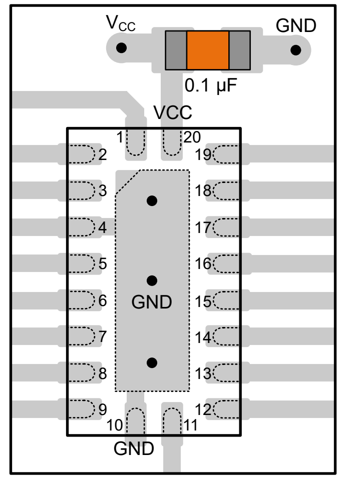

Figure 7-3. Example Bypass Capacitor Placement for WQFN and Similar Packages

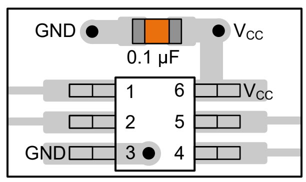

Figure 7-4. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

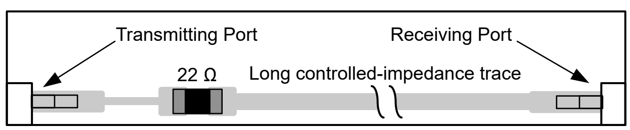

Figure 7-5. Example Damping Resistor Placement for Improved Signal Integrity

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC299	Click here	Click here	Click here	Click here	Click here
CD74AC299	Click here	Click here	Click here	Click here	Click here
CD54ACT299	Click here	Click here	Click here	Click here	Click here
CD74ACT299	Click here	Click here	Click here	Click here	Click here
CD74AC323	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2002) to Revision A (December 2024) **Page**

- Added *Applications* section, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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