# 2.5-V PHASE-LOCKED-LOOP CLOCK DRIVER

## FEATURES

- **Spread-Spectrum Clock Compatible**
- **Operating Frequency: 60 MHz to 220 MHz**
- **Low Jitter (Cycle-Cycle): ±35 ps**
- **Low Static Phase Offset: ±50 ps**
- **Low Jitter (Period): ±30 ps**
- **1-to-10 Differential Clock Distribution (SSTL2)**
- **Best in Class for $V_{OX} = V_{DD}/2 \pm 0.1$ V**
- **Operates From Dual 2.6-V or 2.5-V Supplies**
- **Available in a 40-Pin MLF Package, 48-Pin TSSOP Package, 56-Ball MicroStar Junior™ BGA Package**
- **Consumes < 100-μA Quiescent Current**
- **External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**
- **Meets/Exceeds JEDEC Standard (JESD82-1) For DDRI-200/266/333 Specification**
- **Meets/Exceeds Proposed DDRI-400 Specification (JESD82-1A)**
- **Enters Low-Power Mode When No CLK Input Signal Is Applied or PWRDWN Is Low**

## APPLICATIONS

- **DDR Memory Modules (DDR400/333/266/200)**
- **Zero-Delay Fan-Out Buffer**

## DESCRIPTION

The CDCVF857 is a high-performance, low-skew, low-jitter, zero-delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to 10 differential pairs of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AVDD). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to a high-impedance state (3-state) and the PLL is shut down (low-power mode). The device also enters this low-power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit detects the low frequency condition and, after applying a >20-MHz input signal, this detection circuit turns the PLL on and enables the outputs.

When $AV_{DD}$ is strapped low, the PLL is turned off and bypassed for test purposes. The CDCVF857 is also able to track spread spectrum clocking for reduced EMI.

Because the CDCVF857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCVF857 is characterized for both commercial and industrial temperature ranges.

## AVAILABLE OPTIONS

| $T_A$ | TSSOP (DGG) | 40-Pin MLF | 56-Ball BGA[1] |
|---|---|---|---|
| −40°C to 85°C | CDCVF857DGG | CDCVF857RTB | CDCVF857GQL |
| −40°C to 85°C | | CDCVF857RHA | CDCVF857ZQL |

(1) Maximum load recommended is 12 pf for 200 MHz. At 12-pf load, maximum $T_A$ allowed is 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

MicroStar Junior is a trademark of Texas Instruments.
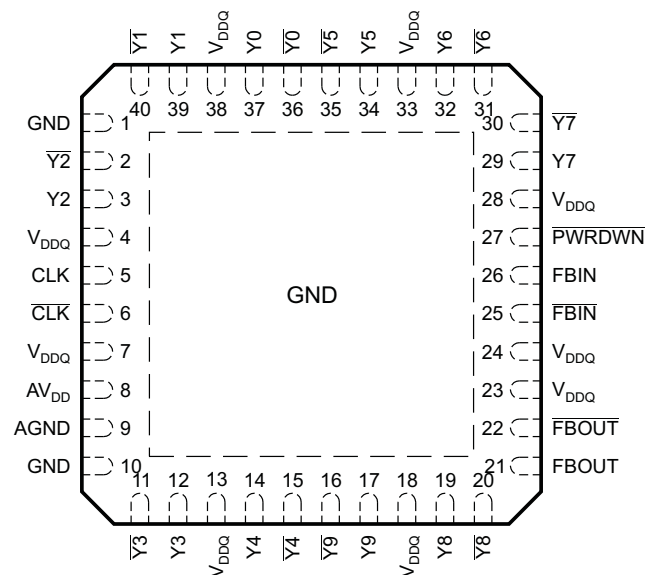
## FUNCTION TABLE
### (Select Functions)

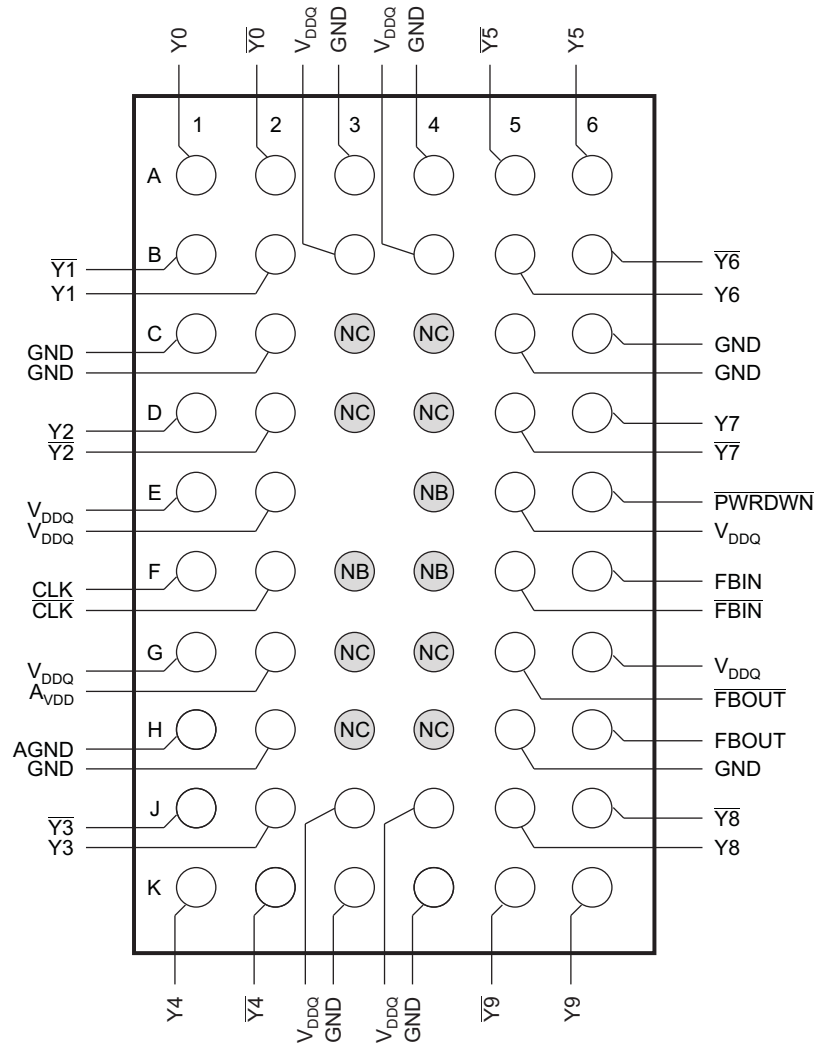| INPUTS | | | | OUTPUTS | | | | PLL |
|---|---|---|---|---|---|---|---|---|
| AVDD | $\overline{\text{PWRDWN}}$ | CLK | $\overline{\text{CLK}}$ | Y[0:9] | $\overline{\text{Y[0:9]}}$ | FBOUT | $\overline{\text{FBOUT}}$ | |
| GND | H | L | H | L | H | L | H | Bypassed/off |
| GND | H | H | L | H | L | H | L | Bypassed/off |
| X | L | L | H | Z | Z | Z | Z | Off |
| X | L | H | L | Z | Z | Z | Z | Off |
| 2.5 V (nom) | H | L | H | L | H | L | H | On |
| 2.5 V (nom) | H | H | L | H | L | H | L | On |
| 2.5 V (nom) | X | <20 MHz | <20 MHz | Z | Z | Z | Z | Off |



DGG PACKAGE
(TOP VIEW)
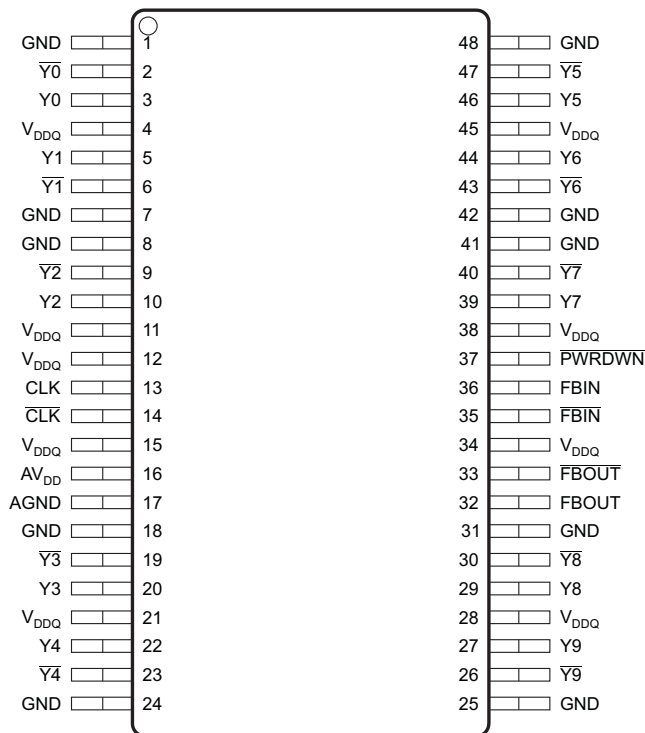
P0052-01



RHA/RTB PACKAGE
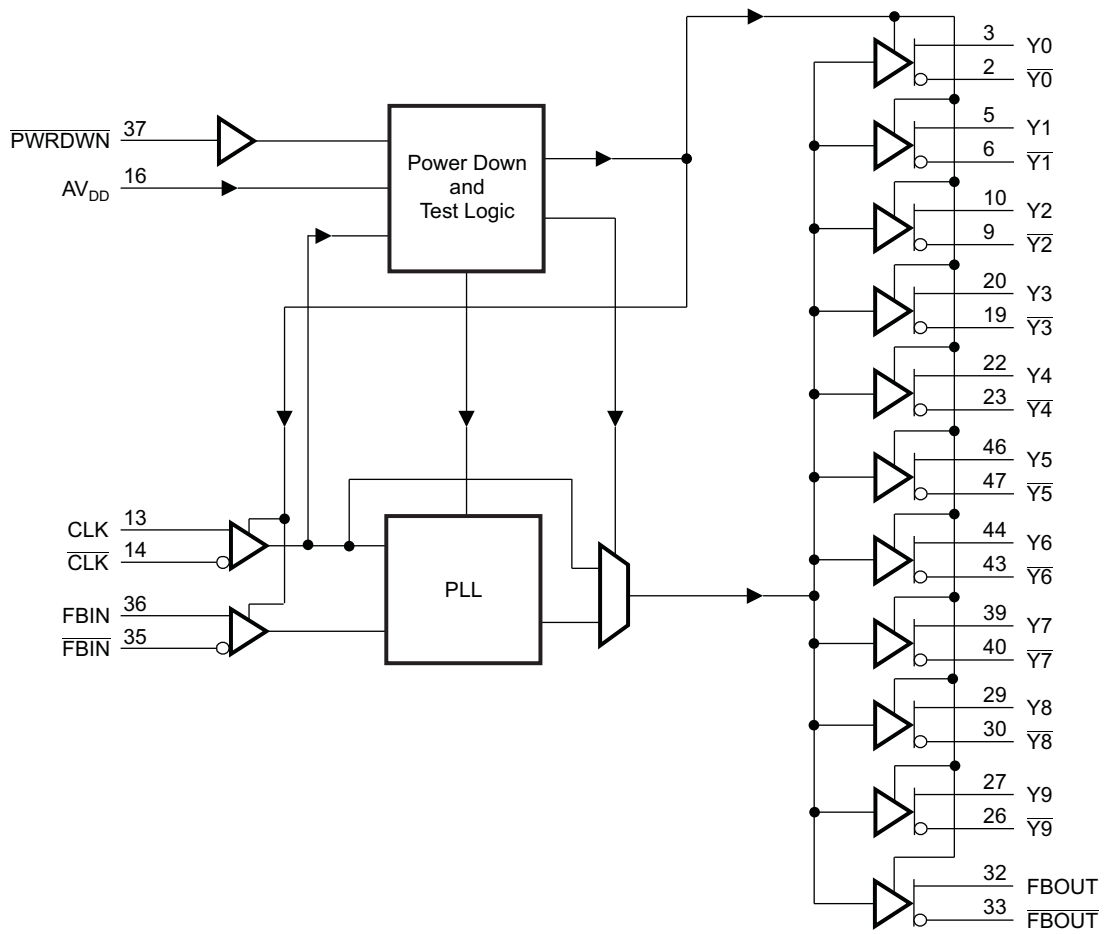(TOP VIEW)

P0053-01

MicroStar Junior™ BGA (GQL/ZQL) PACKAGE
(TOP VIEW)



NB = No Ball
NC = No Connection

P0054-01

## FUNCTIONAL BLOCK DIAGRAM



B0196-01

## Table 1. TERMINAL FUNCTIONS

| | TERMINAL | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | DGG | RHA/RTB | GQL/ZQL | | |
| AGND | 17 | 9 | H1 | – | Ground for 2.5-V analog supply |
| $AV_{DD}$ | 16 | 8 | G2 | – | 2.5-V analog supply |
| CLK, $\overline{CLK}$ | 13, 14 | 5, 6 | F1, F2 | I | Differential clock input |
| $\overline{FBIN}$, FBIN | 35, 36 | 25, 26 | F5, F6 | I | Feedback differential clock input |
| FBOUT, $\overline{FBOUT}$ | 32, 33 | 21, 22 | H6, G5 | O | Feedback differential clock output |
| GND | 1, 7, 8, 18, 24, 25, 31, 41, 42, 48 | 1, 10 | A3, A4, C1, C2, C5, C6, H2, H5, K3, K4 | – | Ground |
| $\overline{PWRDWN}$ | 37 | 27 | E6 | I | Output enable for Y and $\overline{Y}$ |
| $V_{DDQ}$ | 4, 11, 12, 15, 21, 28, 34, 38, 45 | 4, 7, 13, 18, 23, 24, 28, 33, 38 | B3, B4, E1, E2, E5, G1, G6, J3, J4 | – | 2.5-V supply |
| Y0, $\overline{Y0}$ | 3, 2 | 37, 36 | A1, A2 | O | |
| Y1, $\overline{Y1}$ | 5, 6 | 39, 40 | B2, B1 | O | |
| Y2, $\overline{Y2}$ | 10, 9 | 3, 2 | D1, D2 | O | |
| Y3, $\overline{Y3}$ | 20, 19 | 12,11 | J2, J1 | O | |
| Y4, $\overline{Y4}$ | 22, 23 | 14, 15 | K1, K2 | O | |
| Y5, $\overline{Y5}$ | 46, 47 | 34, 35 | A6, A5 | O | Buffered output copies of input clock, CLK, $\overline{CLK}$ |
| Y6, $\overline{Y6}$ | 44, 43 | 32, 31 | B5, B6 | O | |
| Y7, $\overline{Y7}$ | 39, 40 | 29, 30 | D6, D5 | O | |
| Y8, $\overline{Y8}$ | 29, 30 | 19, 20 | J5, J6 | O | |
| Y9, $\overline{Y9}$ | 27, 26 | 17, 16 | K6, K5 | O | |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1]

| | | | |
|---|---|---|---|
| $V_{DDQ}$, $AV_{DD}$ | Supply voltage range | | 0.5 V to 3.6 V |
| $V_I$ | Input voltage range[2][3] | | −0.5 V to $V_{DDQ}$ + 0.5 V |
| $V_O$ | Output voltage range[2][3] | | −0.5 V to $V_{DDQ}$ + 0.5 V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ or $V_I > V_{DDQ}$ | ±50 mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ or $V_O > V_{DDQ}$ | ±50 mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{DDQ}$ | ±50 mA |
| $I_{DDC}$ | Continuous current to GND or $V_{DDQ}$ | | ±100 mA |
| $T_{stg}$ | Storage temperature range | | −65°C to 150°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
(3) This value is limited to 3.6 V maximum.

## THERMAL CHARACTERISTICS

| $R_{\theta JA}$ for TSSOP (DGG) Package[1] | | | $R_{\theta JA}$ for MLF (RHA/RTB) Package | | $R_{\theta JA}$ for BGA (GQL/ZQL) Package[2] | |
|---|---|---|---|---|---|---|
| Airflow | Low K | High K | Airflow | With 4 Thermal Vias | Airflow | High K |
| 0 ft/min | 89.1°C/W | 70°C/W | 0 ft/min | 44.7°C/W | 0 ft/min | 132.2°C/W |
| 150 ft/min | 78.5°C/W | 65.3°C/W | 150 ft/min | | 150 ft/min | 126.4°C/W |

(1) The package thermal impedance is calculated in accordance with JESD 51.
(2) Connecting the NC-balls (C3, C4, D3, D4, G3, G4, H3, H4) to a ground plane improves the $\theta_{JA}$ to 114.8°C/W (0 airflow).

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## RECOMMENDED OPERATING CONDITIONS

| | | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Supply voltage | $V_{DDQ}$ | PC1600 – PC3200 | 2.3 | | 2.7 | V |
| | | AVDD | | $V_{DDQ}$ – 0.12 | | 2.7 | |
| $V_{IL}$ | Low-level input voltage | CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$ | | | | $V_{DDQ}$/2 – 0.18 | V |
| | | $\overline{PWRDWN}$ | | –0.3 | | 0.7 | |
| $V_{IH}$ | High-level input voltage | CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$ | | VDDQ/2 + 0.18 | | | V |
| | | $\overline{PWRDWN}$ | | 1.7 | | $V_{DDQ}$ + 0.3 | |
| | DC input signal voltage [1] | | | –0.3 | | $V_{DDQ}$ + 0.3 | V |
| $V_{ID}$ | Differential input signal voltage [2] | DC | CLK, FBIN | 0.36 | | $V_{DDQ}$ + 0.6 | V |
| | | AC | CLK, FBIN | 0.7 | | $V_{DDQ}$ + 0.6 | |
| $V_{IX}$ | Input differential pair cross voltage [3][4] | | | $V_{DDQ}$/2 – 0.2 | | $V_{DDQ}$/2 + 0.2 | V |
| $I_{OH}$ | High-level output current | | | | | –12 | mA |
| $I_{OL}$ | Low-level output current | | | | | 12 | mA |
| SR | Input slew rate | | | 1 | | 4 | V/ns |
| $T_A$ | Operating free-air temperature | | | –40 | | 85 | °C |

(1)  The unused inputs must be held high or low to prevent them from floating.
(2)  The dc input signal voltage specifies the allowable dc execution of the differential input.
(3)  The differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
(4)  The differential cross-point voltage tracks variations of $V_{CC}$ and is the voltage at which the differential signals must cross.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input voltage, all inputs | $V_{DDQ}$ = 2.3 V, $I_I$ = –18 mA | | | | –1.2 | V |
| $V_{OH}$ | High-level output voltage | $V_{DDQ}$ = min to max, $I_{OH}$ = –1 mA | | $V_{DDQ}$ – 0.1 | | | V |
| | | $V_{DDQ}$ = 2.3 V, $I_{OH}$ = –12 mA | | 1.7 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{DDQ}$ = min to max, $I_{OL}$ = 1 mA | | | | 0.1 | V |
| | | $V_{DDQ}$ = 2.3 V, $I_{OL}$ = 12 mA | | | | 0.6 | |
| $V_{OD}$ | Output voltage swing [2] | Differential outputs are terminated with 120 Ω, $C_L$ = 14 pF (see Figure 3) | | 1.1 | | $V_{DDQ}$ – 0.4 | V |
| $V_{OX}$ | Output differential cross-voltage [3] | | | $V_{DDQ}$/2 – 0.1 | $V_{DDQ}$/2 | $V_{DDQ}$/2 + 0.1 | V |
| $I_I$ | Input current | $V_{DDQ}$ = 2.7 V, $V_I$ = 0 V to 2.7 V | | | | ±10 | µA |
| $I_{OZ}$ | High-impedance-state output current | $V_{DDQ}$ = 2.7 V, $V_O$ = $V_{DDQ}$ or GND | | | | ±10 | µA |
| $I_{DDPD}$ | Power-down current on $V_{DDQ}$ + $AV_{DD}$ | CLK and $\overline{CLK}$ = 0 MHz; $\overline{PWRDWN}$ = Low; Σ of $I_{DD}$ and $AI_{DD}$ | | | 20 | 100 | µA |
| $AI_{DD}$ | Supply current on $AV_{DD}$ | $f_O$ = 170 MHz | | | 6 | 8 | mA |
| | | $f_O$ = 200 MHz | | | 8 | 10 | |
| $C_I$ | Input capacitance | $V_{DDQ}$ = 2.5 V, $V_I$ = $V_{DDQ}$ or GND | | 2 | 2.5 | 3.5 | pF |
| $I_{DD}$ | Dynamic current on $V_{DDQ}$ | Without load | $f_O$ = 170 MHz | | 120 | 140 | mA |
| | | | $f_O$ = 200 MHz | | 125 | 150 | |
| | | Differential outputs terminated with 120 Ω, $C_L$ = 0 pF | $f_O$ = 170 MHz | | 220 | 270 | |
| | | | $f_O$ = 200 MHz | | 230 | 280 | |
| | | Differential outputs terminated with 120 Ω, $C_L$ = 14 pF | $f_O$ = 170 MHz | | 280 | 330 | |
| | | | $f_O$ = 200 MHz | | 300 | 350 | |

(1)  All typical values are at nominal $V_{DDQ}$.
(2)  The differential output signal voltage specifies the differential voltage |VTR – VCP|, where VTR is the true output level and VCP is the complementary output level.
(3)  The differential cross-point voltage tracks variations of $V_{DDQ}$ and is the voltage at which the differential signals must cross.

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## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP [1] | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\Delta C$ | Part-to-part input capacitance variation | $V_{DDQ}$ = 2.5 V, $V_I$ = $V_{DDQ}$ or GND | | | 1 | pF |
| $C_{I(\Delta)}$ | Input capacitance difference between CLK and $\overline{CLK}$, FBIN, and $\overline{FBIN}$ | $V_{DDQ}$ = 2.5 V, $V_I$ = $V_{DDQ}$ or GND | | | 0.25 | pF |

## TIMING REQUIREMENTS

over recommended ranges of supply voltage and operating free-air temperature

| | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{CLK}$ | Operating clock frequency | 60 | 220 | MHz |
| | Application clock frequency | 90 | 220 | |
| | Input clock duty cycle | 40% | 60% | |
| | Stabilization time (PLL mode) [1] | | 10 | µs |
| | Stabilization time (bypass mode) [2] | | 30 | ns |

(1)  The time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK and $V_{DD}$ must be applied. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.
(2)  A recovery time is required when the device goes from power-down mode into bypass mode (AV$_{DD}$ at GND).

## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$[1] | Low-to-high level propagation delay time | Test mode/CLK to any output | | 3.5 | | ns |
| $t_{PHL}$[1] | High-to-low level propagation delay time | Test mode/CLK to any output | | 3.5 | | ns |
| $t_{jit(per)}$[2] | Jitter (period), see Figure 7 | 100 MHz (PC1600) | −65 | | 65 | ps |
| | | 133/167/200 MHz (PC2100/2700/3200) | −30 | | 30 | |
| $t_{jit(cc)}$[2] | Jitter (cycle-to-cycle), see Figure 4 | 100 MHz (PC1600) | −50 | | 50 | ps |
| | | 133/167/200 MHz (PC2100/2700/3200) | −35 | | 35 | |
| $t_{jit(hper)}$[2] | Half-period jitter, see Figure 8 | 100 MHz (PC1600) | −100 | | 100 | ps |
| | | 133/167/200 MHz (PC2100/2700/3200) | −75 | | 75 | |
| $t_{slr(o)}$ | Output clock slew rate, see Figure 9 | Load: 120 Ω, 14 pF | 1 | | 2 | V/ns |
| $t_{(\phi)}$ | Static phase offset, see Figure 5 | 100/133/167/200 MHz | −50 | | 50 | ps |
| $t_{sk(o)}$ | Output skew, see Figure 6 | Load: 120 Ω, 14 pF; 100/133/167/200 MHz | | | 40 | ps |

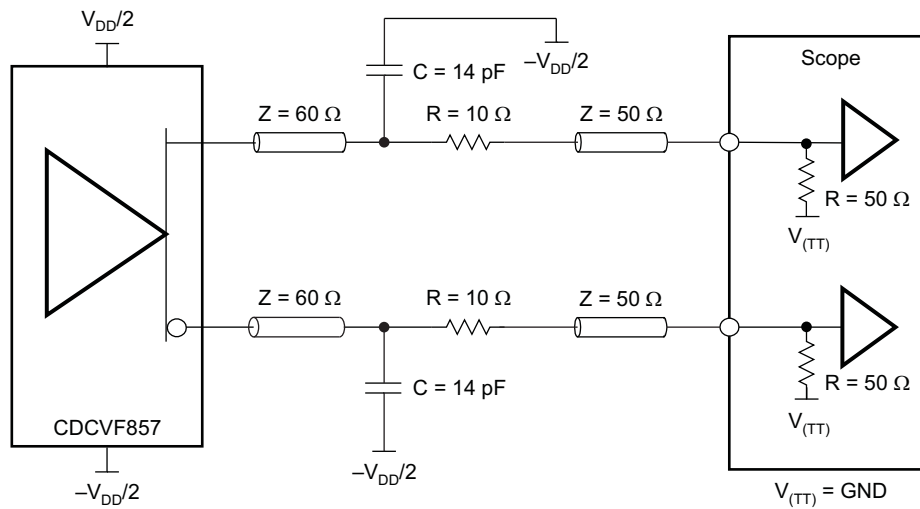(1)  Refers to the transition of the noninverting output.
(2)  This parameter is assured by design but cannot be 100% production tested.
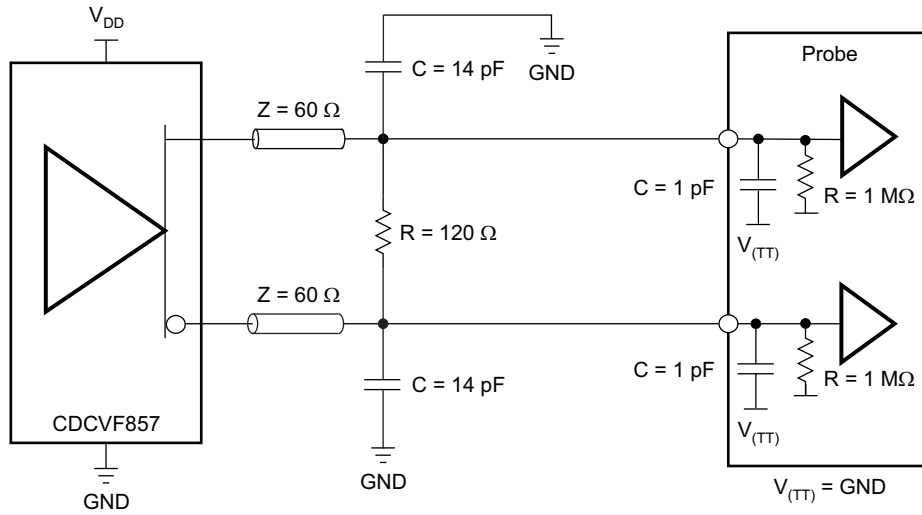
# PARAMETER MEASUREMENT INFORMATION
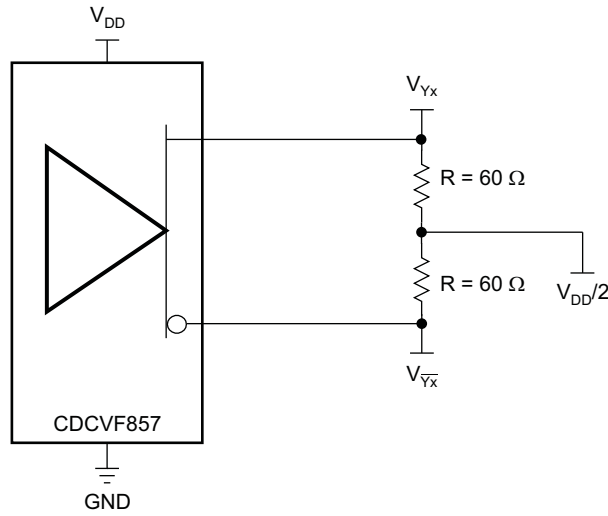


S0229-01

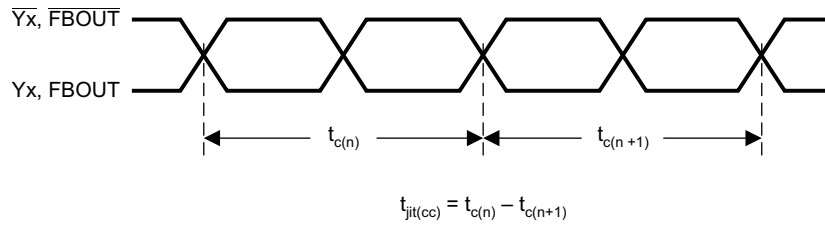**Figure 1. IBIS Model Output Load**



S0230-01

**Figure 2. Output Load Test Circuit**

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## PARAMETER MEASUREMENT INFORMATION (continued)



S0231-01

**Figure 3. Output Load Test Circuit for Crossing Point**



$$t_{jit(cc)} = t_{c(n)} - t_{c(n+1)}$$

T0174-01
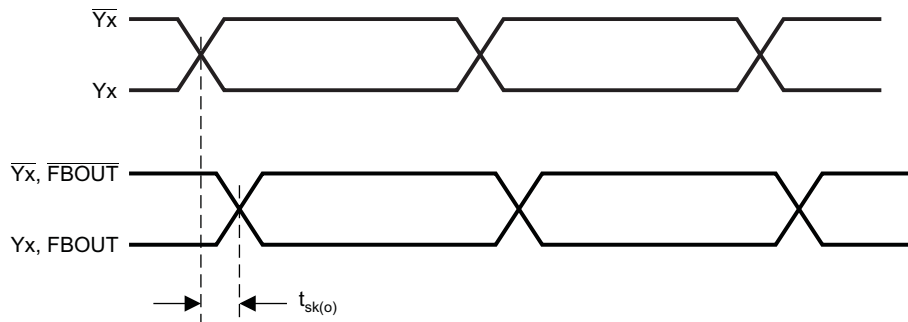
**Figure 4. Cycle-to-Cycle Jitter**
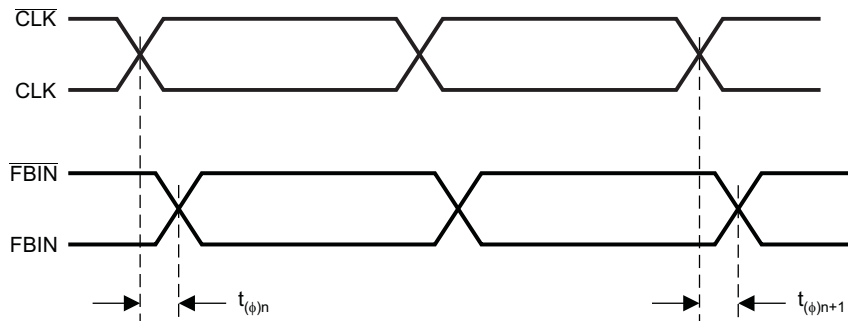


$$t_{(\phi)} = \frac{\sum_{1}^{n = N} t_{(\phi)n}}{N}$$

(N > 1000 Samples)

T0175-01

**Figure 5. Phase Offset**

# PARAMETER MEASUREMENT INFORMATION (continued)

T0176-01

**Figure 6. Output Skew**

$$t_{jit(per)} = t_{c(n)} - \frac{1}{f_0} \qquad f_0 = \text{Average Input Frequency Measured at CLK}/\overline{\text{CLK}}$$
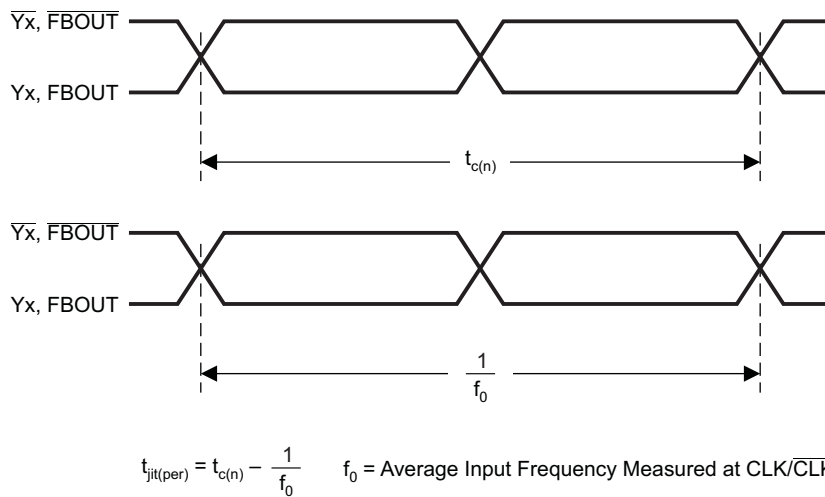
T0177-01

**Figure 7. Period Jitter**

n = Any Half Cycle

$$t_{jit(hper)} = t_{(hper\_n)} - \frac{1}{2 \times f_0} \qquad f_0 = \text{Average Input Frequency Measured at CLK}/\overline{\text{CLK}}$$
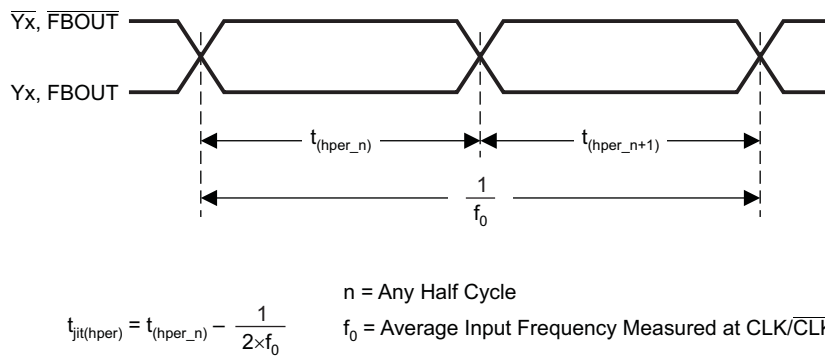
T0178-01

**Figure 8. Half-Period Jitter**

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**PARAMETER MEASUREMENT INFORMATION (continued)**



$$t_{slr(I/O)} = \frac{V_{80\%} - V_{20\%}}{t_r}$$

$$t_{slf(I/O)} = \frac{V_{80\%} - V_{20\%}}{t_f}$$
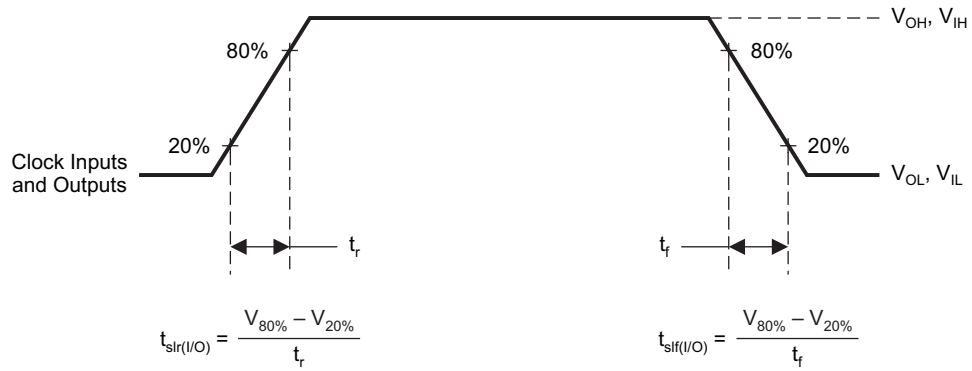
T0179-01

**Figure 9. Input and Output Slew Rates**
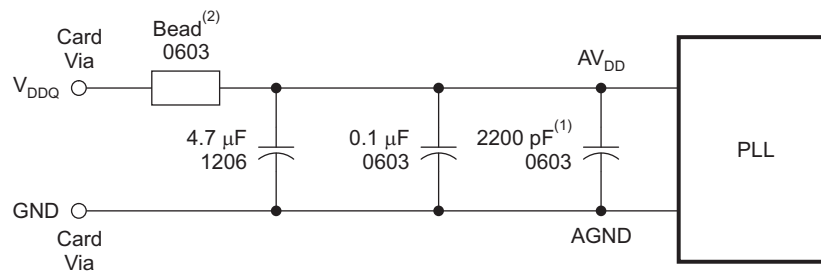


S0232-01

(1) Place the 2200-pF capacitor close to the PLL.

(2) Recommended bead: Fair-Rite P/N 2506036017Y0 or equilvalent (0.8 Ω dc maximum, 600 Ω at 100 MHz).

NOTE: Use a wide trace for the PLL analog power and ground. Connect PLL and capacitors to AGND trace and connect trace to one GND via (farthest from the PLL).

**Figure 10. Recommended AV$_{DD}$ Filtering**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCVF857DGG | ACTIVE | TSSOP | DGG | 48 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CDCVF857 | Samples |
| CDCVF857DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CDCVF857 | Samples |
| CDCVF857DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CDCVF857 | Samples |
| CDCVF857RHAT | ACTIVE | VQFN | RHA | 40 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | CKVF857 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDCVF857DGGR | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| CDCVF857RHAT | VQFN | RHA | 40 | 250 | 180.0 | 16.4 | 6.3 | 6.3 | 1.1 | 12.0 | 16.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDCVF857DGGR | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| CDCVF857RHAT | VQFN | RHA | 40 | 250 | 210.0 | 185.0 | 35.0 |

![Texas Instruments logo]

# PACKAGE MATERIALS INFORMATION

## TUBE



**T - Tube height**

**L - Tube length**

**W - Tube width**

**B - Alignment groove width**

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CDCVF857DGG | DGG | TSSOP | 48 | 40 | 530 | 11.89 | 3600 | 4.9 |

8.3 / 7.9 TYP

A

PIN 1 ID AREA

1

46X 0.5

48

12.6 / 12.4 NOTE 3

2X 11.5

24

25

B

6.2 / 6.0

48X 0.27 / 0.17

⊕ | 0.08 Ⓜ | C | A | B

C

SEATING PLANE

⌒ | 0.1 | C

1.2 / 1.0

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75 / 0.50

0.15 / 0.05

**DETAIL A**
TYPICAL

4214859/B   11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05)
TYP

SYMM

48

SYMM

24

25

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214859/B    11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05) TYP

SYMM

48

SYMM

24

25

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

**DGG (R-PDSO-G\*\*)**　　　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**



| DIM ＼ PINS \*\* | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

**4040078 / F 12/97**

NOTES: A. All linear dimensions are in millimeters.
　　　　　B. This drawing is subject to change without notice.
　　　　　C. Body dimensions do not include mold protrusion not to exceed 0,15.
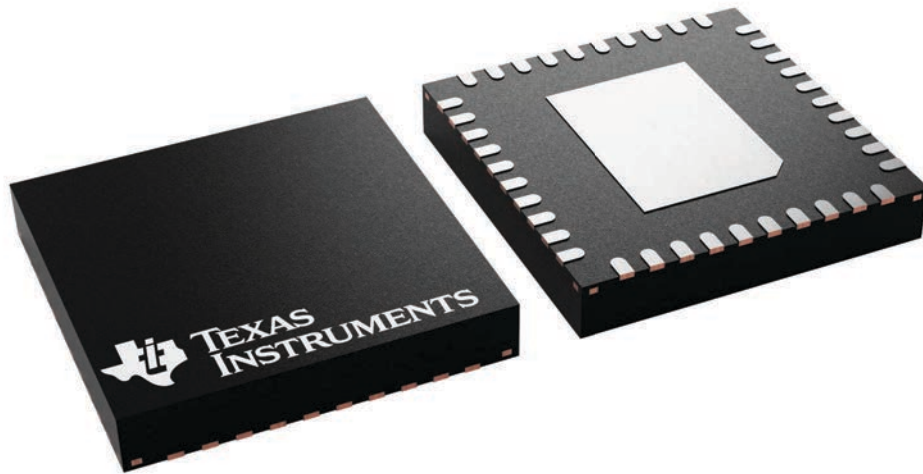　　　　　D. Falls within JEDEC MO-153

**TEXAS INSTRUMENTS**

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**RHA 40**

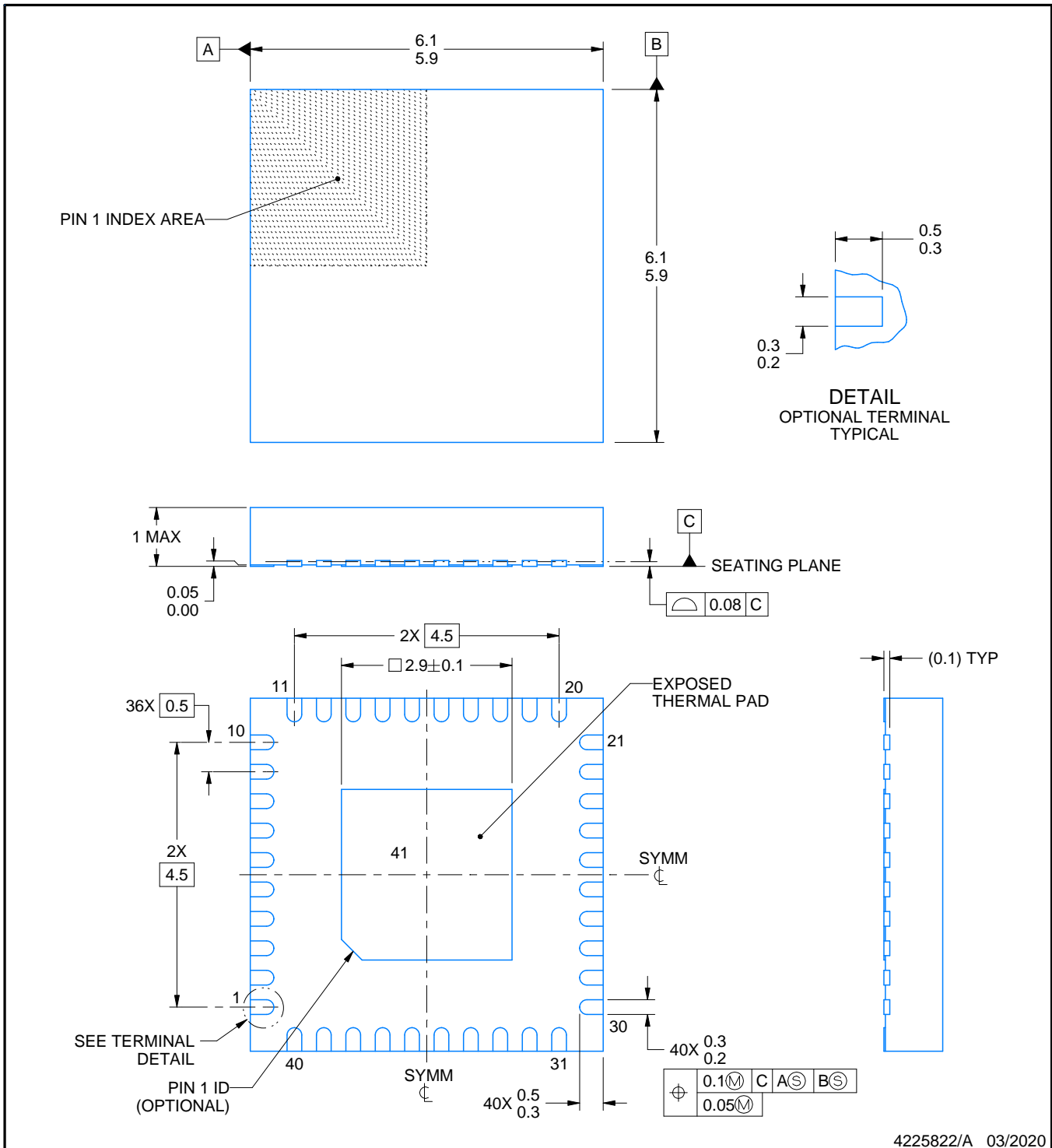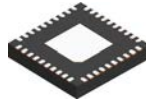**6 x 6, 0.5 mm pitch**

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

A

6.1
5.9

B

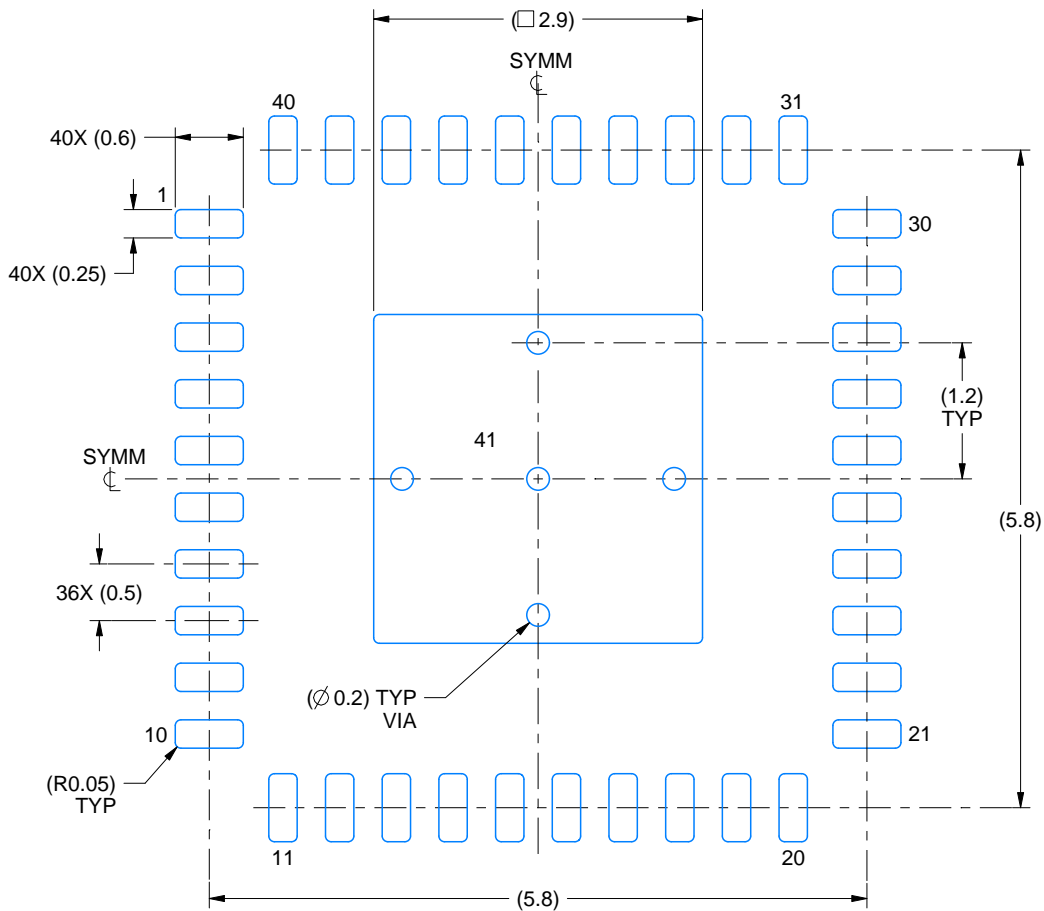PIN 1 INDEX AREA

6.1
5.9

0.5
0.3

0.3
0.2

**DETAIL**
OPTIONAL TERMINAL
TYPICAL

1 MAX

0.05
0.00

C

SEATING PLANE

⌒ 0.08 C

2X 4.5

☐2.9±0.1

(0.1) TYP

11

20

36X 0.5

10

EXPOSED
THERMAL PAD

21

2X
4.5

41

SYMM
₵

1

40

SYMM
₵

31

30

40X 0.3
0.2

SEE TERMINAL
DETAIL

PIN 1 ID
(OPTIONAL)

40X 0.5
0.3

⊕ 0.1Ⓜ C AⓈ BⓈ
0.05Ⓜ

4225822/A   03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
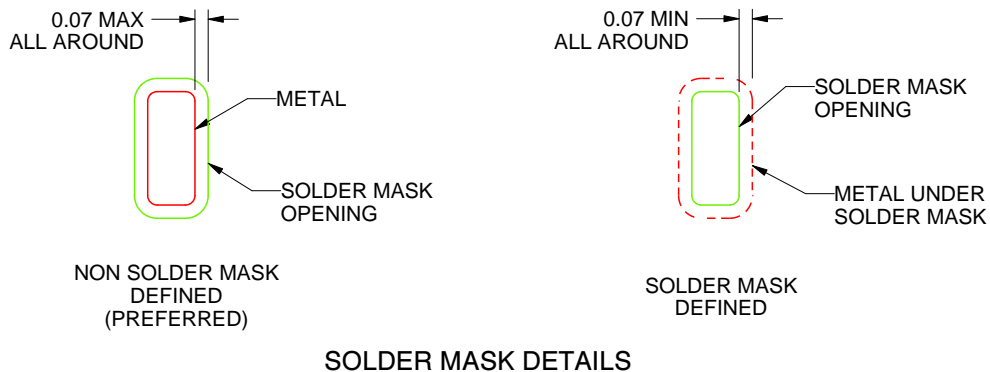
**TEXAS INSTRUMENTS**
www.ti.com

(□ 2.9)

SYMM

40X (0.6)

1

40X (0.25)

36X (0.5)

SYMM

40

31

30

41

(1.2)
TYP

(5.8)

21

10

(R0.05)
TYP

(∅ 0.2) TYP
VIA

11

20

(5.8)

**LAND PATTERN EXAMPLE**
SCALE:15X

0.07 MAX
ALL AROUND

METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

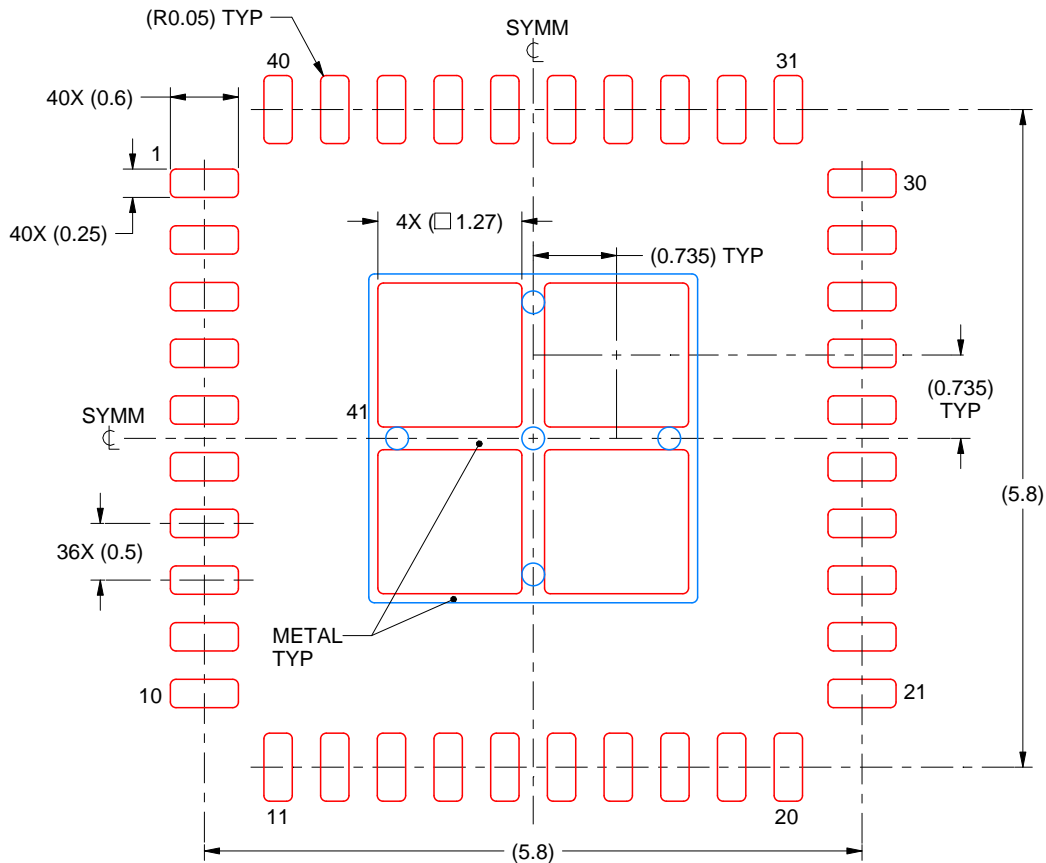4225822/A   03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.

## RHA0040D

(R0.05) TYP

SYMM

40

40X (0.6)

1

40X (0.25)

31

30

4X (□1.27)

(0.735) TYP

41

SYMM

(0.735) TYP

36X (0.5)

(5.8)

METAL TYP

10

21

11

20

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
76.46% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4225822/A   03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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